Hardware Details of the 68000

- CPU Pin Descriptions
- System Timing Diagrams

CPU Pin Descriptions

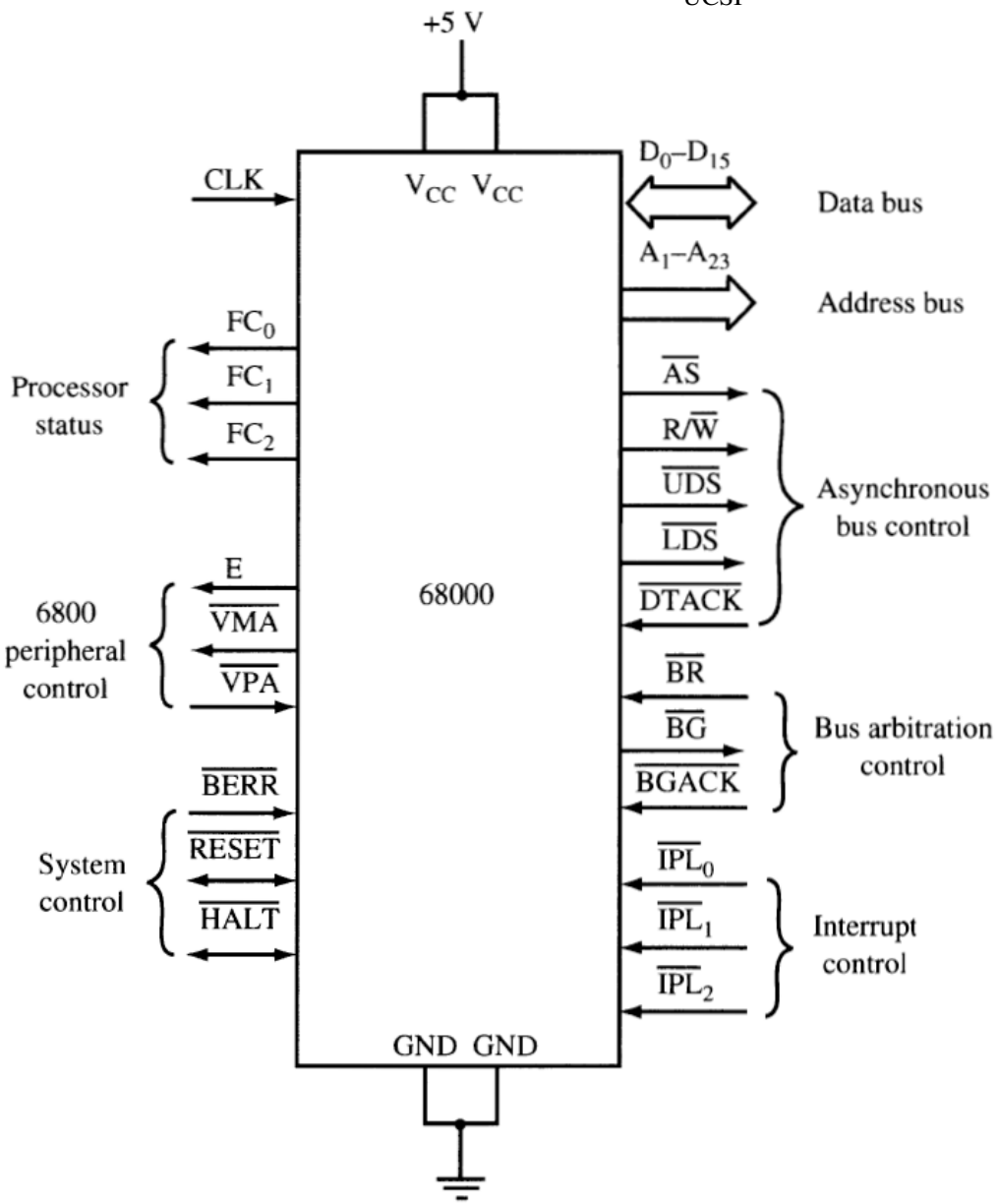


Figure 7.1: 68000 CPU input and output signals (pg 240) [1]

V_{CC}, GND, CLK

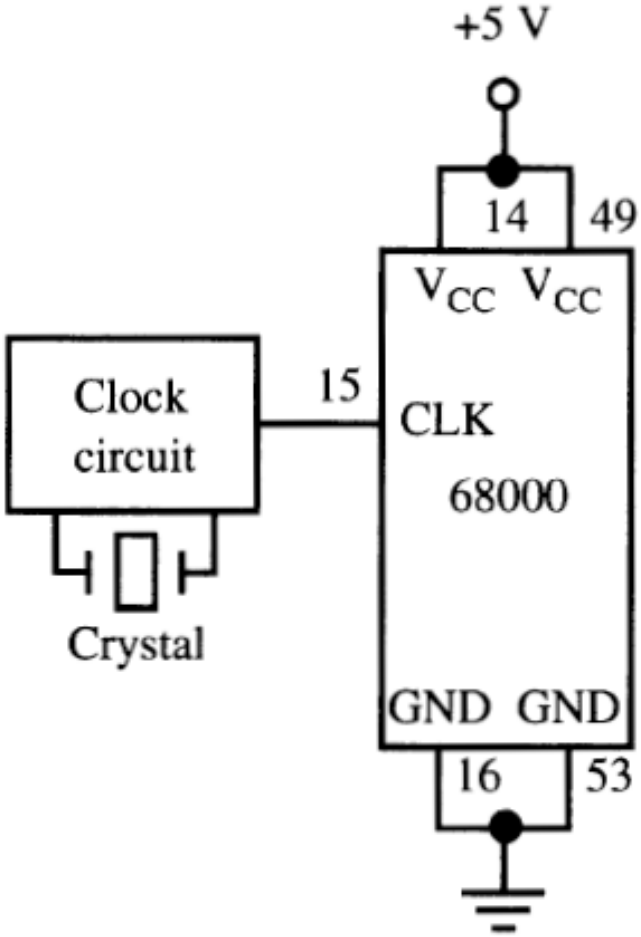
- Processor power and clock inputs.
- 2 pins each for VCC and GND
- Both must be connected

VCC:

- 8MHz, 5V $\pm$ 5%, 1.5 watts

CLK:

- Max t_{rise} and t_{fall} are 10ns (all versions except 5ns for 12.5MHz and 16MHz)
- TTL-compatible with 50 percent duty cycle.



FC_0, FC_1, and FC_2

- FC_0, FC_1, and FC_2 are function code outputs
- Informs external circuitry of current internal processing state of the 68000.
- Only valid when $\overline{AS}$ is active.

Table 7.1: Function code outputs (pg 241) [1]

FC_2	FC_1	FC_0	Cycle type
0	0	0	Reserved*
0	0	1	User data
0	1	0	User program
0	1	1	Reserved*
1	0	0	Reserved*
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	Interrupt acknowledge

*By Motorola, for future use.

- Frequently used to restrict memory accesses by connecting the FC pins to the memory address decoding circuitry.

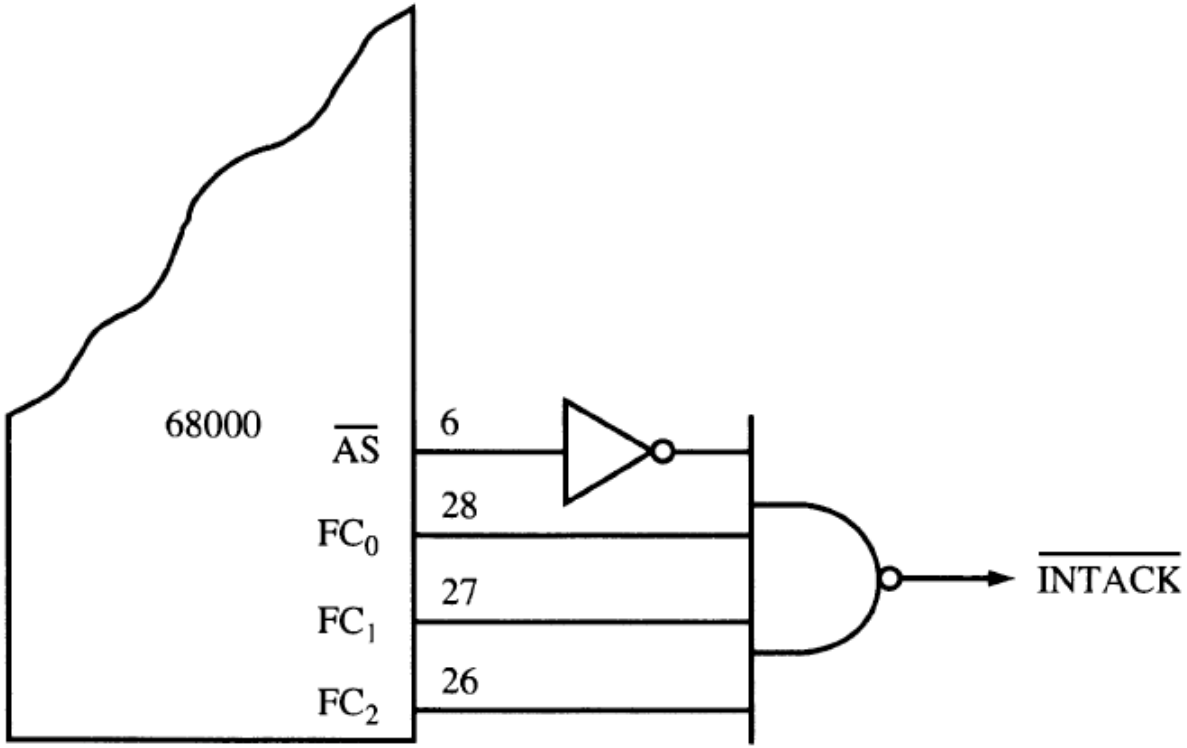
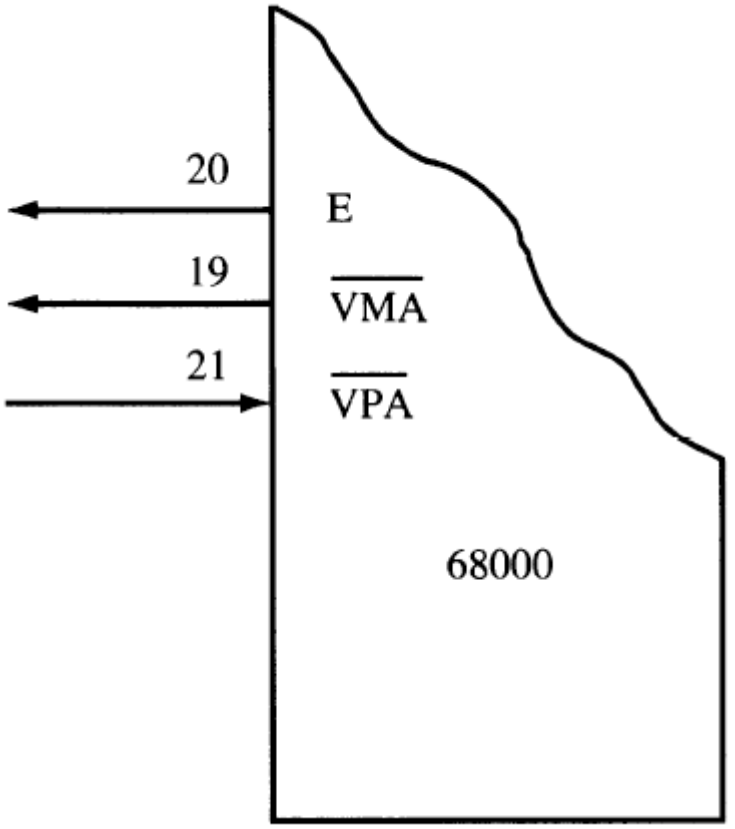


Figure 7.3: Interrupt acknowledge cycle decoder (pg 242) [1]

E, $\overline{VMA}$, and $\overline{VPA}$

- Provides the capability to control older 6800 peripherals.
- E clock, $\overline{VMA}$ (valid memory address), and $\overline{VPA}$ (valid peripheral address)



E clock:

- Generates proper timing signals for 6800 peripherals.
- 1/10th of 68000's clock frequency, with 40% duty cycle (high for 4 CLK cycles, low for 6 CLK cycles)

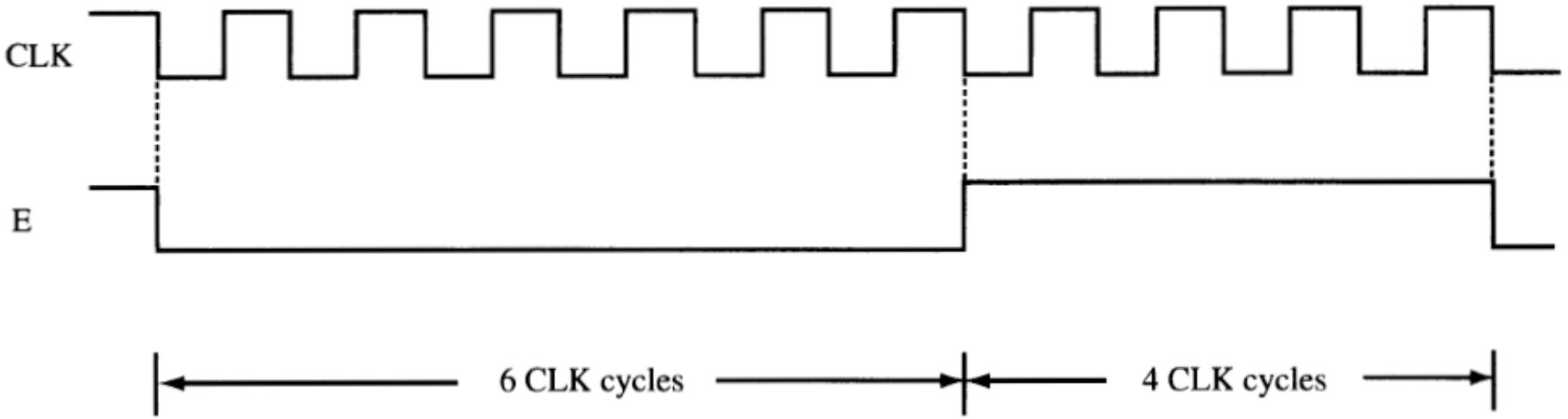


Figure 7.5: Timing relationship between CLK and E (pg 243) [1]

Sequence of events during 6800 peripheral access:

- The 68000 places address of 6800 peripheral on A_1 through A_{23}.
- $\overline{VPA}$ input is activated (low) to request synchronization of 68000
- 68000 synchronizes with the E clock, then activates $\overline{VMA}$ (outputs a low).
- Data transfer takes place.

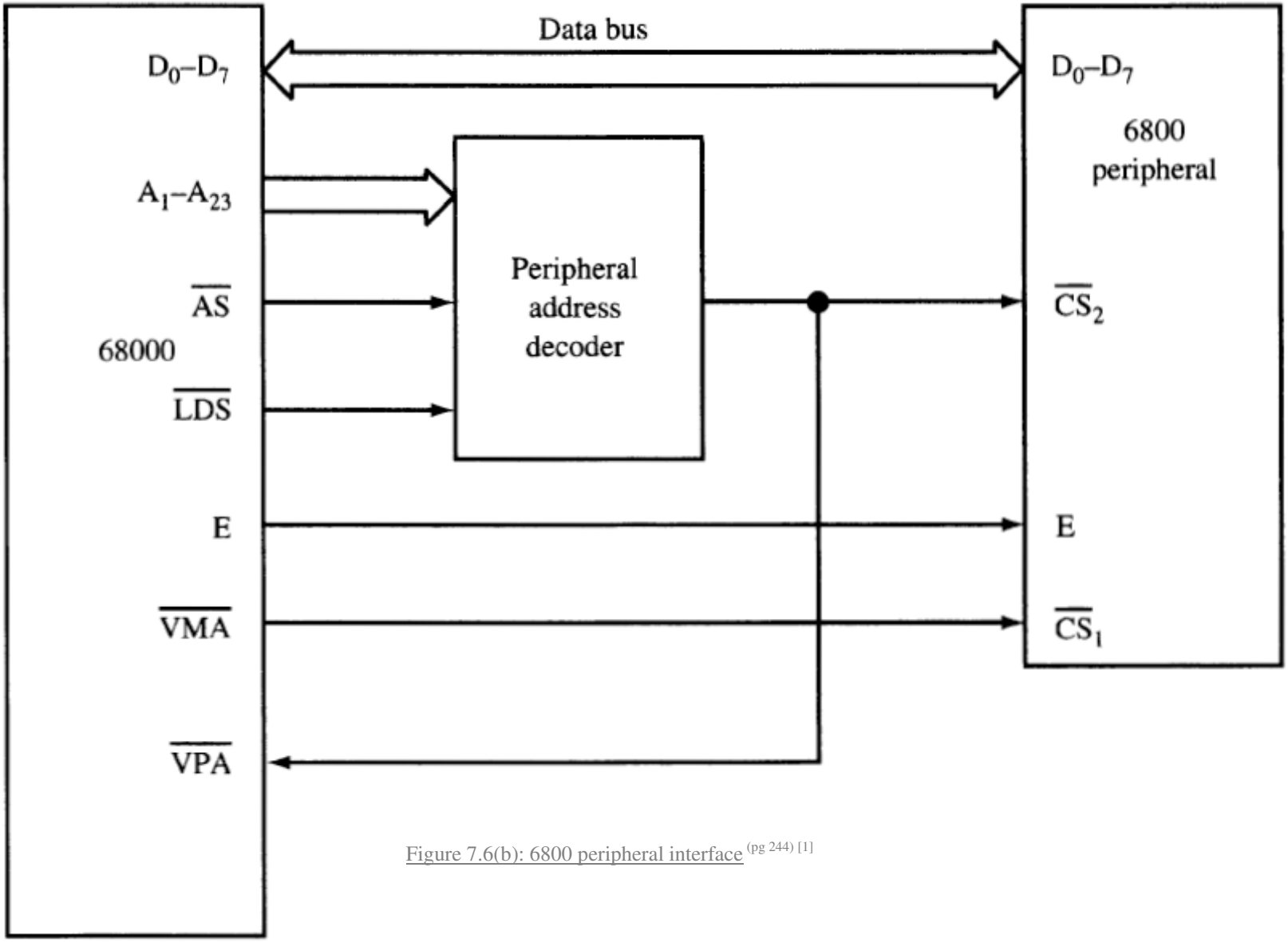


Figure 7.6(b): 6800 peripheral interface (pg 244) [1]

$\overline{RESET}$, $\overline{HALT}$, and $\overline{BERR}$

- Provides system control.
- $\overline{RESET}$, $\overline{HALT}$, and $\overline{BERR}$ (buss error) are panic buttons of the 68000
- External circuitry pulls $\overline{BERR}$ low to indicate to the 68000 that an error has occurred during execution of current bus cycle.
- $\overline{RESET}$ and $\overline{HALT}$ lines are bi-directional

Sequence of events when bus error occurs:

- If $\overline{HALT}$ is not asserted when bus error occurs:
  - The 68000 will terminate the current failed cycle and start bus error exception processing.

If $\overline{HALT}$ was asserted before or at the same time as $\overline{BERR}$:

- The 68000 will terminate the current failed cycle, and enter a "do nothing" state
- Once the $\overline{HALT}$ line is deactivated, the processor will rerun the previous cycle
- Note that $\overline{BERR}$ must be deactivated at least one clock cycle before $\overline{HALT}$ is deactivated.

Example (Power On Hardware Reset):

- $\overline{RESET}$ and $\overline{HALT}$ both act as inputs
- After power on, $\overline{RESET}$ and $\overline{HALT}$ are taken low for at least 100ms
- This stabilizes V_{CC} and results in total processor reset

Example (Normal Execution Hardware Reset):

- $\overline{RESET}$ and $\overline{HALT}$ both act as inputs
- Asserting $\overline{RESET}$ and $\overline{HALT}$ at least 10 clock cycles resets the 68000

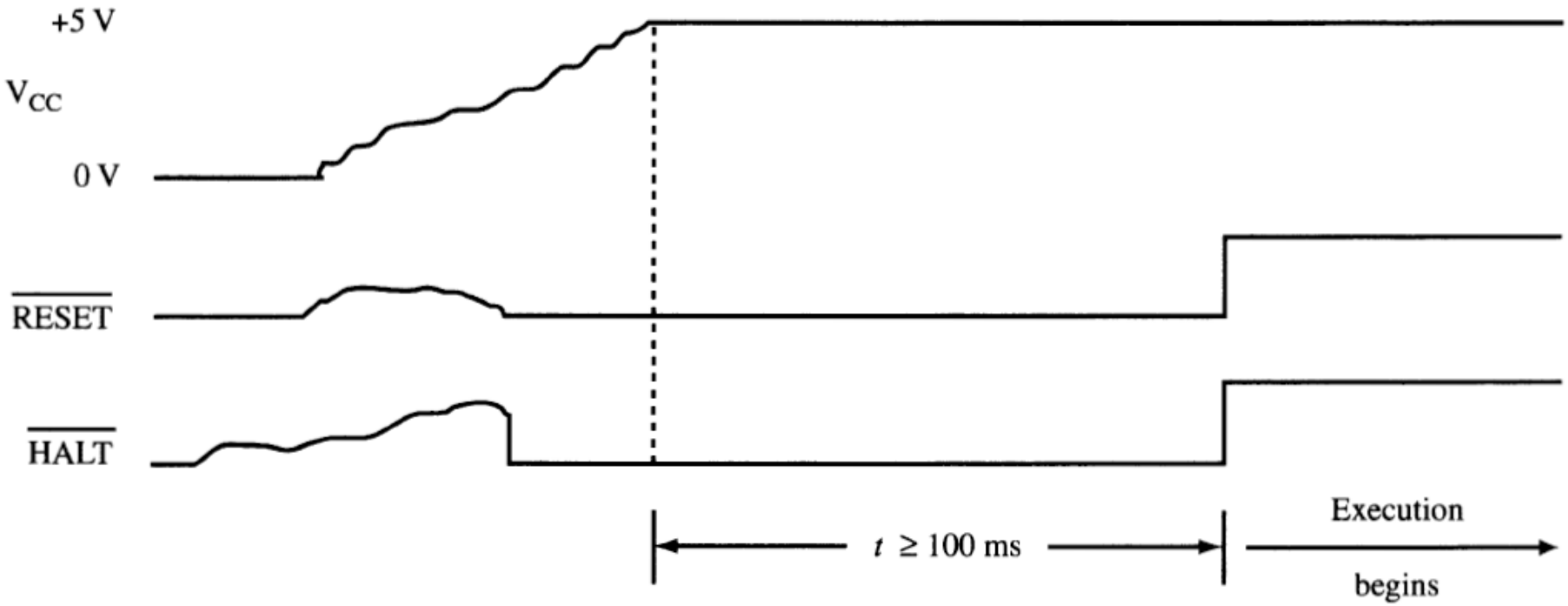


Figure 7.9: Power-on $\overline{RESET}$ and $\overline{HALT}$ timing (pg 246) [1]

Example (Normal Execution Peripheral Soft Reset):

- $\overline{RESET}$ acts as an output
- The RESET instruction causes the 68000 to output a low level on $\overline{RESET}$ for 124 clock cycles.
- This resets all external circuitry connected to $\overline{RESET}$ without affecting the state of the processor.

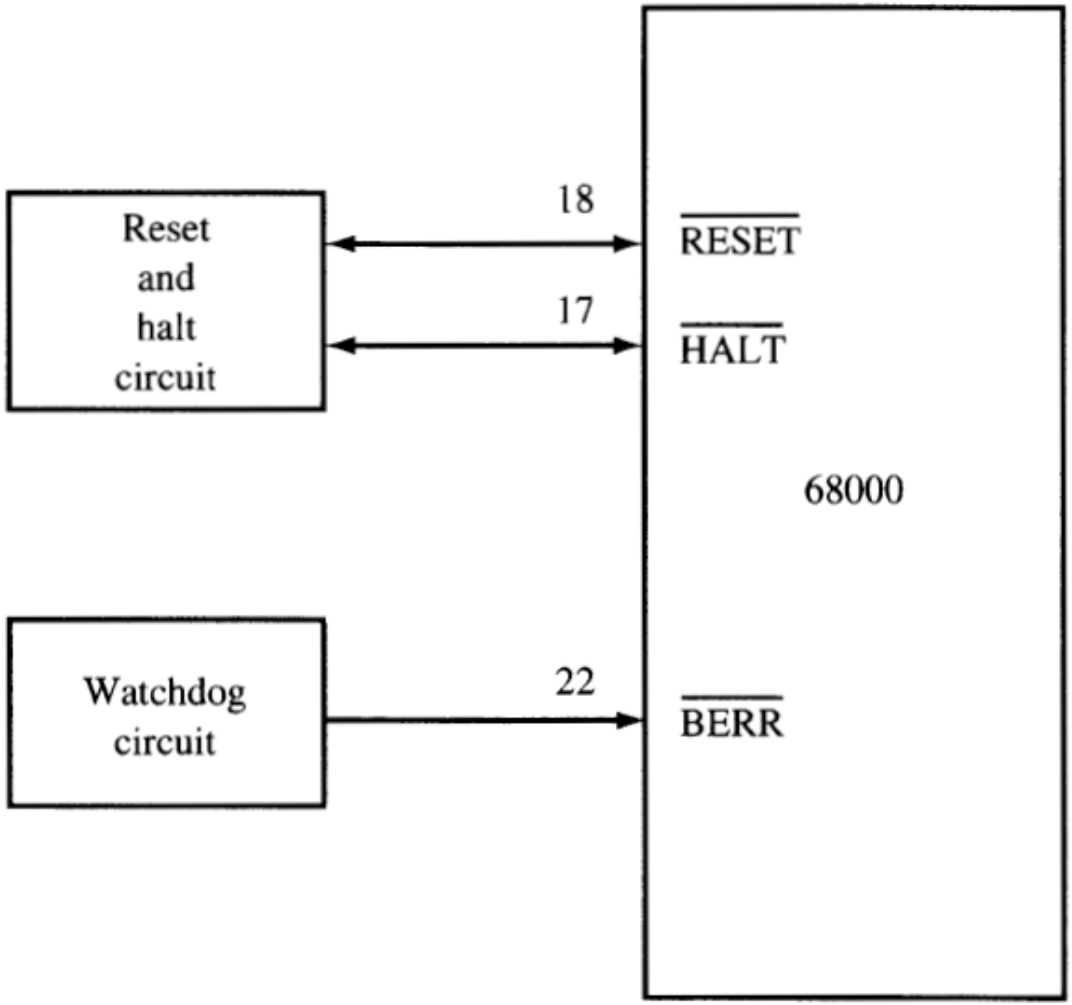


Figure 7.7: Power-on $\overline{RESET}$ and $\overline{HALT}$ timing (pg 245) [1]

Example (External Peripheral Halt):

- $\overline{HALT}$ acts as an input
- $\overline{HALT}$ may be driven low at any time by an external device.
- The processor then completes the current bus cycle and halts:
  - All tristate signals are set to high-impedance
  - All control signals are inactive.
- Execution returns to normal when $\overline{HALT}$ is deactivated

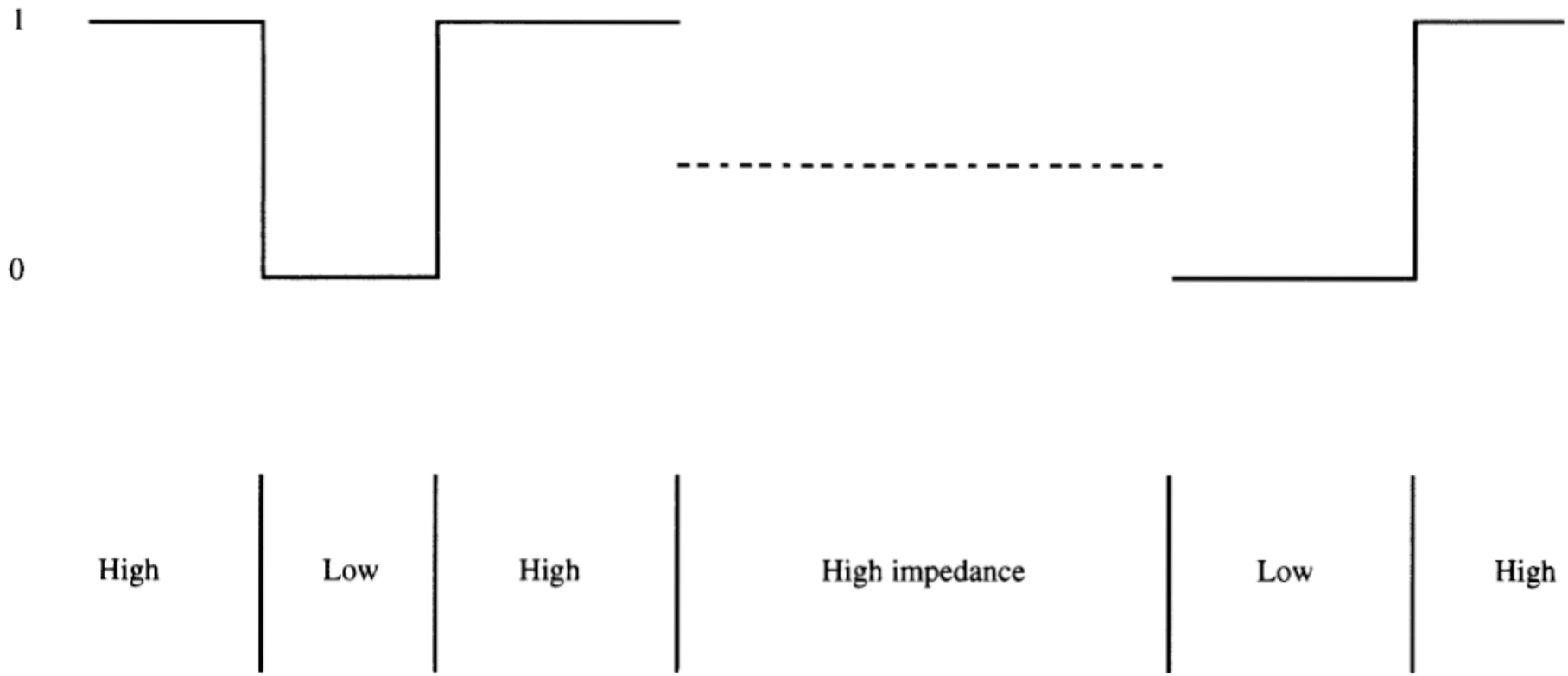


Figure 7.8: Tristate signal levels (pg 246) [1]

$\overline{IPL_0}$, $\overline{IPL_1}$ and $\overline{IPL_2}$

- Provides interrupt control/request
- $\overline{IPL_0}$, $\overline{IPL_1}$ and $\overline{IPL_2}$ are used by external circuitry to send an interrupt request to the 68000.

- Vectored and auto-vectored interrupts may be requested.

Interrupt			
$\overline{IPL_2}$	$\overline{IPL_1}$	$\overline{IPL_0}$	Interrupt level*
1	1	1	0 (Lowest, none)
1	1	0	1
1	0	1	2
1	0	0	3
0	1	1	4
0	1	0	5
0	0	1	6
0	0	0	7 (Highest, nonmaskable)

*Note the inversion of the binary bits needed on $\overline{IPL_2}$–$\overline{IPL_0}$.

Figure 7.2: Interrupt level encoding (pg 246) [1]

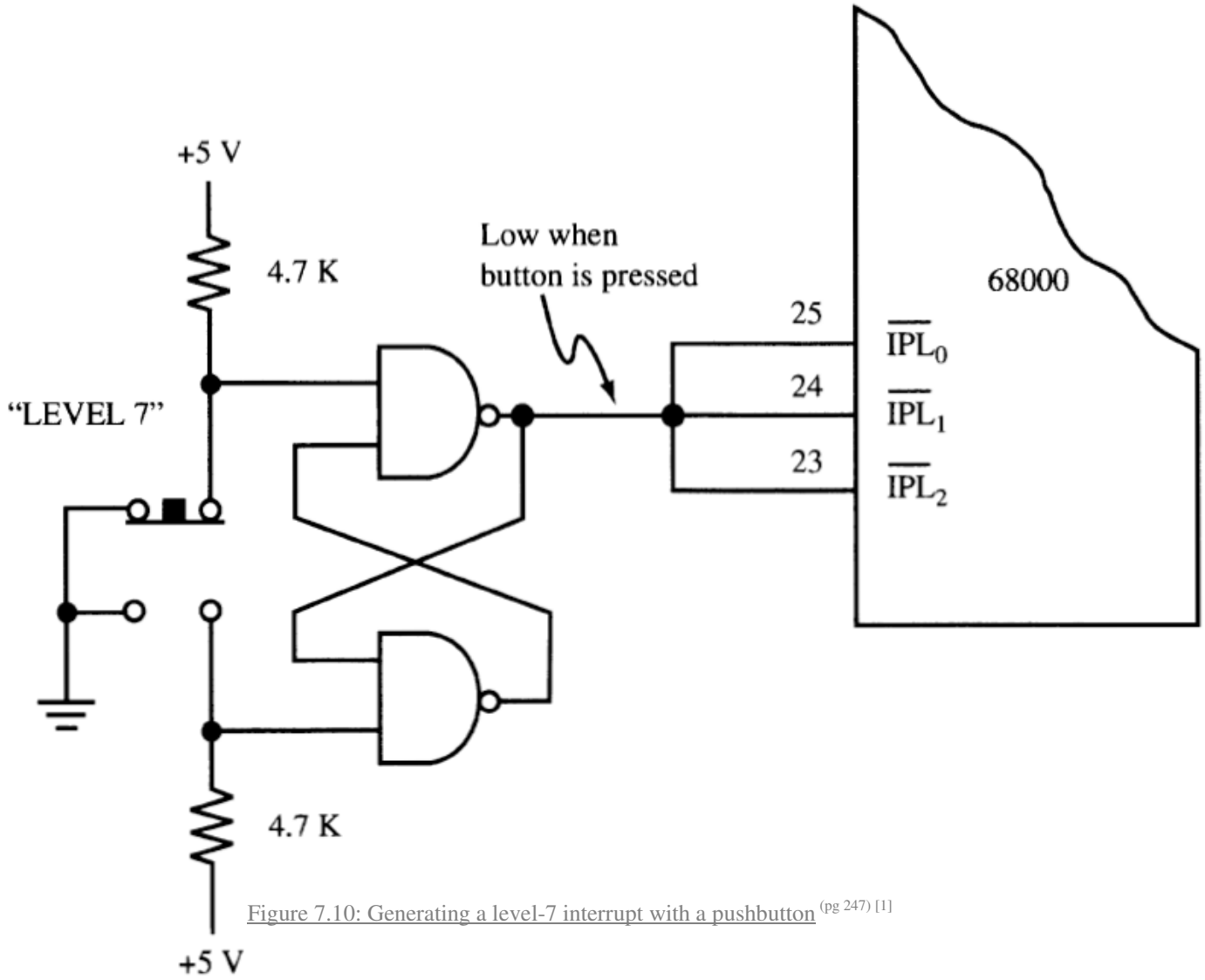


Figure 7.10: Generating a level-7 interrupt with a pushbutton (pg 247) [1]

$\overline{BR}, \overline{BG}$ and $\overline{BGACK}$

- Provides bus arbitration control (use to place 68k in a wait state while hardware connected to the bus)
- $\overline{BR}$ (bus request), $\overline{BG}$ (bus grant), and $\overline{BGACK}$ (bus grant acknowledge) are used when a device (DMA controller or another processor) is taking over control of the bus

Sequence of events for bus arbitration control:

- Requesting device (bus master) activate $\overline{BR}$ low to request the 68k system bus
- 68k will respond to bus master by asserting $\overline{BG}$ low to indicate its willingness to release control of the bus at the end of the current cycle.
- To take control, the new bus master asserts $\overline{BGACK}$
- When the new bus master wishes to relinquish control of the bus, it does so by negating $\overline{BGACK}$

There are 4 conditions that must be met before the new bus master may activate $\overline{BGACK}$:

- $\overline{BG}$ is active
- $\overline{AS}$ is inactive
- $\overline{DTACK}$ is inactive
- $\overline{BGACK}$ is inactive

Provides asynchronous bus control (for proper operation of external hardware)

- All lines are outputs except $\overline{DTACK}$ (input)

- $\overline{AS}$ (address strobe) : to indicate that a valid memory address exists on the address bus.

- $R/\overline{W}$ (read/write) : determine whether the current cycle is a read or write.
- $\overline{UDS}$ (upper data strobe)
- $\overline{LDS}$ (lower data strobe)

  - To transfer 8 bits (1 byte) of data: either $\overline{UDS}$ or $\overline{LDS}$ asserted
  - To transfer 16 bits: both $\overline{UDS}$ and $\overline{LDS}$ asserted low

- $\overline{DTACK}$ (data transfer acknowledge)

  - When $\overline{DTACK}$ is asserted by external hardware, the 68000 recognizes that the current bus cycle can be completed