Australian National University Department of Engineering Automated Systems Lab Business Card Computers Bob's Card Computer Mk II
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Bob's Card Computer Mk II

Introduction

This page describes Bob's Card Computer Mk II (bobcc2) which is an enhancement of Bobs's Card Computer (bobcc), in turn based on Motorola's Business Card Computer (BCC).

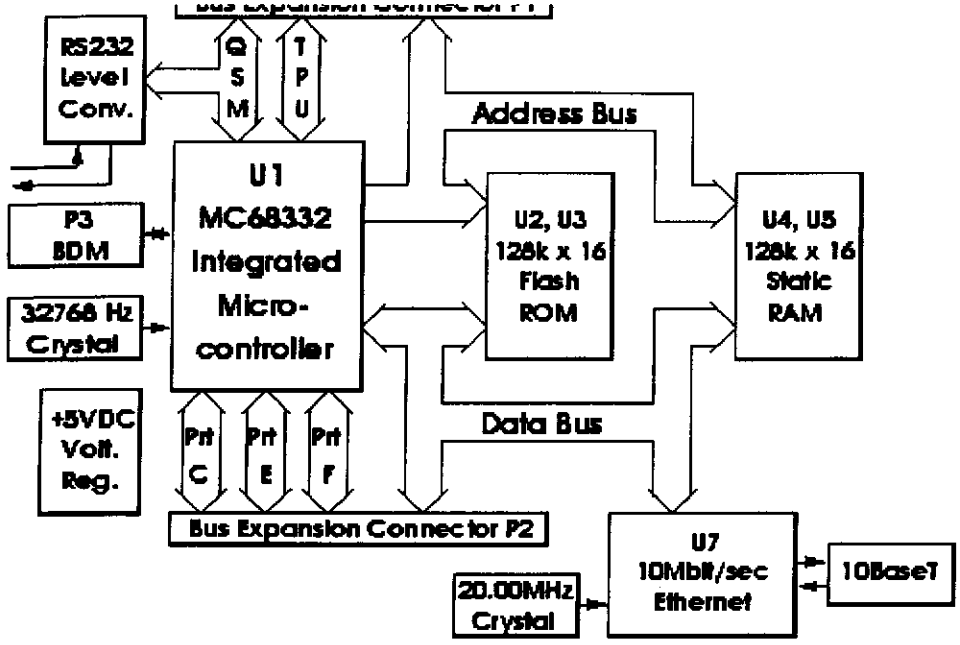
The main enhancements in bobcc2 over bobcc are:

- addition of a 10 MBit/sec Ethernet interface (10BaseT)
- addition of the separate Background Debug Mode (BDM) connector
- provision for on-board voltage regulator
- provision for up to 512kbytes Flash ROM
- more complete set of signals brought out on connector P2
- 4-layer circuit board with ground plane
- 4 x 2.5mm mounting holes for standalone operation without Bus Connectors

Features

- 132-pin MC68332 microprocessor operating at 16.6, 20 or 25MHz
- 2 x 32 pin JEDEC sockets hold 128k x 16 or 256k x 16 Flash ROM, EPROM or EEPROM
- 32k x 16 or 128k x 16 fast static RAM (in 2 x 28 pin or 2 x 32 pin 0.3" skinny-DIPs)
- SMC 91C94 10 MBit/sec Ethernet interface (10BaseT)
- 3-wire RS-232 compatible serial interface with on-board +/- 9v supply
- Motorola Business Card Computer (BCC) compatible form factor - 3.5" x 2.3"
- Motorola BCC compatible Bus Connector pinouts implemented as 2 x DIN41612 64-way sockets
- 10-pin Background Debug Mode (BDM) connector
- on board +5v regulator - allows operation from a DC plug-pack
- 4-layer circuit board with ground plane

Block Diagram



Bob's Card Computer MkII (bobcc2)

Read Only Memory (ROM)

bobcc2 has provision for two 28 pin or 32 pin JEDEC-compatible 0.6" DIP sockets for non-volatile program storage. These sockets (U2 and U3) are physically located straddling the skinny-DIP static RAM devices at U4 and U5, using two 16-way turned-pin socket strips each.

These sockets can be loaded with:

- Flash ROM devices (eg. AMD 29F010 128k x 8 or AMD 29F020 256k x 8)
- UV Erasable Programmable ROM (EPROM) devices of similar size; or
- Electrically Erasable Programmable ROM (EEPROM) devices of similar size

for a total of up to 512kbytes of ROM memory.

Pin 22 of each of these devices (~Chip Select) is permanently tied to ground (enabled) for faster access times, but possibly at the expense of higher power consumption for some devices.

~CSBOOT from the MC68332 is connected to pin 24 of each device (~Output Enable) to enable reading from these devices at system boot time. If it is desired to boot from external ROM devices, then these devices (U2 and U3) should be removed from their sockets.

Jumper J3 selects whether +5v or A18 goes to pin 30 of each device. For 128k x 8 devices, this jumper should be set to +5v (the default), otherwise the track on the bottom of the board should be cut and the jumper set to A18.

Ethernet Controller

The optional 10 MBit/sec Ethernet Controller is implemented with two ICs and some other discrete components all mounted on the bottom side of the circuit board except for LED1 mounted on the top side.

The Ethernet controller chip is an SMC 91C94 device at U7 implemented as a 100 pin Quad Flat Pack (QFP100). This chip provides an almost complete interface from an ISA or PCMCIA bus to a 10BaseT

(QFP100). This chip provides an almost complete interface from an ISA or PCMCIA bus to a 10BaseT or AUI interface including buffer memory. In this case, a minimal bus interface is implemented to the MC68332 processor.

U8, a 74HC14 hex schmitt-trigger input inverter, is used to:

- provide an active-high RESET signal (on pin 6) for the 91C94 from the active-low ~RESET signal (input on pin 5) from the MC68332 and Bus Connector P1.
- provide an active-low IRQ signal (on pin 8) to MC68332 ~IRQ3 from the active-high INTR0 signal (input on pin 9) from the 91C94.

All accesses to the 91C94 are controlled by MC68332 chip select outputs ~CS5 and ~CS6. ~CS5 drives the ~IORD input and should be set up to activate on read cycles only. ~CS6 drives the ~IOWR input and should be set up to activate on write cycles only. These chip selects also need to be programmed appropriately to provide the correct setup and access times.

The interface to the 10BaseT Ethernet is via a pulse transformer with limiting resistors R2, R3, R4 and R5 on the transmit side and by the parallel resistor R9 on the receive side. The four 10BaseT Ethernet signals are then brought out on connector P5 where they can be connected to standard RJ-45 connectors.

The 20.000MHz Crystal (XTAL2) is connected to the 91C94 via a 100kohm series resistor (R7) and a 20Mohm parallel resistor (R6), as well as two 22pf bypass capacitors (C17 and C18).

The LED LED1 is connected to the RXLED output of the 91C94 via a 470ohm resistor R10 to indicate Ethernet receive traffic activity. The other LED outputs of the 91C94 are not used in this implementation.

The usual 8-pin 64 x 16 serial EEPROM device that is used to store the MAC layer address is omitted in this implementation, due to board space restrictions. The 91C94 signal ENEEP is tied to ground to disable the EEPROM interface.

Limitations

Due to the omission of the serial EEPROM for non-volatile storage of a unique MAC layer address, it is up to the MC68332 ROMs to store this address that the processor can load into the 91C94 during initialisation.

The proposed option is to store the lower 4 bytes of a unique MAC address at Boot ROM locations 0 - 3, which is normally used to initialise the Stack Pointer at reset. As the Stack Pointer can't be used until after the RAM Chip Selects are initialised, the Stack Pointer can be explicitly set at that time. Therefore, storing the MAC layer address here will not upset normal system operation.

To simplify the bus interface logic (to nil), only 16-bit transfers to/from the 91C94 controller are supported. A0 and ~SBHE inputs on the 91C94 are both tied to ground to force this. The Address ENable (AEN) input is also tied to ground and the BALE input is tied to +5v to permanently enable address decoding. The 91C94 address bus is permanently tied to the address range 0x300 - 0x30e. Due to the reverse byte-ordering of the ISA bus versus the MC68332, data bits D0 - D7 of the 91C94 are connected to D8 - D15 of the MC68332 and, similarly, D8 - D15 of the 91C94 are connected to D0 - D7 of the MC68332.

Voltage Regulator

To facilitate use of this board in remote embedded environments, a +5V DC Low-voltage DropOut (LDO) surface mount voltage regulator (U9) is included on the board. This regulator allows the use of an unregulated DC supply, such as a plug-pack, to power the board (and limited peripheral devices). Such a supply must be capable of supplying at least 7V (unregulated) at 500mA (min).

Chip Select Usage

The usage of the 12 MC68332 chip selects on bobcc2 is backward compatible with the Motorola BCC, but several more are used for Flash ROM programming and for the Ethernet controller.

- ~CSBOOT - read enable for the two Boot ROMs (U2 and U3) - also on P2:25
- ~CS0 - write enable for high-byte (even) RAM (U5) - NOT on P2
- ~CS1 - write enable for low-byte (odd) RAM (U4) - NOT on P2
- ~CS2 - read enable for both RAMs (U4 and U5) - NOT on P2
- ~CS3 - write enable for high-byte (even) Flash ROM (U3) - NOT on P2
- ~CS4 - write enable for low-byte (odd) Flash ROM (U2) - NOT on P2
- ~CS5 - read enable for optional Ethernet controller (U7) - also on P2:35
- ~CS6 - write enable for optional Ethernet controller (U7) - also on P2:34
- ~CS7 - unused - on P2:33
- ~CS8 - unused - on P2:32
- ~CS9 - unused - on P2:31
- ~CS10 - unused - on P2:30

Interrupt Request Usage

Most of the interrupt request lines from the MC68332 (~IRQ1 - ~IRQ7) are brought out directly to respective pins on connector P2. However, if the optional on-board Ethernet controller is implemented, then it is hard-wired to use ~IRQ3 via U8 pins 9 (input) and 8 (output).

Errata

- missing 820 ohm pull-up on ~RESET line - there are several places where a SMD 0603 resistor can be placed between the ~RESET line and VDD (+5v) including near pin 57 of P1 on the top layer, or between pins 7 and 9 of P3 on the bottom layer.
- missing 10kohm pull-up on ~BKPT line. Again, there is an ideal location for the addition of an SMD 0603 resistor on the top side of the board near pin 55 of P1.
- voltage regulator U9 has it's input and output pins reversed. The work-around is to swap the functions of the pins connected to the input and output of U9, although doing so will makes it less convenient to jumper the output to the VDD rail of the module. This will need to be done with wire-wrap wire.
- chip selects ~CS0 - ~CS4 remain unconnected to respective pins of P2.
