

80-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

KS0083/84 is a graphic type LCD driver LSI which is fabricated by CMOS process for high voltage. In case of segment driver, can be selected 4 bit, 1 bit data transfer or chip select mode. KS0084 is reverse type of KS0083

FUNCTION

- DOT MATRIX LCD DRIVER with 80 channel output.
- Input/Output
 - Output: 80 channel waveform for LCD driving
 - Input: • parallel display data and control signal from controller
 - bias voltage (V_3 , V_4 , V_{SS})

FEATURES

- Power supply voltage: $-5V \pm 10\%$
- LCD driving voltage: $-24V(\text{typ}) (V_{EE})$
- Interface

type 1		type 2		type 3	
COM	SEG	COM	SEG	COM	SEG
KS0083/84	KS0083/84	KS0103	KS0083/84	KS0083/84	KS0104

- 100QFP and bare chip available

BLOCK DIAGRAM

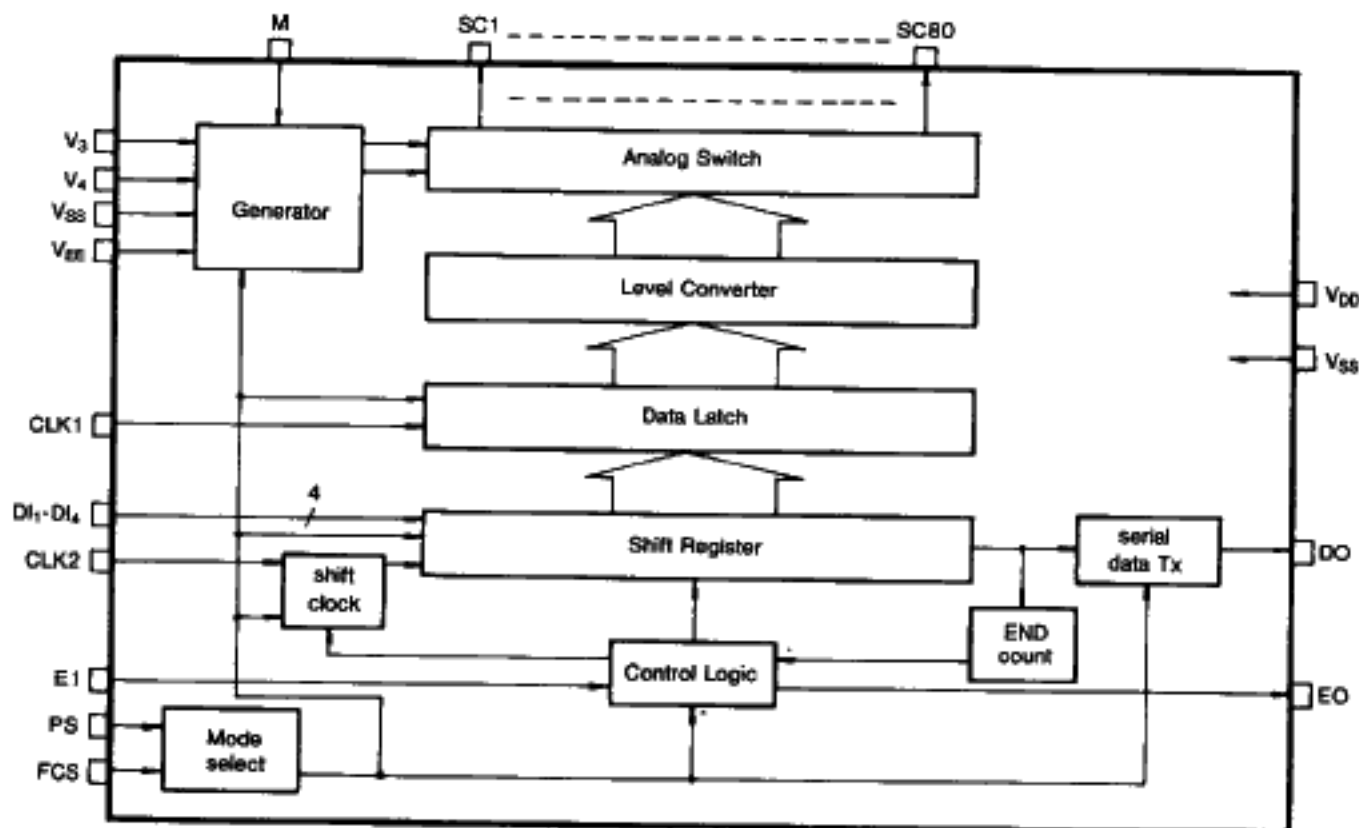
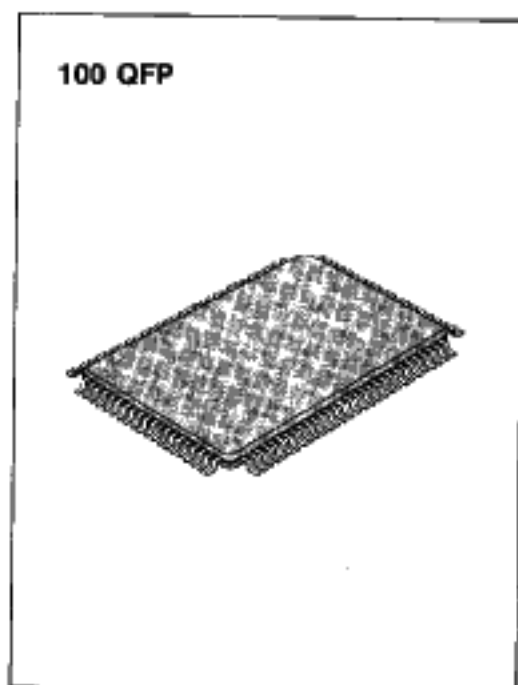


Fig. 1 KS0083/84 functional block diagram.



PIN CONFIGURATION

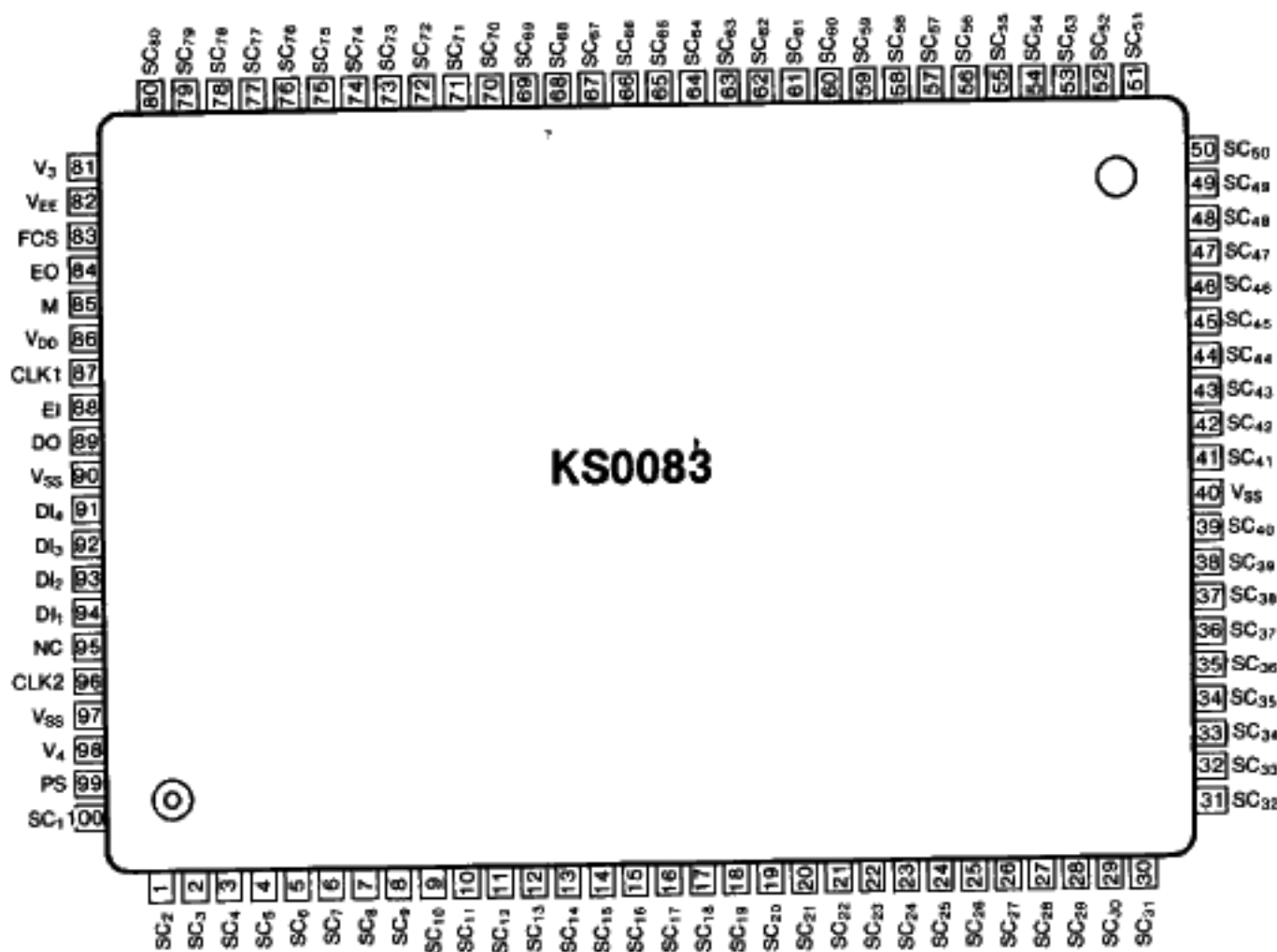


Fig. 2. 100 QFP Top View

PIN CONFIGURATION

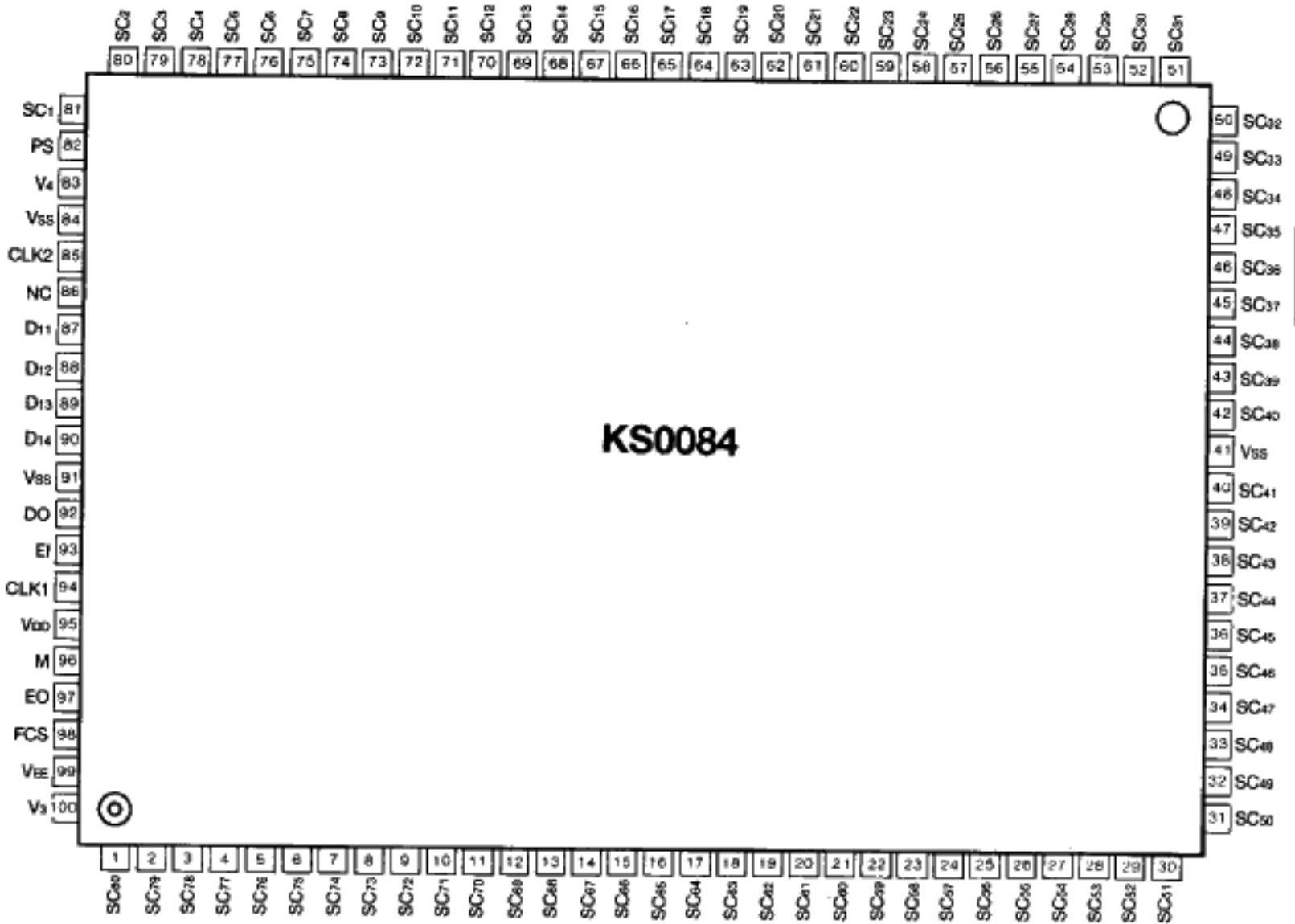


Fig.3 100QFP Top View.

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PIN FUNCTIONAL DESCRIPTION

Pin (No.)	Input Output	Description	Interface																																						
SC1~SC80 (100, 1-39, 41-80)	Output	LCD driver output terminals (80 Channel)	LCD																																						
Power supply	VSS(40,90,97)	GND (0V)	Power Supply																																						
	VEE (82)	LCD driving Voltage (-24V)																																							
	VDD(86)	Internal Logic driving Voltage																																							
V3, V4(81, 98)		Bias Voltage input for LCD drive: Non-select Level (Must maintain VSS>V3>V4>VEE.)	Power																																						
FCS, PS (83, 89)	Input	<p>Mode Select inputs. (refer to application circuit)</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th>FCS</th> <th>PS</th> <th>Com/seg driver</th> <th>Input mode</th> <th>Chip select mode</th> <th>DO Output</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Segment driver</td> <td>1 bit serial input</td> <td>X</td> <td>O</td> </tr> <tr> <td>L</td> <td>H</td> <td>Segment driver</td> <td>4 bit parallel input</td> <td>O</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>Segment driver</td> <td>1 bit serial input</td> <td>X</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>Common driver</td> <td>Serial input</td> <td>O</td> <td>O</td> </tr> </tbody> </table> <ul style="list-style-type: none"> - In case of serial input mode, DI1 is data input pin and DO is data output pin - In case of 4 bit parallel input mode, Data input and output are; <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <tr> <td>DI1</td> <td>SC1, SC5, ...SC77</td> <td>DI2</td> <td>SC2, SC6, ...SC76</td> </tr> <tr> <td>DI3</td> <td>SC3, SC7, ...SC79</td> <td>DI4</td> <td>SC4, SC8, ...SC80</td> </tr> </table> <div style="display: flex; justify-content: space-around; margin-top: 10px;"> <div style="border: 1px solid black; padding: 5px; text-align: center;"> <p>4 bit Data shift direction</p> </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> <p>1 bit Data shift</p> </div> </div> <ul style="list-style-type: none"> - In case of the common driver, the data transfer clock is CLK2 - Non-used data input pins are set to VSS or VDD to minimize current consumption 	FCS	PS	Com/seg driver	Input mode	Chip select mode	DO Output	L	L	Segment driver	1 bit serial input	X	O	L	H	Segment driver	4 bit parallel input	O	H	H	L	Segment driver	1 bit serial input	X	H	H	H	Common driver	Serial input	O	O	DI1	SC1, SC5, ...SC77	DI2	SC2, SC6, ...SC76	DI3	SC3, SC7, ...SC79	DI4	SC4, SC8, ...SC80	
FCS	PS	Com/seg driver	Input mode	Chip select mode	DO Output																																				
L	L	Segment driver	1 bit serial input	X	O																																				
L	H	Segment driver	4 bit parallel input	O	H																																				
H	L	Segment driver	1 bit serial input	X	H																																				
H	H	Common driver	Serial input	O	O																																				
DI1	SC1, SC5, ...SC77	DI2	SC2, SC6, ...SC76																																						
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PIN FUNCTIONAL DESCRIPTION (continued)

Pin (No.)	Input Output	Description	Interface																														
EO, EI (84, 88)	input output	<p>Input/Output for Chip Select.</p> <ol style="list-style-type: none"> EO becomes low by (CLK1, CLK2) timing. When "HIGH" data is input to EI, the device becomes select mode and reads input data at CLK2 falling timing. Synchronized at the fall of CLK2. Input data is shifted. After reading 80 input data (equivalent to 80 CLK2 clock cycle in the serial mode or 20 CLK2 clock cycles in the 4 bit parallel mode), EO automatically becomes HIGH level and data reading is complete. EO is reset 1.5 cycles later. When two or more devices are used in the chip select mode, EO of each stage is connected to EI of the next stage. <ol style="list-style-type: none"> EO of all device connected is reset and device becomes non-select state and waits for EI input after the previous 1). When "HIGH" level is input to the first EI in the cascade connection, the first device performs the operations in 2) and 3). When EI of the second device is connected to DO of the first device, the second device perform the operations 2) and 3) after the first device. This operation is repeated in the same method subsequently 	controller or KS0083/84																														
M(85)	input	<p>LCD waveform AC conversion signal input</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Latch data</th> <th>M</th> <th>SC</th> <th>Latch data</th> <th>M</th> <th>SC</th> </tr> </thead> <tbody> <tr> <td>L (non-select)</td> <td>L</td> <td>V₃</td> <td>L (non-select)</td> <td>L</td> <td>V₃</td> </tr> <tr> <td>H (select)</td> <td>H</td> <td>V₄</td> <td>H (select)</td> <td>H</td> <td>V₄</td> </tr> <tr> <td></td> <td>L</td> <td>GND</td> <td></td> <td>L</td> <td>V_{EE}</td> </tr> <tr> <td></td> <td>H</td> <td>V_{EE}</td> <td></td> <td>H</td> <td>GND</td> </tr> </tbody> </table> <p style="text-align: center;">(segment signal drive mode) (common signal drive mode)</p>	Latch data	M	SC	Latch data	M	SC	L (non-select)	L	V ₃	L (non-select)	L	V ₃	H (select)	H	V ₄	H (select)	H	V ₄		L	GND		L	V _{EE}		H	V _{EE}		H	GND	controller
Latch data	M	SC	Latch data	M	SC																												
L (non-select)	L	V ₃	L (non-select)	L	V ₃																												
H (select)	H	V ₄	H (select)	H	V ₄																												
	L	GND		L	V _{EE}																												
	H	V _{EE}		H	GND																												
CLK1(87)	input	Clock pulse input terminal for data latch	controller																														
CLK2(96)	input	Clock pulse input terminal for data shift	controller																														
DI1-DI4(91-94)	input	<p>Display data input from the LCD controller LSI.</p> <p>In case of the common driver mode or serial input mode, supply the input data to DI1 and DI2-DI4 have to be set to VSS level or VDD level.</p>	controller																														
DO(89)	output	DO is high level in the chip select mode	KS0083/84																														
NC		No Connection	nc																														

MAXIMUM ABSOLUTE LIMIT (T_a=25°C)

Characteristic		Symbol	Value	Unit
Supply voltage	Logic	V _{DD}	-7 to +0.3	V
	LCD drivers	V _{LCD}	-30 to +0.3	
Input voltage		V _{IN}	V _{DD} -0.3 to +0.3	
Operating temperature		T _{opr}	-20 to +70	°C
Storage temperature		T _{stg}	-55 to +150	

* Voltage greater than above may damage to the circuit.

Maximum absolute limits are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device beyond them is not implied. Long exposure to these conditions may affect device reliability.

DC CHARACTERISTICS (V_{DD} = -5V ± 10%, V_{SS} = 0V, V_{EE} = -24V ± 3V, T_a = 25°C)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit
Power supply current		I _{DD}	1 bit serial (3.3MHz)			5.0	mA
			4 bit parallel (2.0MHz)			10.0	mA
Input Voltage	High	V _{IH}	—	0.2V _{DD}			V
	Low	V _{IL}	—			0.8V _{DD}	V
Output Voltage	High	V _{OH}	I _{OH} = -0.4mA	-0.4			V
	Low	V _{OL}	I _{OL} = 0.4mA			V _{DD} + 0.4	V
Voltage descending (Vi-SCi)		V _{D1}	I _{ON} = 1mA for one of SCi			1.0	V
		V _{D2}	I _{ON} = 0.08mA for each SCi			1.5	V
Leakage Current	Input	I _{LI}	—			1.0	μA
	Output	I _{LO}	—			10.0	μA

AC CHARACTERISTICS

($V_{DD} = -5V \pm 10\%$, $V_{SS} = 0V$, $V_{EE} = -24V \pm 3V$; $T_a = +25^\circ C$)

(1) Segment driver1; 1 bit serial data input (PS=LOW, FCS=LOW)

(refer to: fig. 3)

Characteristic	Symbol	Test condition	Min	Max	Unit
Clock cycle time	t_c		300		ns
Clock pulse width	High level	t_{WH}	130		
	Low level	t_{WL}	130		
Set up time D before CLK2↓	t_{SU}		70		
Hold time D after CLK2↓	t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)	t_{c1}		20		
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓)	t_{c2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)	t_{c3}		20		
Clock rise/fall time	t_r, t_f			50	
Output Delay	t_D	$C_L = 15pF$		230	
High level latch clock width	t_{CWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"	t_{OV}		130		

(2) segment driver: 4 bit data input (PS=High, FCS=LOW)

(refer to: fig 4.)

Characteristic	Symbol	Test condition	Min	Max	Unit
Clock cycle time	t_c		500		ns
Clock pulse width	High level	t_{WH}	230		
	Low level	t_{WL}	230		
Set-up time D before CLK2↓	t_{SU}		70		
Hold time D after CLK2↓	t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)	t_{c1}		20		
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓)	t_{c2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)	t_{c3}		20		
Clock rise/fall time	t_r, t_f			50	
Output Delay	t_D	$C_L = 15pF$		230	
High level latch clock width	t_{LWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"	t_{OV}		130		

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(3) Common Driver (PS=HIGH, FCS=HIGH)

(refer to: fig 5)

Characteristic	Symbol	Test condition	Min	Max	Unit
Clock cycle time	t_c		1000		ns
Clock pulse width	High level	t_{WH}	130		
	Low level	t_{WL}	830		
Set-up time D before CLK↓	t_{SU}		70		
Hold time D after CLK↓	t_h		50		
Output Delay	t_D	CL=15pF		500	
Clock rise/fall time	t_r, t_f			50	

(4) segment driver 2; 1 bit serial data input (PS=LOW, FCS=HIGH)

(refer to: fig 6)

Characteristic	Symbol	Test condition	Min	Max	Unit
Clock cycle time	t_c		380		ns
Clock pulse width	High level	t_{WH}	170		
	Low level	t_{WL}			
Set-up time D before CLK↑	t_{SU}		70		
Hold time D after CLK↑	t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)	t_{c1}		20		
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↑)	t_{c2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)	t_{c3}		20		
Clock rise/fall time	t_r, t_f			50	
Output delay	t_D	CL=15pF		230	
High level latch clock with	t_{LWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"	t_{ov}		130		

note (Input frequency, I/O reference level; 0.8 V_{DD}, 0.2 V_{DD})

- 1: Valid time (internal shift register)
 2: $(t_c \times 1.5) - (t_{c1}) - (t_{c3}) - (t_r \times 3)$

TIMING DIAGRAM

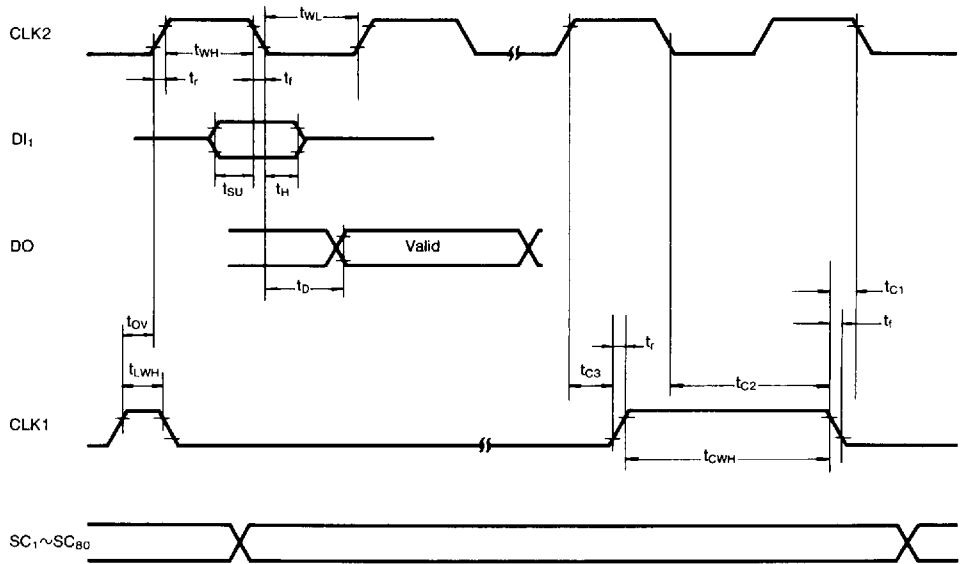


Fig. 3 Segment driver (1 bit serial input)

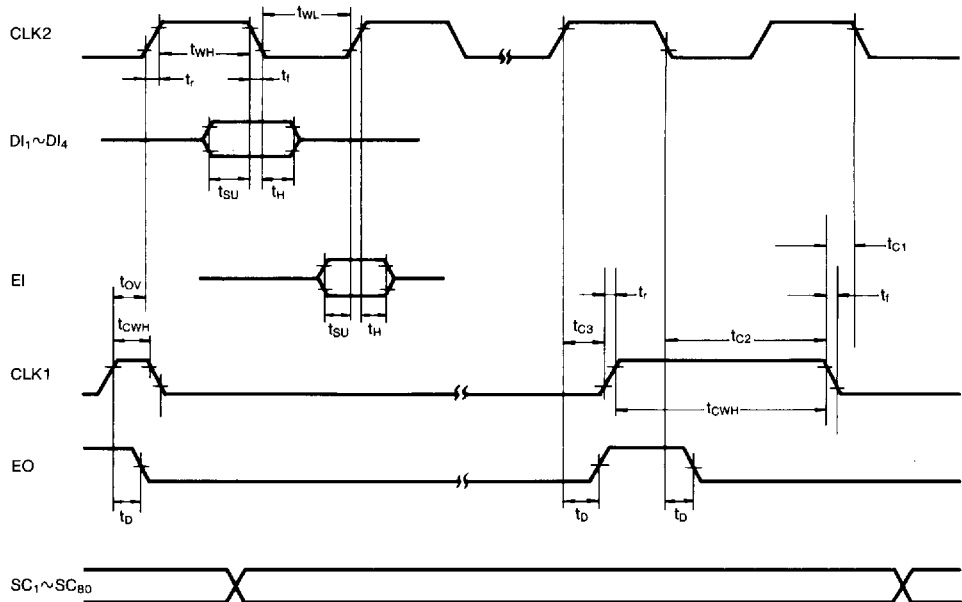


Fig. 4. 4-bit input segment driver

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TIMING DIAGRAMS (Continued)

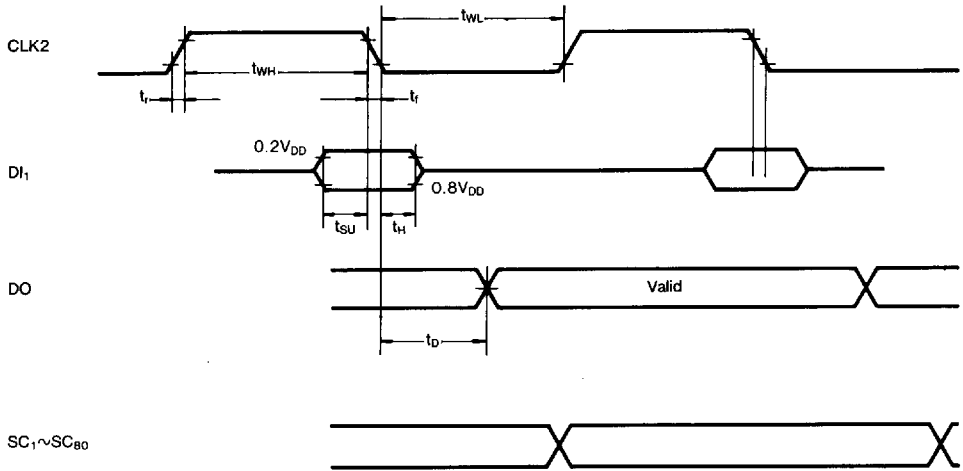


Fig. 5. Common driver

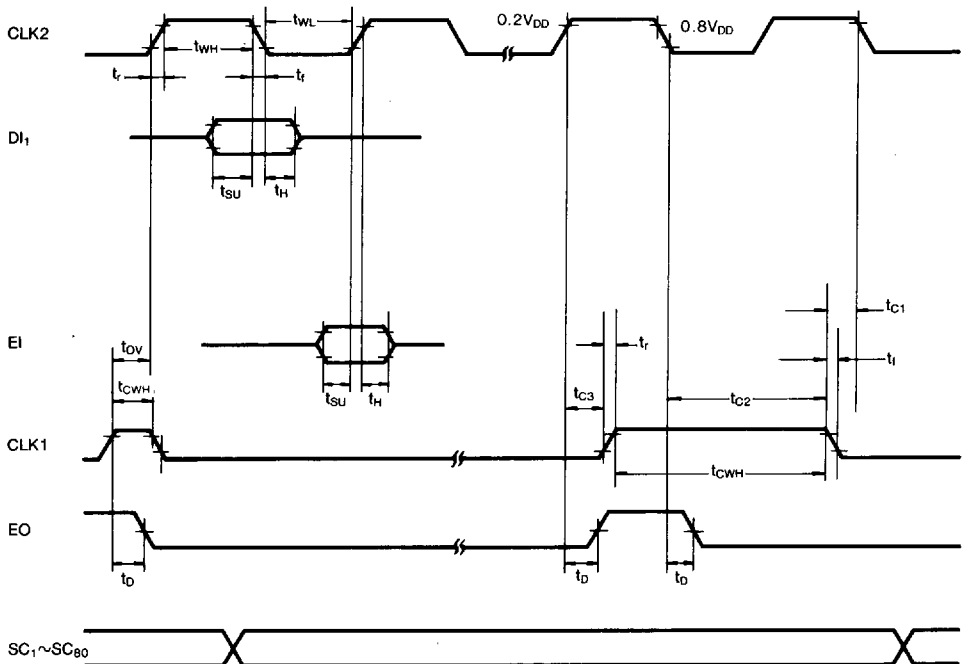


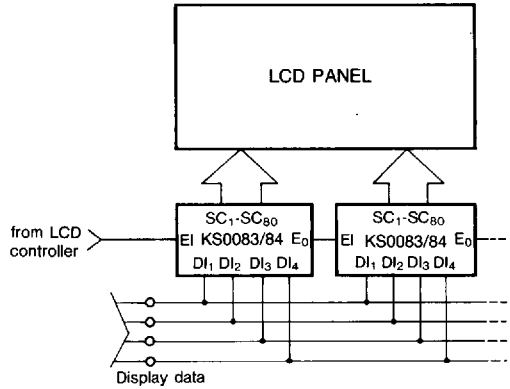
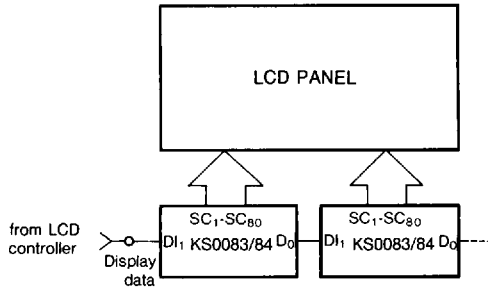
Fig. 6. Segment driver (1 bit serial data input)

APPLICATION CIRCUIT .

Mode Select

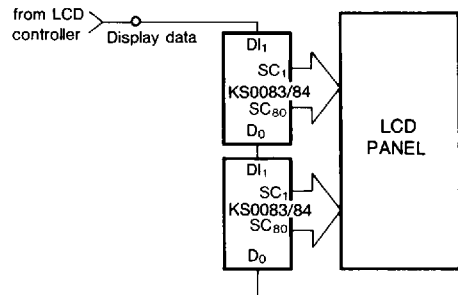
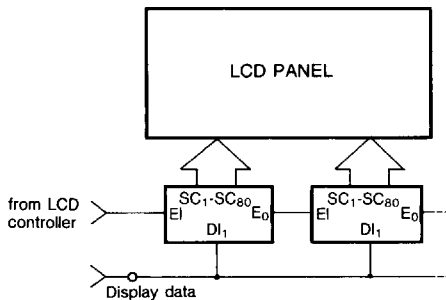
1. segment driver 1; 1 bit serial data input (FCS=L, PS=L)

2. segment driver; 4 bit data input (FCS=L, PS=H)



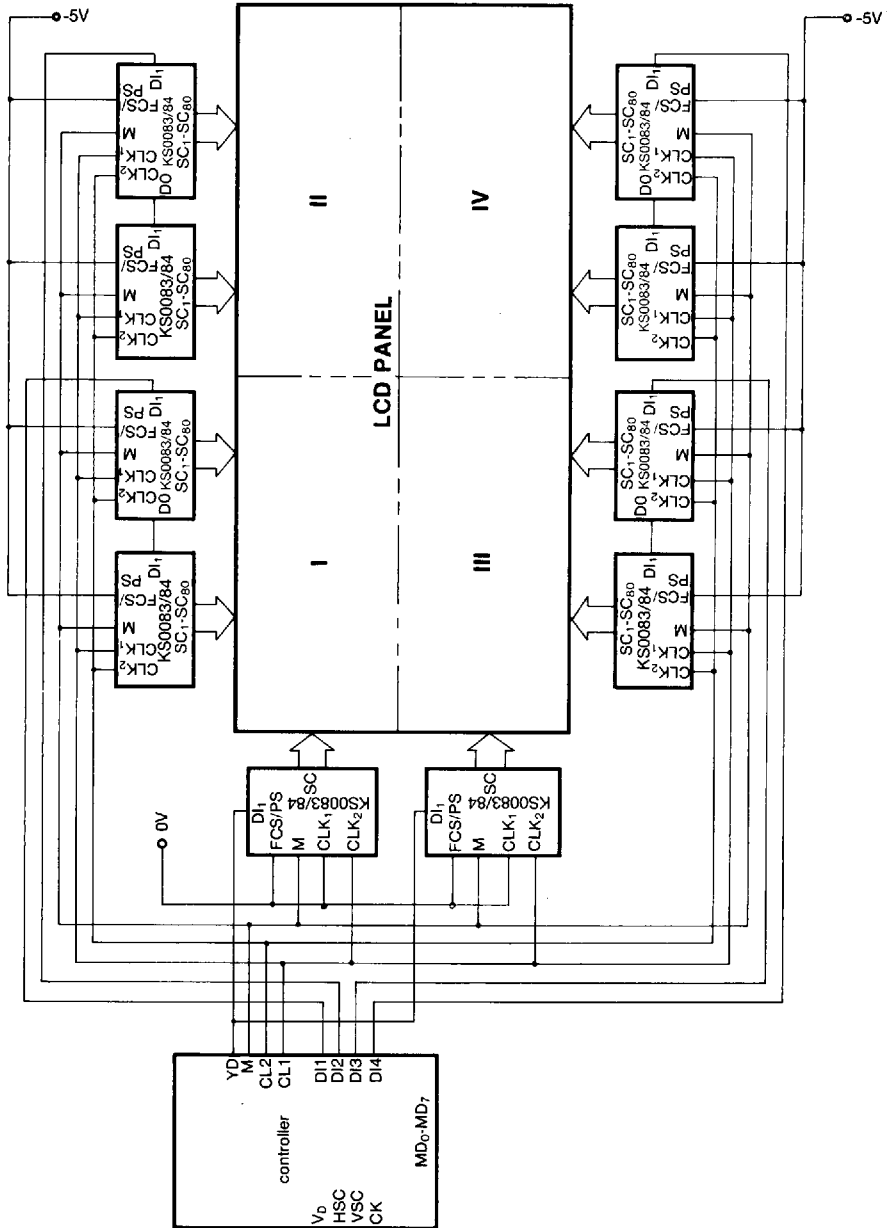
3. segment driver 2; 1 bit serial data input (FCS=H, PS=L)

4. common driver (FCS=H, PS=H)



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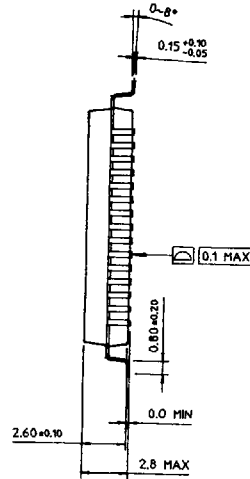
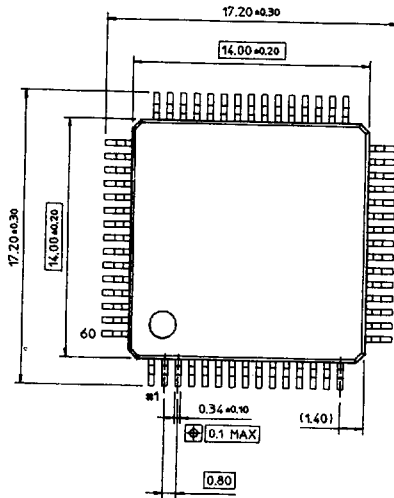
APPLICATION CIRCUIT



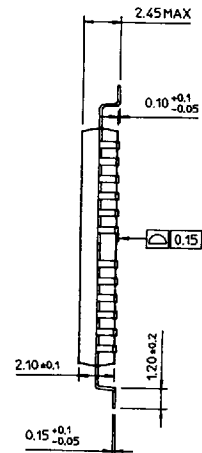
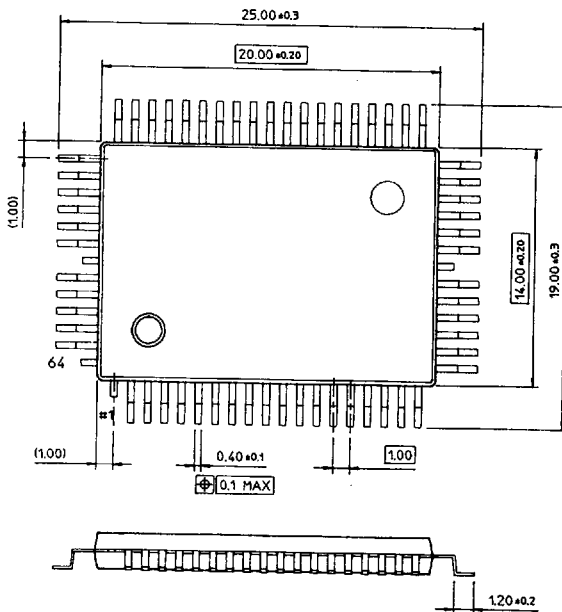
PACKAGE DIMENSIONS

Dimensions in Millimeters

60-QFP-1414A



64-QFP-1420D



SAMSUNG

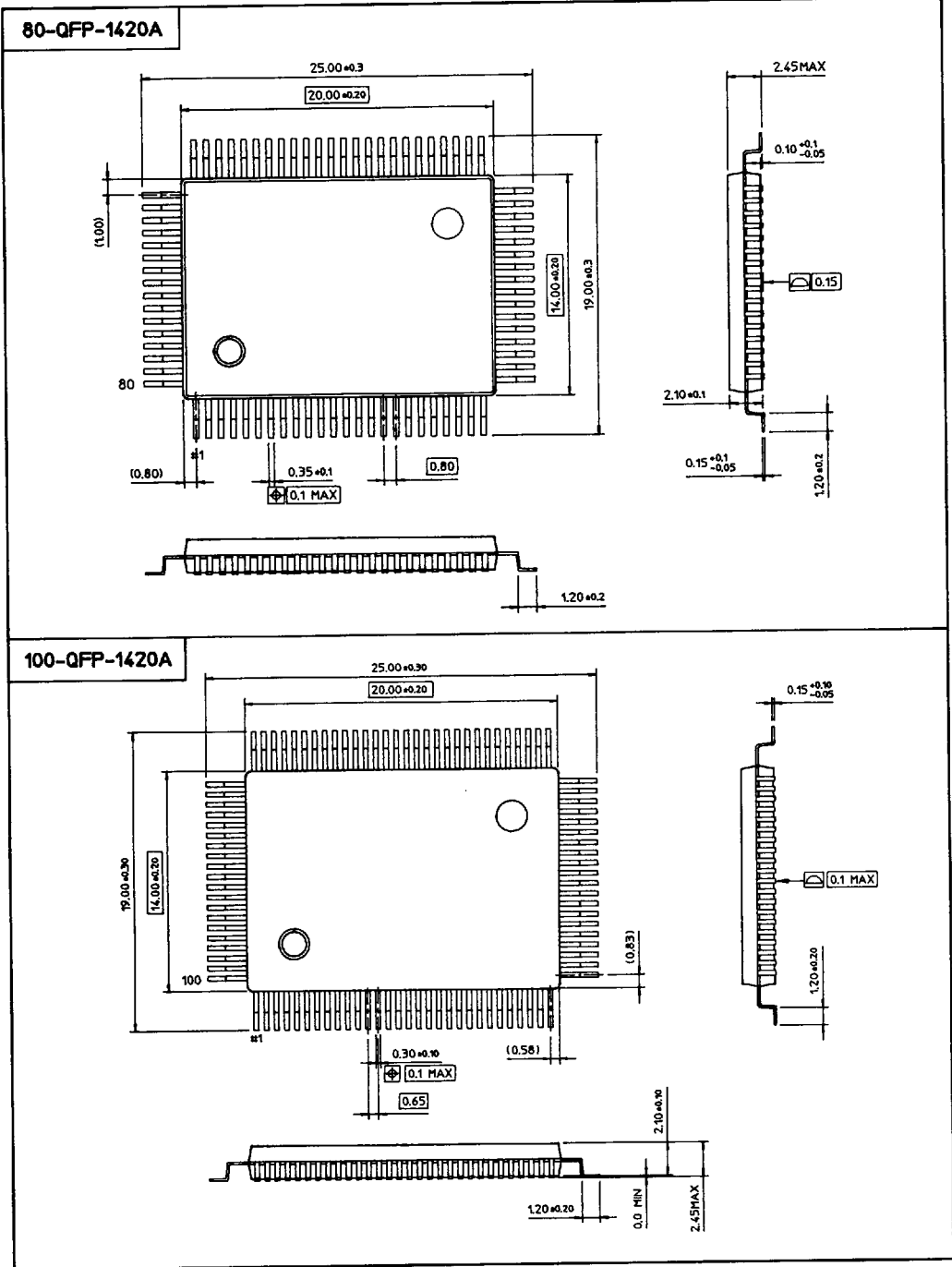
ELECTRONICS

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7964142 0022066 667

PACKAGE DIMENSIONS

Dimensions in Millimeters

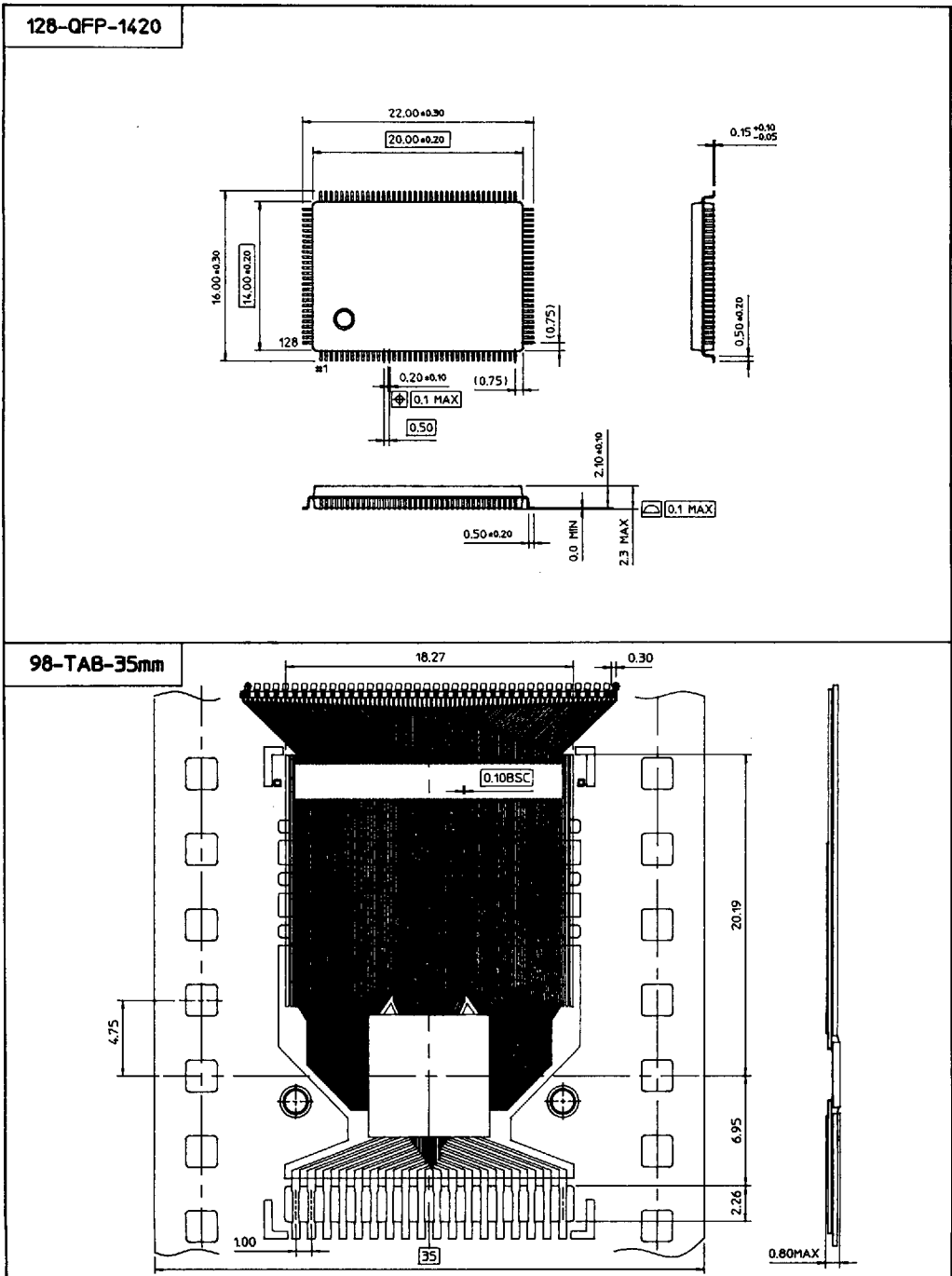


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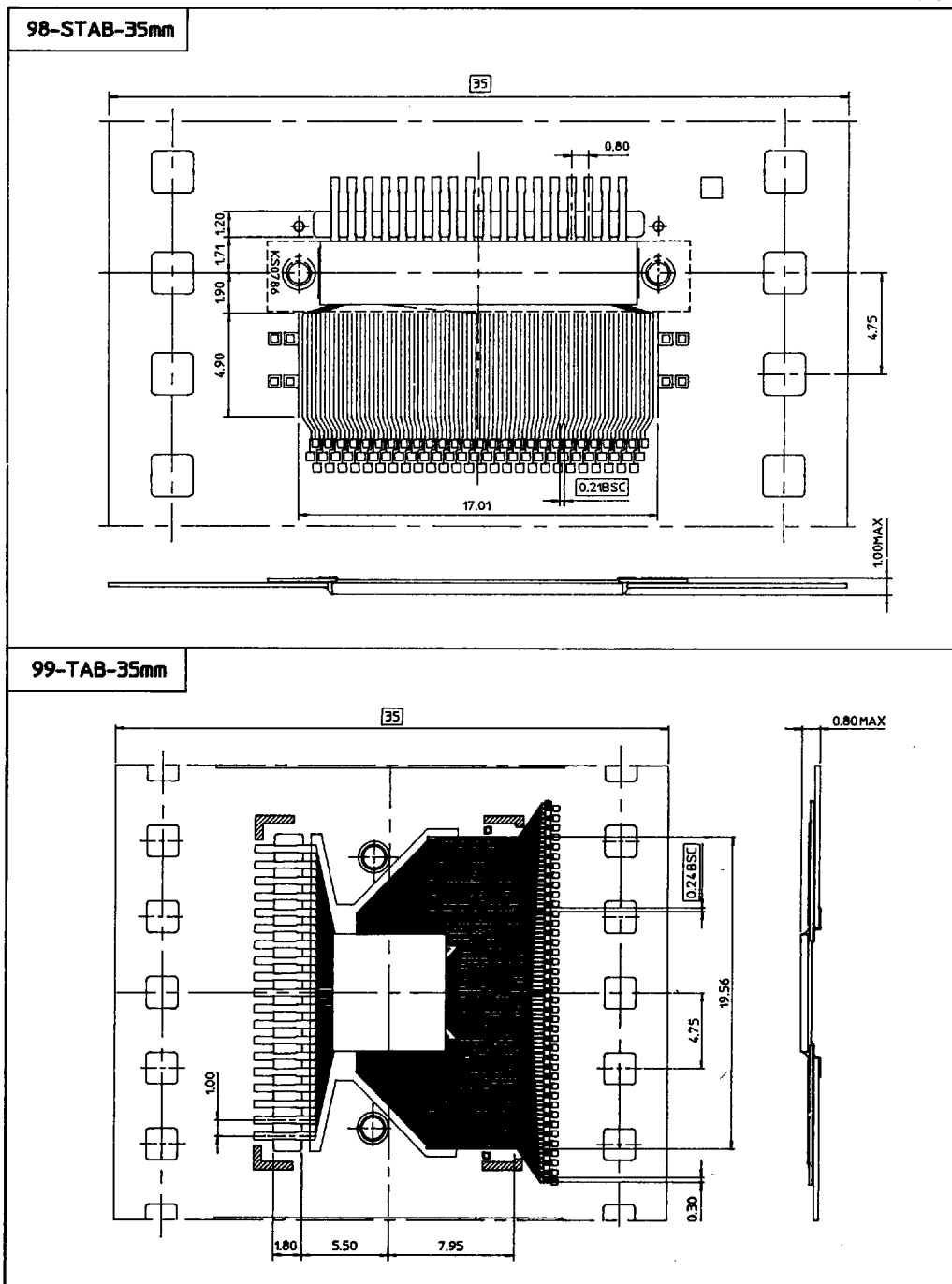
Dimensions in Millimeters



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PACKAGE DIMENSIONS

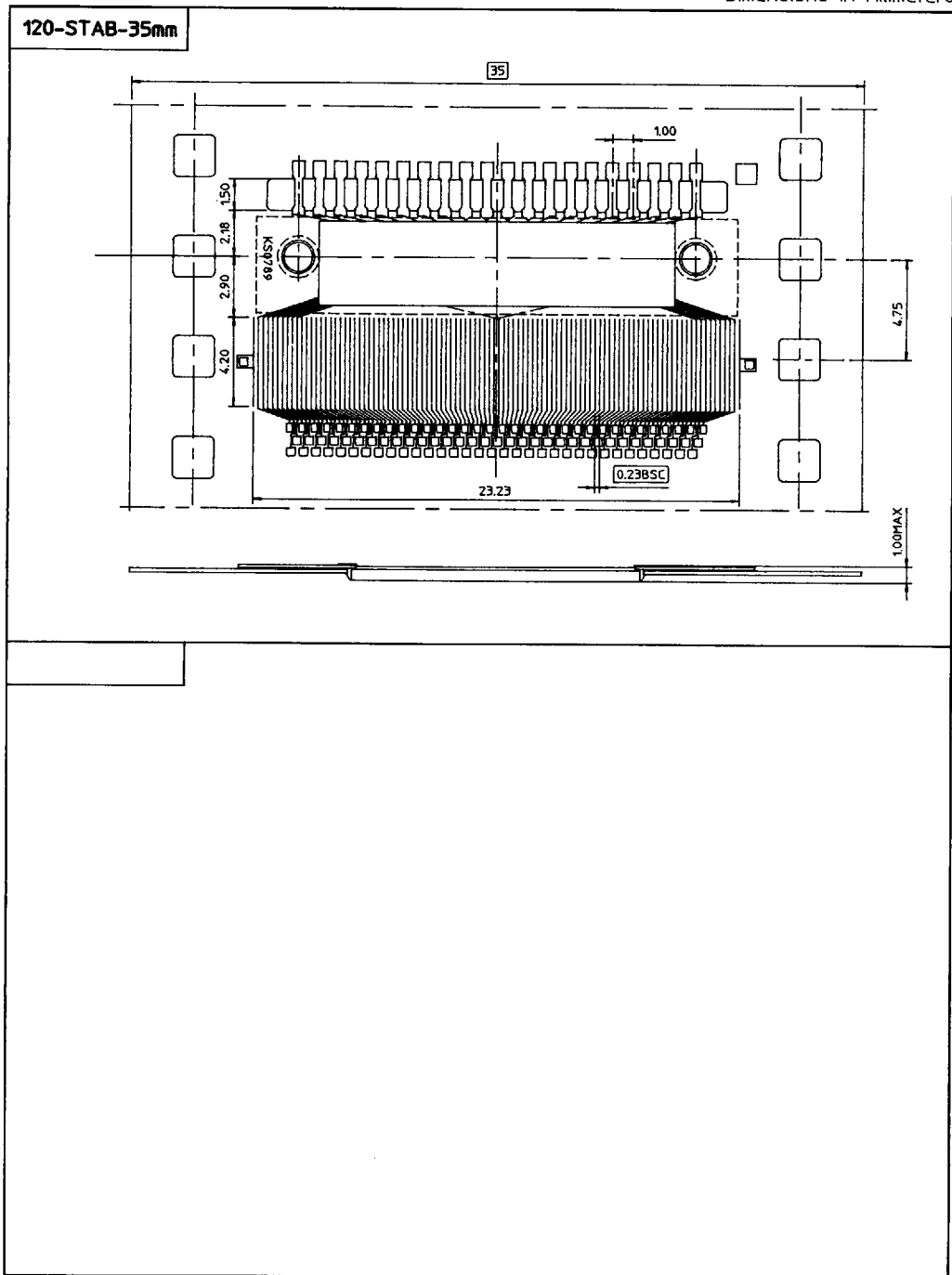
Dimensions in Millimeters



ELECTRONICS

PACKAGE DIMENSIONS

Dimensions in Millimeters



3