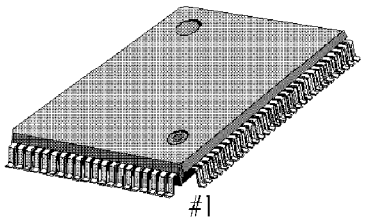
INTRODUCTION

The KS0104 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of 80 bit bidirectional shift register, 80 bit data latch and 80 bit driver

100 QFP



FUNCTION

- Dot matrix LCD segment driver with 80 channel output
- Input/Output signal
  - Input : 4 bit parallel display data, control pulse from controller and bias voltage (V_1,V_3, V_4, V_{EE})
  - Output ; 80 channel waveform for LCD driving.
- Power down function to make power consumption low.

FEATURES

- Power supply voltage : + 5V ± 10%
- Supply voltage for display : 8 ~ 28V (V_{DD} - V_{EE})
- Parallel data processing (4 bit)
- Applicable LCD duty : 1/64 ~ 1/256
- Interface

Driver	
COMMON	SEG (cascade)
KS0083/84/86, KS0103	Other KS0104/B

- High voltage CMOS process
- 100 QFP and bare chip available.

BLOCK DIAGRAM

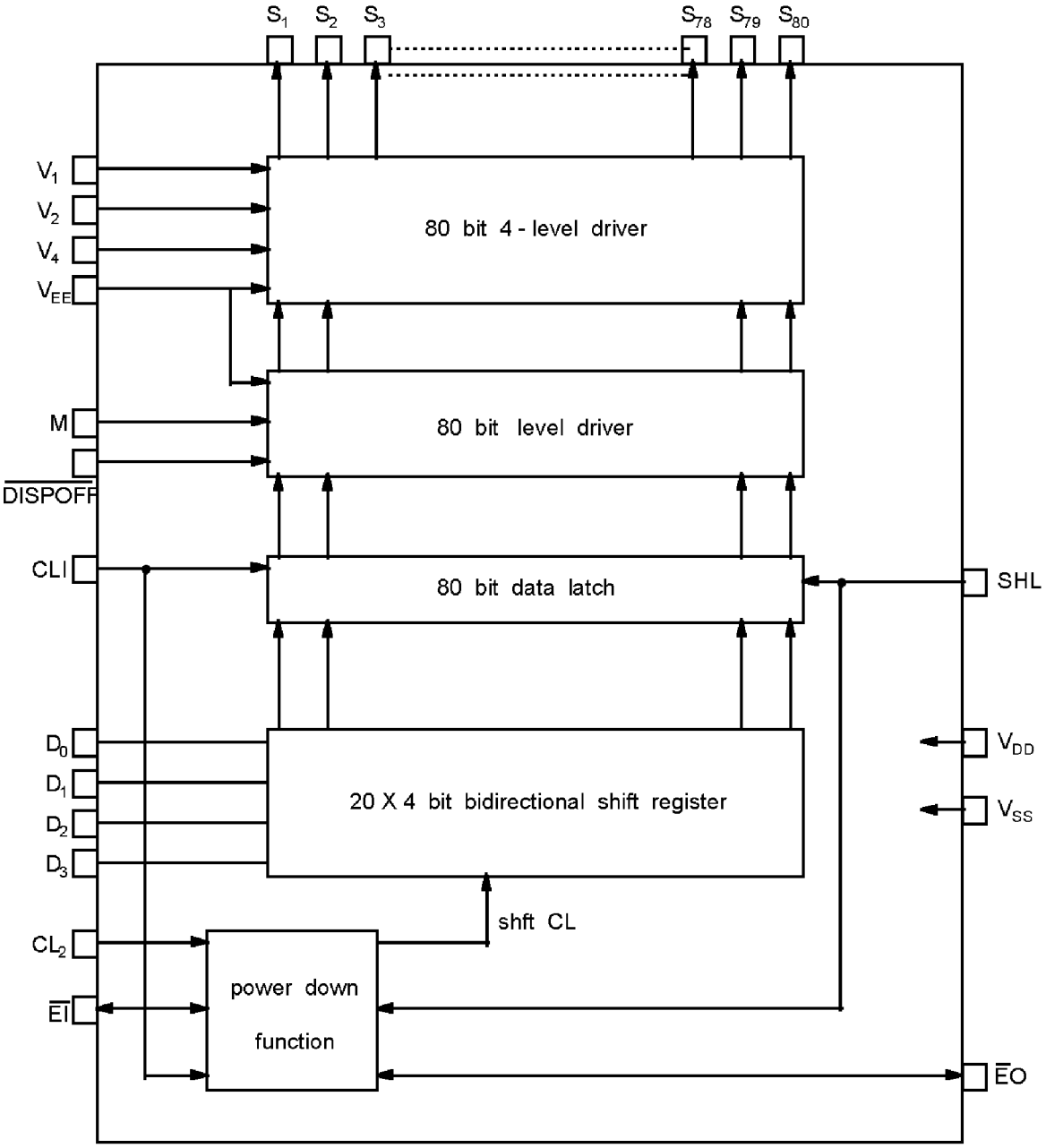


Fig 1. KS0104 Function block diagram

PIN CONFIGURATION

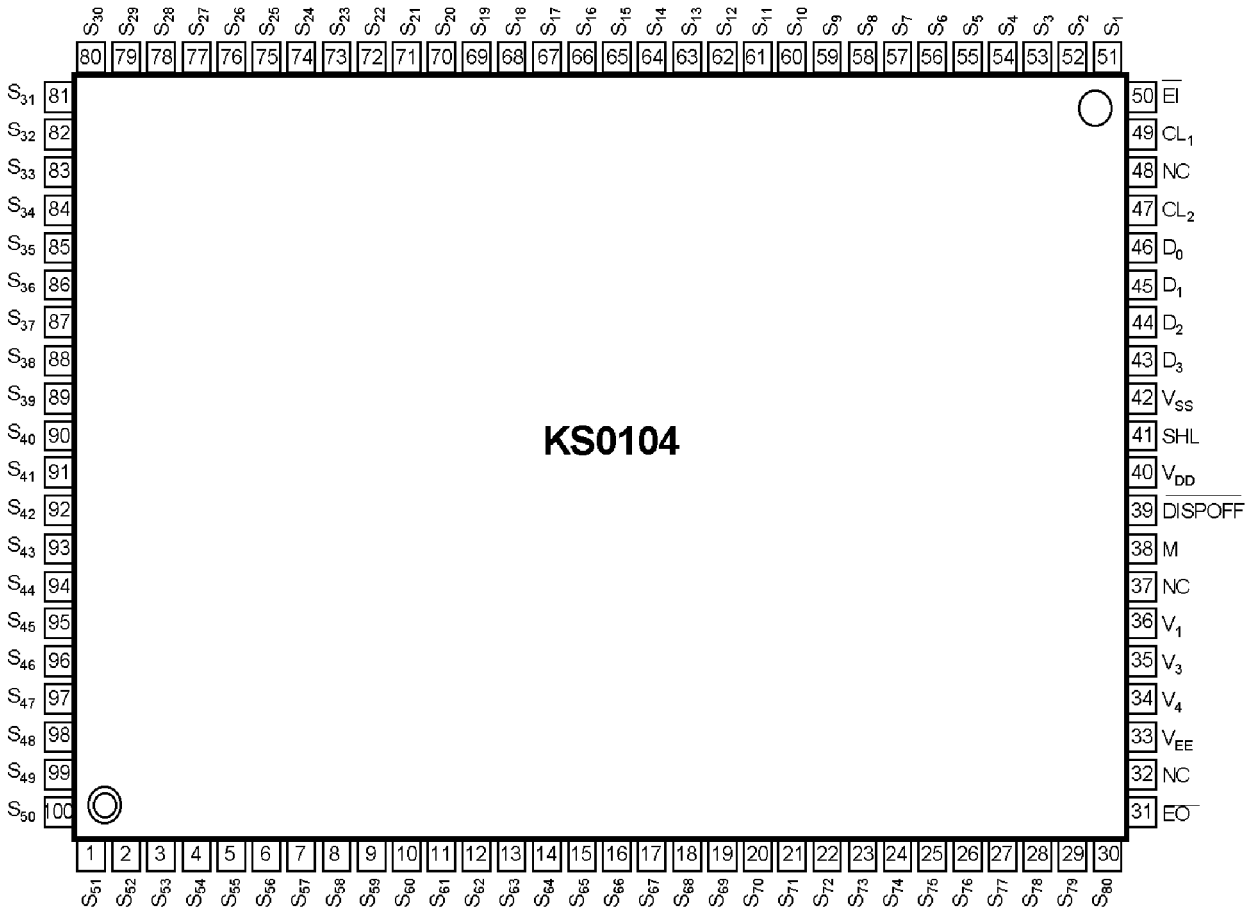
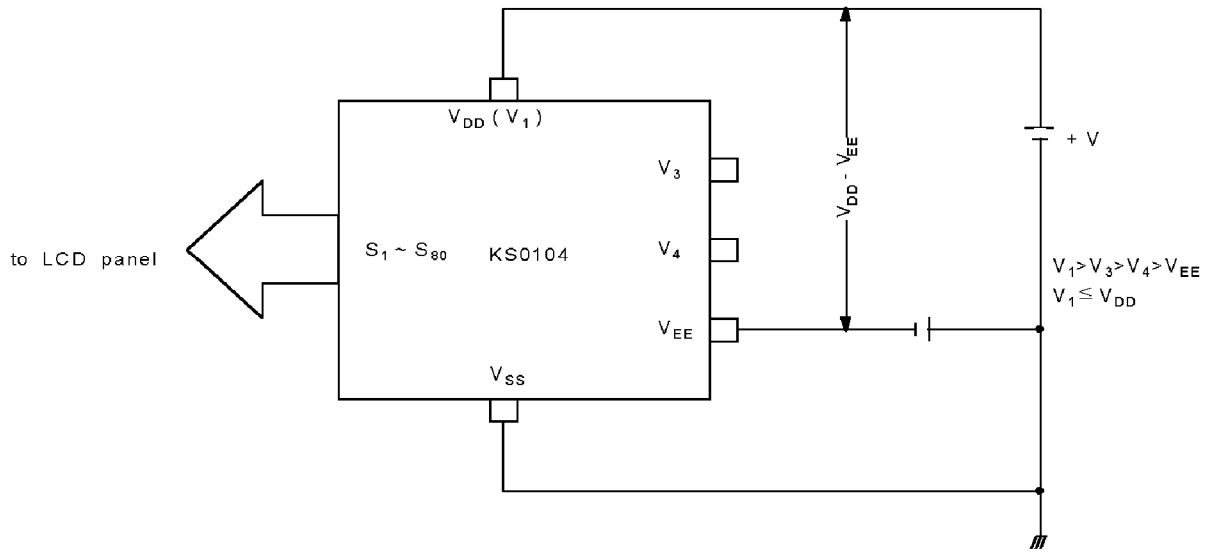


Fig. 2. 100 QFP Top View

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3~6.0	V
Driver Supply Voltage	V_{LCD}	0~30	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Operating Temperature	T_{OPR}	-30~+85	℃
Storage Temperature	T_{STG}	-55~+150	℃

* Voltage greater than above may result in damage to the circuit.



ELECTERICAL CHARACTERISTICS

DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Ta=-30 ~ +85℃, C_L=15pF)

Characteristics	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-		4.5	-	5.5	V
Driver Supply Voltage	V_{DD}-V_{EE}	-		8	-	28	V
Input Voltage (*1)	V_{IH}	-		0.8V_{DD}	-	-	V
	V_{IL}	-		-	-	0.2V_{DD}	V
Input Current (*1)	I_{IH}	V_{IH}=V_{DD}, V_{DD}=5.5V		-	-	1	μA
	I_{IL}	V_{IH}=0V, V_{DD}=5.5V		-	-	-1	μA
Output Voltage (*2)	V_{OH}	I_O=-0.2mA, V_{DD}=4.5V		V_{DD}-0.4	-	-	V
	V_{OL}	I_O=0.2mA, V_{DD}=4.5V		-	-	0.4	V
On Resistance(*3)	R_{ON}	V_{DD}-V_{EE}=23V, V_{DD}=4.5V (*4) | Vn-Vo | =0.25V		-	2	4	KΩ
Supply Current (*5)	I_{SBY}	CL2=1MHz V_{DD}=5.5V V_{DD}-V_{EE}=26V	Display data is not processing	-	-	200	μA
	I_{DD}		Display data is processing	-	-	3	mA
	I_V		Current on V_1, V_3, V_4 V_{EE} pins	-	-	±100	μA
Input Capacitance	Ci	f=1MHz		-	5	-	pF

*1; Applicable pin; $\overline{CL_1}$, $\overline{CL_2}$, $\overline{EI}$, $\overline{EO}$, D_0-D_3, SHL, $\overline{DISPOFF}$, M
*2; Applicable pin; $\overline{EI}$, $\overline{EO}$
*3; Applicable pin; S_1-S_{80}
*4; V_n=V_{DD}-V_{EE}, V_3=13/15 (V_{DD}-V_{EE}), V_4=2/15 (V_{DD}-V_{EE}), V_{DD}=V_1
*5; Display data 1010-M=40Hz.

AC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, T_a=-30 ~ +85℃, C_L=15pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock Frequency	f_{CL}	Duty=50%	3.4	-	-	MHz
Clock Pulse Width	t_W	-	100	-	-	ns
Clock Rise/Fall Time	t_R,t_F	-	-	-	50	
Data Set-up Time	t_{SU}	-	50	-	-	
Data Hold Time	t_{DH}	-	80	-	-	
Clock-CL_1 Time	t_{KCL}	-	200	-	-	
CL_1 Set-up Time	t_{CSU}	-	90	-	-	
CL_1-Clock Time	t_{CLK}	-	200	-	-	
Propagation Delay Time	t_{PD}	$\overline{EO}$ Output	-	-	224	
		$\overline{EI}$ Output			224	
$\overline{EO}$, $\overline{EI}$ Set-up Time	t_{PSU}	$\overline{EO}$ Input	70	-	-	
		$\overline{EI}$ Input	70			

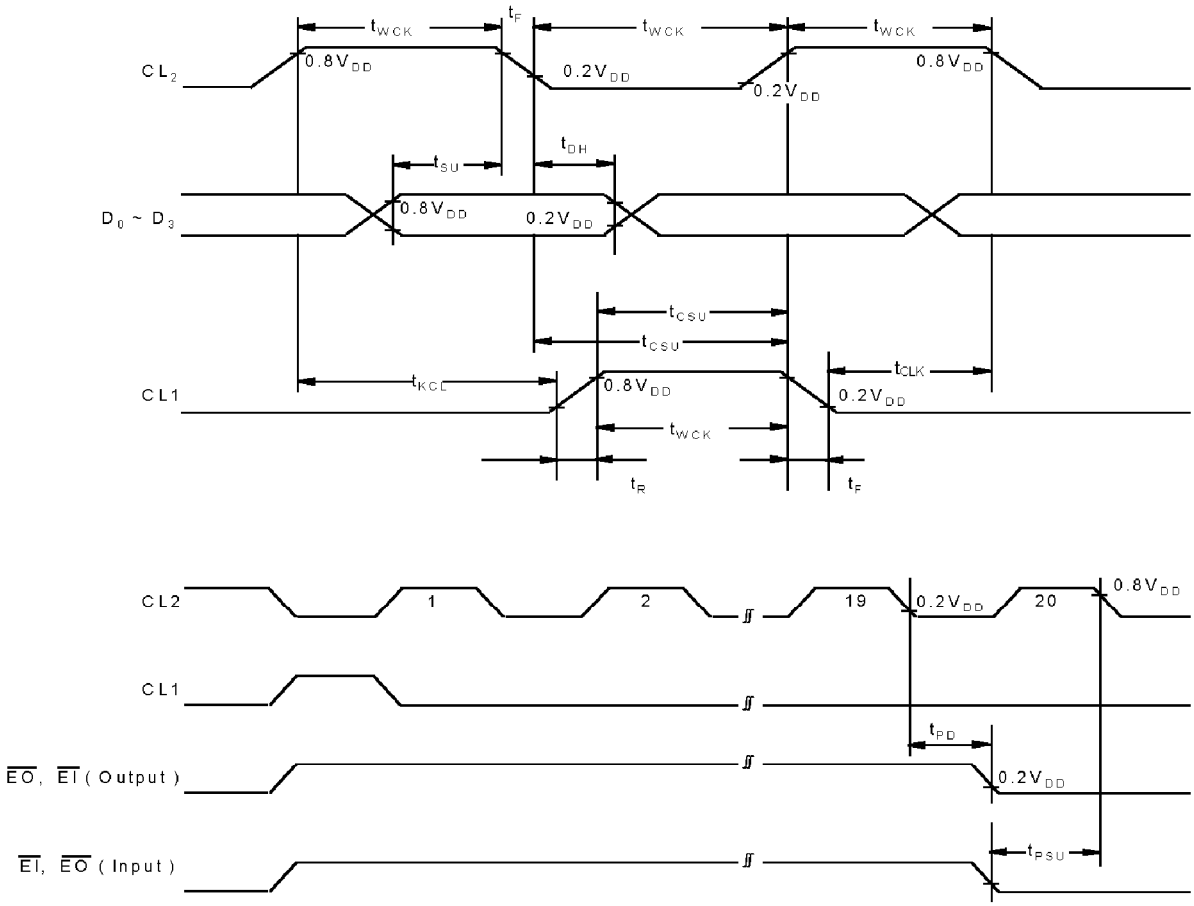


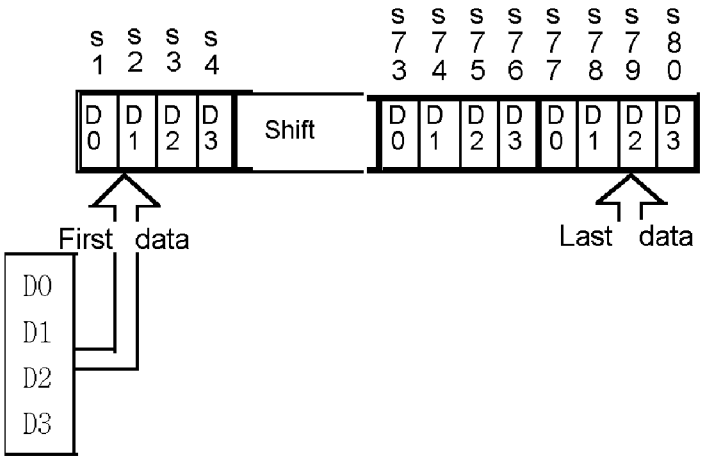
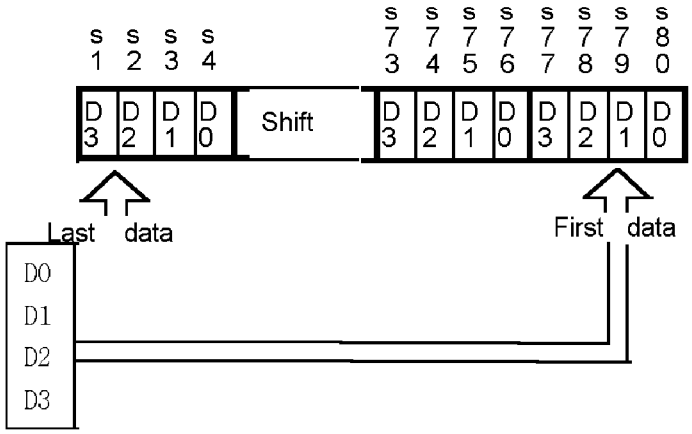
Fig. 3. Timing characteristic

PIN DESCRIPTION

PIN (No)	INPUT OUTPUT	NAME	DESCRIPTION	INTERFACE
V_{DD}(40)	Power	Operating Voltage	For logical circuit (+5V±10%)	Power Supply
V_{SS}(42)			0V (GND)	
V_{EE}(33)		Negative Supply Voltage	For LCD drive circuit	
V_1, V_3 V_4 (34-36)	Input	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divded by the resistance is usually used as supply voltage source. (refer to note 1)	Power
S_1~S_{80} (1-30, 51-100)	Output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to note 2)	LCD
CL_2 (47)	Input	Data shift clock	Clock pulse input for the 4 bit parallel shift register. The data is shifted to 80 bit shift register at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.	Controller
M(38)	Input	Alternate signal for LCD driver output	Alternate signal input pin for LCD driving Normal frame inversion signal is input.	Controller
CL_1(49)	Input	Data latch clock	The signal for latching the shift register contents is input to this terminal. CL1 pulse "H" level initializes ENABLE F/F	Controller
$\overline{DISPOF}$ (39)	Input	Output level control	Control input pin for display data output level (S_1~S_{80}). V_1 level is output from S_1~S_{80} terminal during "L" level input. LCD becomes non-selected by V_1 level output from every output of segment drivers and every output of common drivers.	Controller
SHL(41)	Input	Data interface	EO and EI can be used as either input terminal or output terminal according to the condition of SHL. The shifting direction of each data, D_0~D_3, the I/O condition of EO and EI, and the condition of SHL are described in the table below. (refer to note 3)	
$\overline{EO}$,$\overline{EI}$ (31,50)	Input Output			

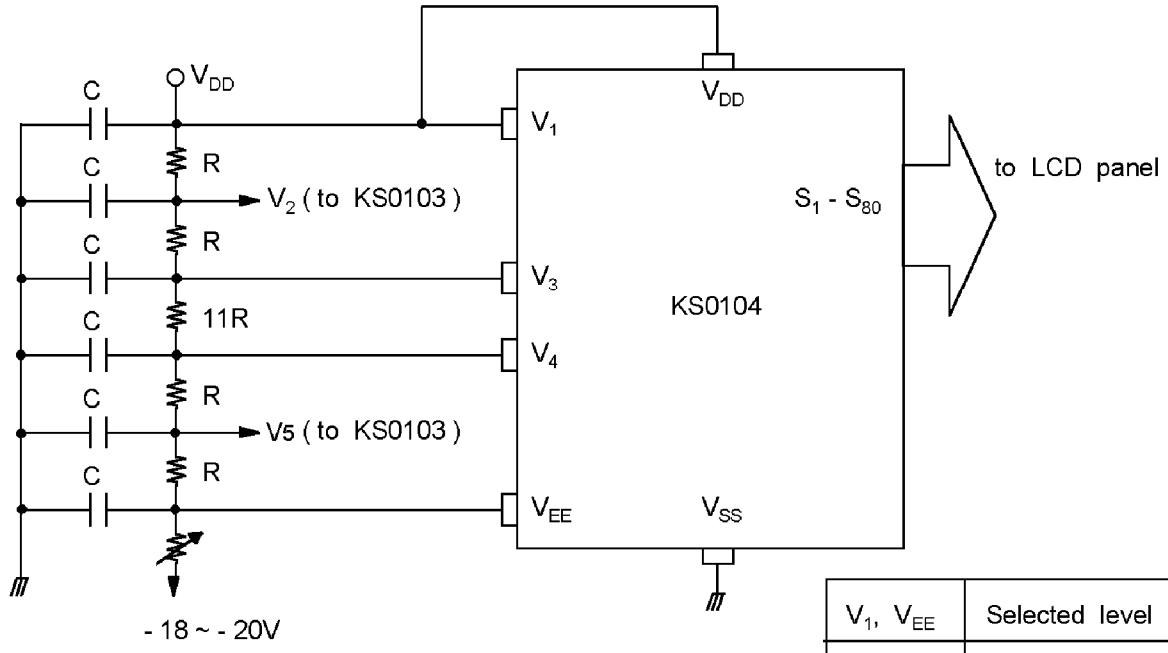
Pin	I/O	SHL	Display data shift direction	Description
$\overline{EO}$	Input	L	D_0; $S_1 \rightarrow S_5 \rightarrow S_{77}$ D_1; $S_2 \rightarrow S_6 \rightarrow S_{78}$ D_2; $S_3 \rightarrow S_7 \rightarrow S_{79}$ D_3; $S_4 \rightarrow S_8 \rightarrow S_{80}$	Input terminal to ENABLE F/F of KS0104
$\overline{ET}$	Output			Output terminal of ENABLE F/F. $\overline{EI}$ is connected to next KS0104's $\overline{EO}$ when the KS0104's are connected in series (cascade connection)
$\overline{ET}$	Input	H	D_0; $S_{80} \rightarrow S_{76} \rightarrow S_4$ D_1; $S_{79} \rightarrow S_{75} \rightarrow S_3$ D_2; $S_{78} \rightarrow S_{74} \rightarrow S_2$ D_3; $S_{77} \rightarrow S_{73} \rightarrow S_1$	Input terminal to ENABLE F/F of KS0104
$\overline{EO}$	Output			Output terminal of ENABLE F/F. $\overline{EO}$ is connected to next KS0104's $\overline{EI}$ when the KS0104's are connected in series (cascade connection)

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN
(No)</th><th>INPUT
OUTPUT</th><th>NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td rowspan="3">D_0~D_3
(43-46)</td><td rowspan="3">Input</td><td colspan="3"></td><td></td></tr>
<tr><td colspan="3">
<table>
<tr><th>PIN</th><th>I/O</th><th>SHL</th><th>Data direction</th></tr>
<tr><td>$\overline{EO}$</td><td>Input</td><td rowspan="2">L</td><td rowspan="2"> 
</td></tr>
<tr><td>$\overline{EI}$</td><td>Output</td></tr>
<tr><td>$\overline{EI}$</td><td>Input</td><td rowspan="2">H</td><td rowspan="2"> 
</td></tr>
<tr><td>$\overline{EO}$</td><td>Output</td></tr>
</table>
</td><td></td></tr>
<tr><td>Display data input</td><td colspan="2">Display data input pins for 4 bit paralle shift register and its is input synchronized with the clock pulse.
The combination of D_0~D_3 level, M signal, Display data output level and the display on the LCD panel is described on the table below.
($\overline{DISPOFF}$=H)
<table>
<tr><th>D_0~D_3</th><th>M</th><th>Display data output level</th><th>Display on the LCD</th></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>OFF</td></tr>
<tr><td>H</td><td>L</td><td>V_1</td><td>ON</td></tr>
<tr><td>L</td><td>H</td><td>V_4</td><td>OFF</td></tr>
<tr><td>H</td><td>H</td><td>V_{EE}</td><td>ON</td></tr>
</table></td><td>controller</td></tr>
</table>

***NOTE 1**

The below figure shows when the bias voltage is devided by the resistor (1/15 Bias, 1/200 Duty)



V_1, V_{EE}	Selected level
V_3, V_4	Nonselected level

***NOTE 2**

M	Latched data	$\overline{\text{DISPOFF}}$	Output level (S1-S80)
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	VEE
X	X	L	V1

X : Don't Care

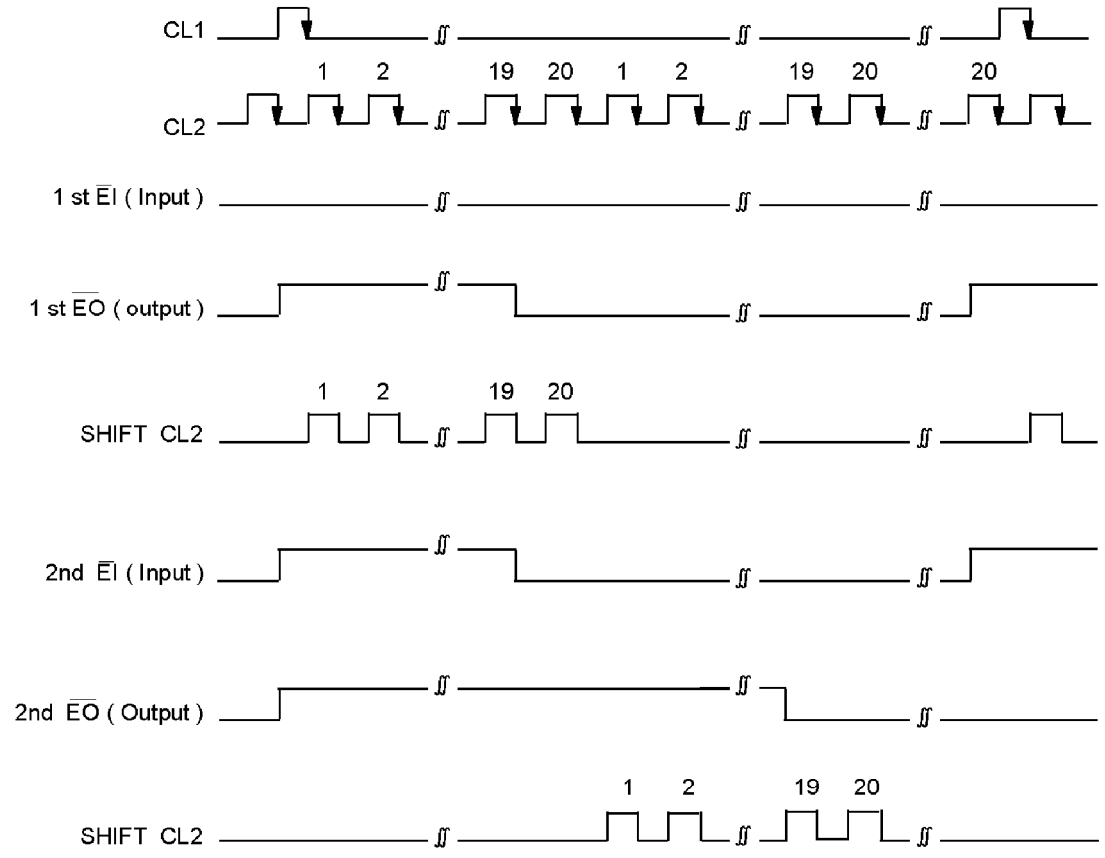
*NOTE 3

- $\overline{EO}$ and $\overline{EI}$ pins working as input terminals.
  ENABLE F/F stops Display Data in at "H" level input. ENABLE F/F starts Display data in at "L" level input.
- $\overline{EO}$ and $\overline{EI}$ pins working as output terminals.
  These terminals are set to the "H" level immediately after ENABLE F/F is intialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the CL2 terminal, these terminals are then set to the "L" level.
  The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected.
  (For cascade connection, refer to the application circuit drawing.)

POWER DOWN FUNCTION

In order to reduce the power consumption, in case of cascade connection, KS0104 has a "power down function."

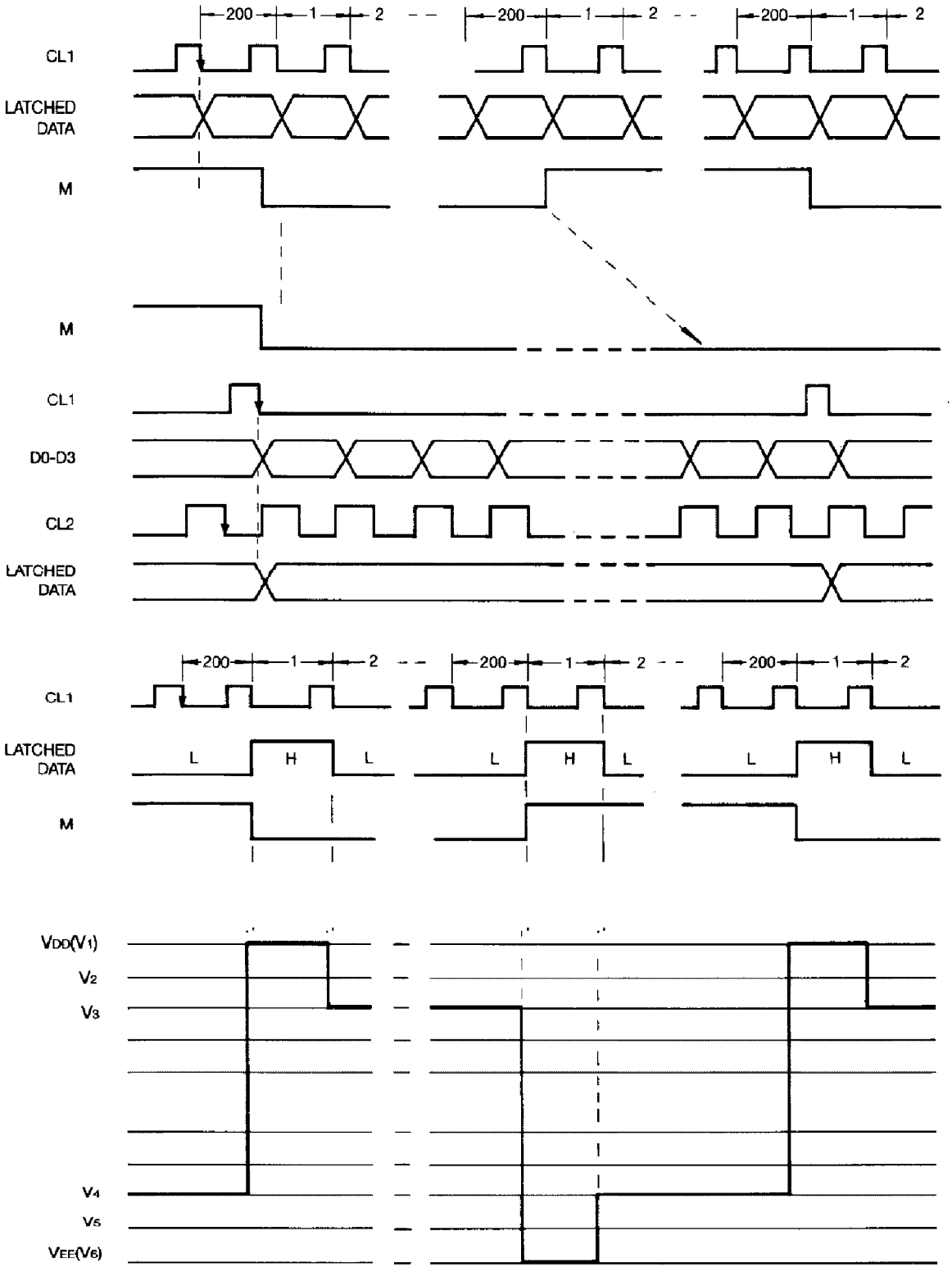
$\overline{EI}$	Enable input	Enable	L
		Disable	H
$\overline{EO}$	Enable output	$\overline{EO}$ of N th driver is connected to $\overline{EI}$ of (N+1)th driver KS0104	



SHL = "H" ($\overline{EI}$ = Input $\overline{EO}$ = Output)
First KS0104`s $\overline{EO}$ should be connected to second KS0104`s EI.

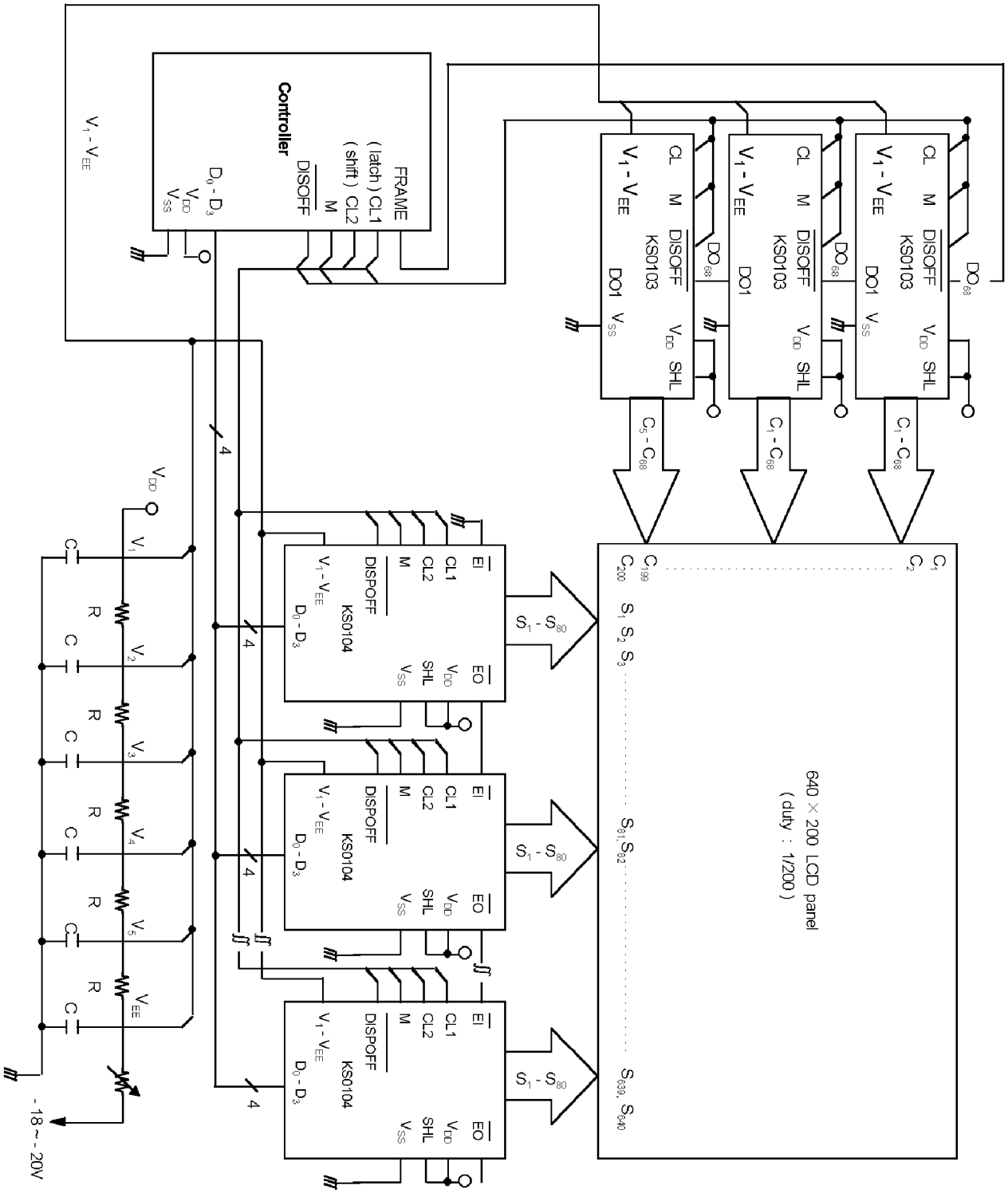
Fig 4. Timing Characteristics. (cascade connection)

Timing Chart - 1/200 Duty, 1/15 Bias

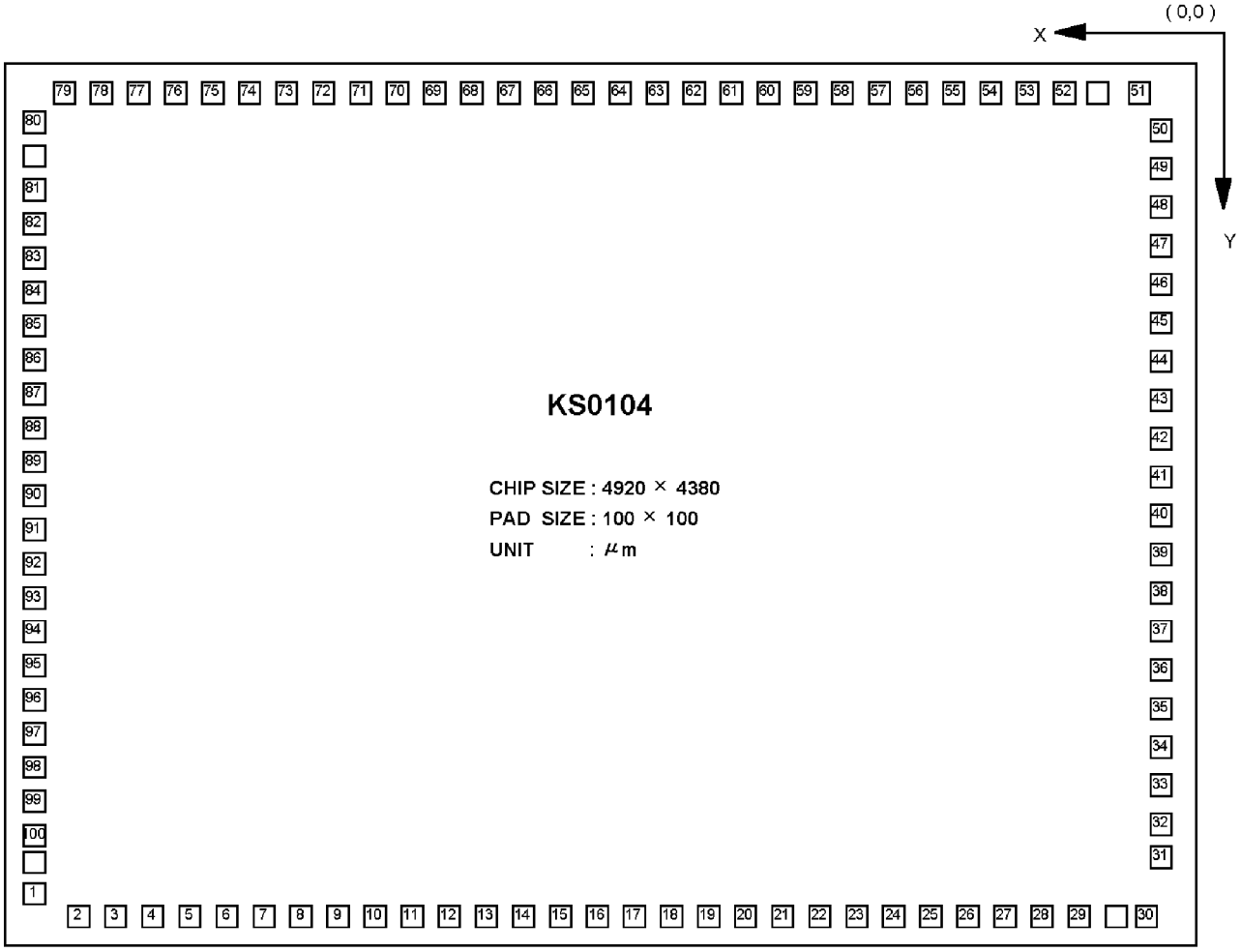


V1=VDD
V2=VDD-1/15 VLCD
V3=VDD-2/15 VLCD
V4=VDD-13/15 VLCD
V5=VDD-14/15 VLCD
VLCD=VDD-VEE

APPLICATION CIRCUIT



PAD DIAGRAM



PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
*	NC	4788	3838.5	34	V4	130	3419	68	S18	2913	135
1	S51	4788	4091	35	V3	130	3230.5	69	S19	3063	135
2	S52	4563	4248	36	V1	130	3042	70	S20	3213	135
3	S53	4413	4248	37	NC	*	*	71	S21	3363	135
4	S54	4263	4248	38	M	130	2808	72	S22	3513	135
5	S55	4113	4248	39	$\overline{DISPOFF}$	130	2573	73	S23	3663	135
6	S56	3963	4248	40	VDD	130	2383	74	S24	3813	135
7	S57	3813	4248	41	SHL	130	2158.5	75	S25	3963	135
8	S58	3663	4248	42	VSS	130	1971.5	76	S26	4113	135
9	S59	3513	4248	43	D3	130	1776.5	77	S27	4263	135
10	S60	3363	4248	44	D2	130	1541.5	78	S28	4413	135
11	S61	3213	4248	45	D1	130	1365	79	S29	4563	135
12	S62	3063	4248	46	D0	130	1130	80	S30	4788	292
13	S63	2913	4248	47	CL2	130	953.5	*	NC	4788	544.5
14	S64	2763	4248	48	NC	*	*	81	S31	4788	694.5
15	S65	2613	4248	49	CL1	130	718.5	82	S32	4788	844.5
16	S66	2463	4248	50	$\overline{EI}$	130	485.5	83	S33	4788	994.5
17	S67	2313	4248	51	S1	150	135	84	S34	4788	1144.5
18	S68	2163	4248	*	NC	363	135	85	S35	4788	1311.5
19	S69	2013	4248	52	S2	513	135	86	S36	4788	1471.5
20	S70	1863	4248	53	S3	663	135	87	S37	4788	1631.5
21	S71	1713	4248	54	S4	813	135	88	S38	4788	1791.5
22	S72	1563	4248	55	S5	963	135	89	S39	4788	1951.5
23	S73	1413	4248	56	S6	1113	135	90	S40	4788	2111.5
24	S74	1263	4248	57	S7	1263	135	91	S41	4788	2271.5
25	S75	1113	4248	58	S8	1413	135	92	S42	4788	2431.5
26	S76	963	4248	59	S9	1563	135	93	S43	4788	2591.5
27	S77	813	4248	60	S10	1713	135	94	S44	4788	2751.5
28	S78	663	4248	61	S11	1863	135	95	S45	4788	2911.5
29	S79	513	4248	62	S12	2013	135	96	S46	4788	3071.5
*	NC	363	4248	63	S13	2163	135	97	S47	4788	3238.5
30	S80	253	4248	64	S14	2313	135	98	S48	4788	3388.5
31	$\overline{EO}$	130	3871	65	S15	2463	135	99	S49	4788	3538.5
32	NC	*	*	66	S16	2613	135	100	S50	4788	3688.5
33	VEE	130	3607.5	67	S17	2763	135				

Dimensions in Milimeters