

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

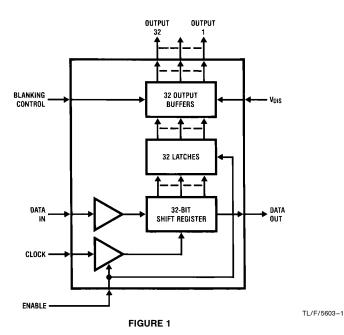
Applications

- COPSTM or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation at 25°C

 $\begin{array}{lll} \mbox{Molded DIP Package, Board Mount} & 2.28W^* \\ \mbox{Molded DIP Package, Socket Mount} & 2.05W^{**} \\ \mbox{*Molded DIP Package, Board Mount,} & \theta_{\mbox{JA}} = 46^{\circ}\mbox{C/W} \\ \mbox{Derate 21.7 mW}^{\circ}\mbox{C Above 25}^{\circ}\mbox{C} \end{array}$

** Molded DIP Package, Socket Mount, $\theta_{\rm JA} = 51^{\circ}{\rm C/W}$ Derate 19.6 mW/°C Above 25°C

Junction Temperature 130°C Lead Temperature (Soldering, 10 seconds) 260°C **Operating Conditions**

 $\begin{array}{c|cccc} & \text{Min} & \text{Max} & \text{Units} \\ \text{Supply Voltage (V}_{DD}) & & & & & \\ V_{SS} = 0V & & 4.5 & 5.5 & V \\ \text{Display Voltage (V}_{DIS}) & -30 & -10 & V \\ \text{Temperature Range} & -40 & +85 & ^{\circ}\text{C} \end{array}$

DC Electrical Characteristics

 $T_{A}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}, V_{DD}=5\text{V}\,\pm0.5\text{V}, V_{SS}=0\text{V}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I _{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD} , $V_{SS} = 0V$, V_{DIS} Disconnected			150	μΑ
I _{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -30V$, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '0'				0.8	٧
V _{IH}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '1'	(Note 1)	2.4			٧
V _{OH}	Data Output Logic Levels Logic '0'	$I_{OUT} = 400 \mu A$			0.4	٧
V _{OH}	Data Output Logic Levels Logic '1'	$I_{OUT} = -10 \mu A$	V _{DD} - 0.5			٧
V _{OH}	Data Output Logic Levels Logic '1'	$I_{OUT} = -500 \mu A$	2.8			٧
I _{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V \text{ or } V_{DD}$	-10		10	μΑ
C _{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
Roff	Display Output Impedances Output Off (Figure 3a)	$V_{DD} = 5.5V, V_{SS} = 0V$ $V_{DIS} = -10V$ $V_{DIS} = -20V$ $V_{DIS} = -30V$	55 60 65		250 300 400	kΩ kΩ kΩ
R _{ON}	Display Output Impedances Output On (Figure 3b)	$V_{DIS} = -10V$ $V_{DIS} = -20V$ $V_{DIS} = -30V$		700 600 500	800 750 680	Ω Ω Ω
V _{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V, I_{OUT} = Open Circuit, \\ -30V \le V_{DIS} \le -10V$	V _{DIS}		V _{DIS} + 2	٧

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400$ μA , TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400$ μA .

AC Electrical Characteristics TA	$= -40$ °C to $+ 85$ °C, $V_{DD} = 5V \pm 0.5V$
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Symbol	Parameter	Conditions	Min	Тур	Max	Units
f _C	Clock Input Frequency	(Notes 3, 4)			800	kHz
t _H	Clock Input High Time		300			ns
tL	Clock Input Low Time		300			ns
t _{DS}	Data Input Setup Time		100			ns
t _{DH}	Data Input Hold Time		100			ns
t _{ES}	Enable Input Setup Time		100			ns
t _{EH}	Enable Input Hold Time		100			ns
t _{CDO}	Data Output Clock Low to Data Out Time	$C_L = 50 pF$			500	ns

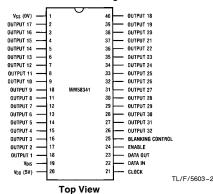
Note 2: Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, $t_f = 800$ kHz, $50\% \pm 10\%$ duty cycle $t_f \le 20$ ns, $t_f \le 20$ n

Note 4: Clock input rise and fall times must not exceed 5 μ s.

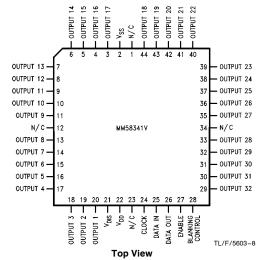
Connection Diagrams

Dual-In-Line Package



Order Number MM58341N See NS Package Number N40A

Plastic Chip Carrier



Order Number MM58341V See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

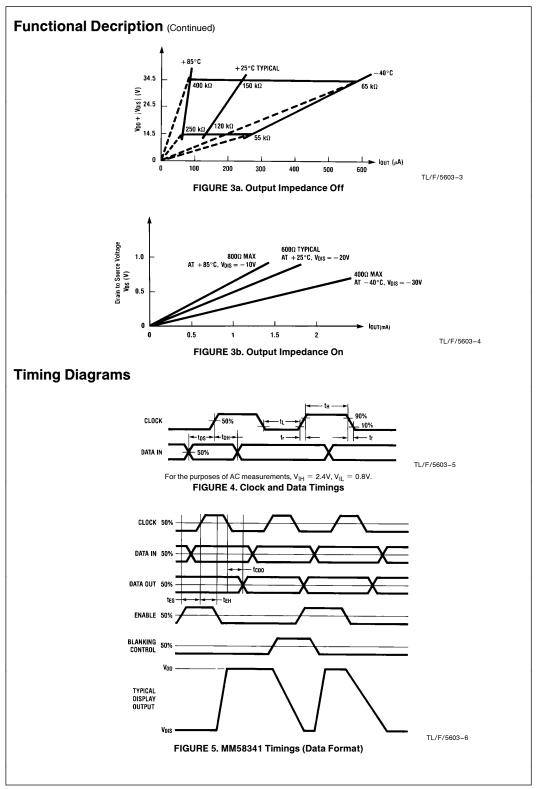
A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 32 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

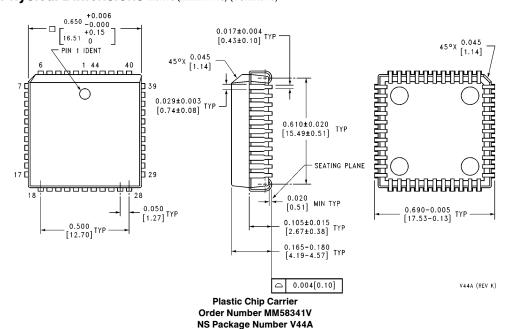
In Figure 5, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'-'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessorbased system where the MM58341 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.



Typical Application 32-DIGIT MULTIPLEXED 5×7 DOT MATRIX VACUUM FLUORESCENT (VF) DISPLAY 35 ANODES 32 GRIDS MM58348 DISPLAY DRIVER MM58341 DISPLAY DRIVER DATA 8 DATA 1 CLOCK 8 CLOCK 1 ENABLE 1 BLANK 1 DATA OUT 1 MICROPROCESSOR TL/F/5603-7 FIGURE 6. Microprocessor-Controlled Word Processor Physical Dimensions inches (millimeters) 40 39 38 37 36 35 34 33 32 31 30 29 28 27 28 25 24 23 22 21 0.062 (1.575) RAD (+)0.550 ±0.005 (13.970 ±0.127) (+)PIN NO. 1 IDENT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 (14.73) MIN 0.030 0.050 (1.270) → TYP 0.600-0.620 (15.240-15.748) 0.125-0.165 (3.175-4.191) 0.009-0.015 (0.229-0.381) 0.625 +0.025 -0.015 0.075 ±0.015 (15.875 +0.635) (1.905 ±0.381) (0.457 ±0.076) Molded Dual-In-Line Package (N) Order Number MM58341N NS Package Number N40A

Physical Dimensions inches (millimeters) (Continued)



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