

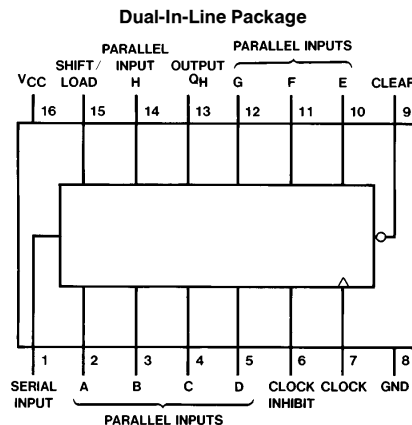
## DM54166 8-Bit Parallel In/Serial Out Shift Registers

### General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on

the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

### Connection Diagram



TL/F/6554-1

Order Number DM54166J  
See NS Package Number J16A

### Function Table

Inputs						Internal Outputs		Output Q <sub>H</sub>
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q <sub>A</sub>	Q <sub>B</sub>	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from Low to High Level

a...h = The level of steady-state input at inputs A through H, respectively

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = The level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established

Q<sub>An</sub>, Q<sub>Gn</sub> = The level of Q<sub>A</sub>, Q<sub>G</sub>, respectively, before the most recent ↑ transition of the clock

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	–55°C to +125°C
DM54	
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter		DM54166			Units
			Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	V
V <sub>IH</sub>	High Level Input Voltage		2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8	V
I <sub>OH</sub>	High Level Output Current				–0.8	mA
I <sub>OL</sub>	Low Level Output Current				16	mA
f <sub>CLK</sub>	Clock Frequency (Note 4)		0		25	MHz
t <sub>W</sub>	Pulse Width (Note 4)	Clock	24			ns
		Clear	20			
t <sub>SU</sub>	Setup Time (Note 4)	Mode	30			ns
		Data	20			
t <sub>H</sub>	Data Hold Time (Note 4)		0			ns
T <sub>A</sub>	Free Air Operating Temperature		–55		125	°C

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –12 mA			–1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			–1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	–20		–57	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		72	104	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

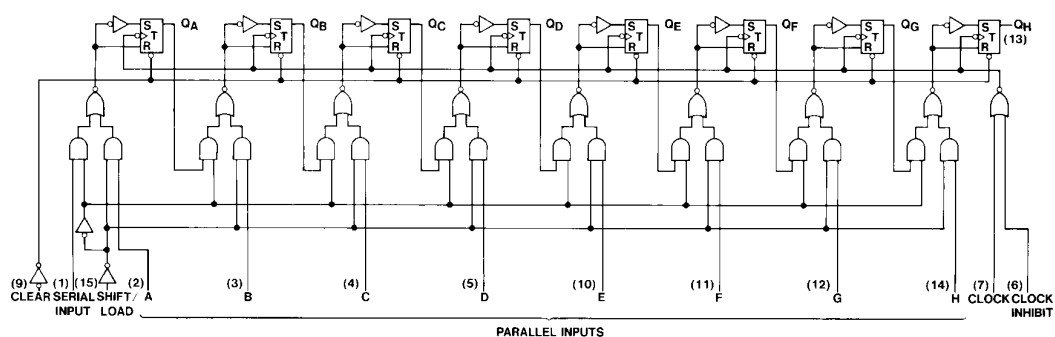
Note 3: With all outputs open, 4.5V applied to the SERIAL input, all other inputs except CLOCK grounded, I<sub>CC</sub> is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Note 4: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

### Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R <sub>L</sub> = 400Ω, C <sub>L</sub> = 15 pF		Units
			Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency		25		MHz
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	Clock to Output	8	26	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	Clock to Output	8	30	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	Clear to Output		35	ns

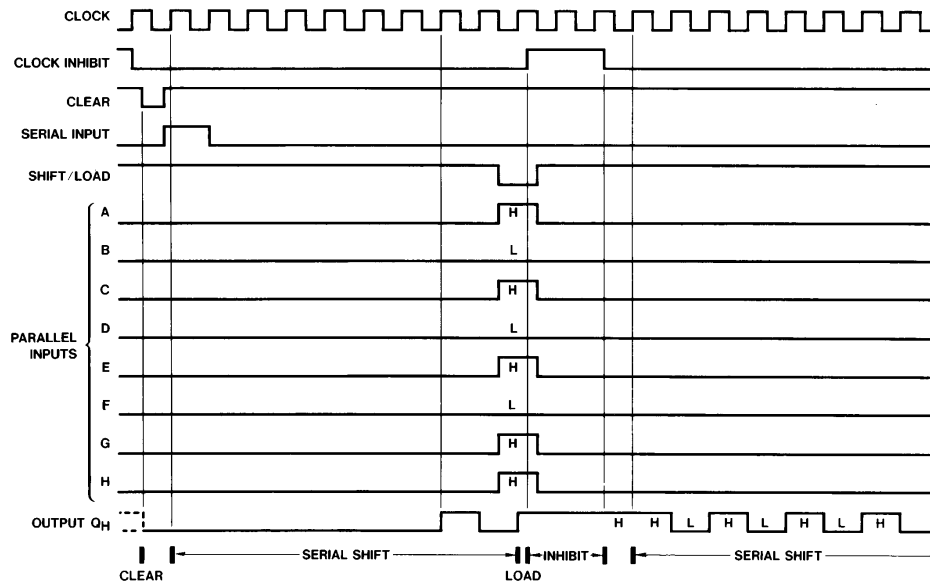
### Logic Diagram



TL/F/6554-2

## Timing Diagram

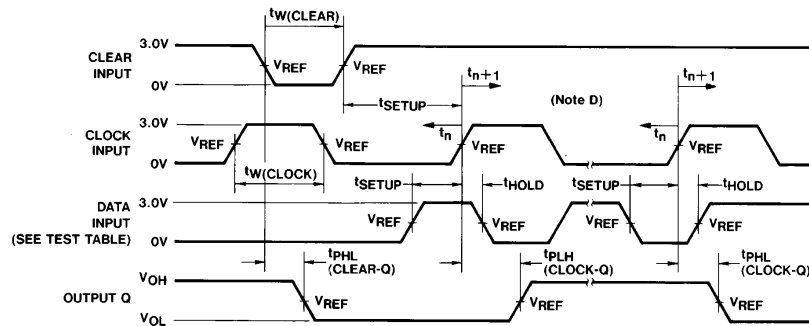
Typical Clear, Shift, Load, Inhibit, and Shift Sequences



TL/F/6554-3

## Parameter Measurement Information

Voltage Waveforms



TL/F/6554-4

Test Table for Synchronous Inputs

Data Input For Test	Shift/Load	Output Tested (See Note C)
H	0V	$Q_H$ at $T_N + 1$
Serial Input	4.5V	$Q_H$ at $T_N + 8$

**Note A:** The clock pulse has the following characteristics:

$t_W(\text{clock}) \geq 20 \text{ ns}$  and  $\text{PRR} = 1 \text{ MHz}$ .

The clear pulse has the following characteristics:

$t_W(\text{clear}) \geq 20 \text{ ns}$  and  $t_{\text{HOLD}} = 0 \text{ ns}$ .

When testing  $f_{\text{MAX}}$ , vary the clock PRR.

**Note B:** A clear pulse is applied prior to each test.

**Note C:** Propagation delay times ( $t_{\text{PLH}}$  and  $t_{\text{PHL}}$ ) are measured at  $t_n + 1$ . Proper shifting of data is verified at  $t_n + 8$  with a functional test.

**Note D:**  $t_n$  = bit time before clocking transition.

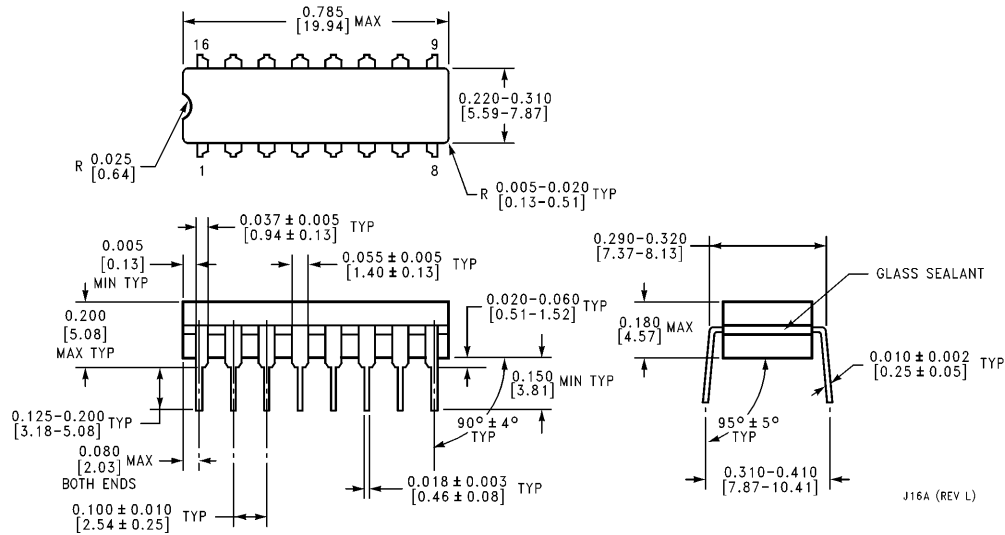
$t_n + 1$  = bit time after one clocking transition.

$t_n + 8$  = bit time after eight clocking transitions.

**Note E:**  $V_{\text{REF}} = 1.5\text{V}$  for 166.



## Physical Dimensions inches (millimeters)



**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54166J**  
**NS Package Number J16A**

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