

DP8307A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

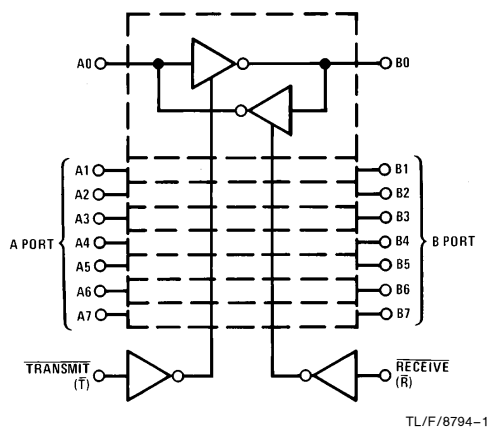
The DP8307A is a high speed Schottky 8-bit TRI-STATE bidirectional transceiver designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, it features glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/Receive (T/R) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 is featured with Transmit (T) and Receive (R) control inputs.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\bar{T}$ and $\bar{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams

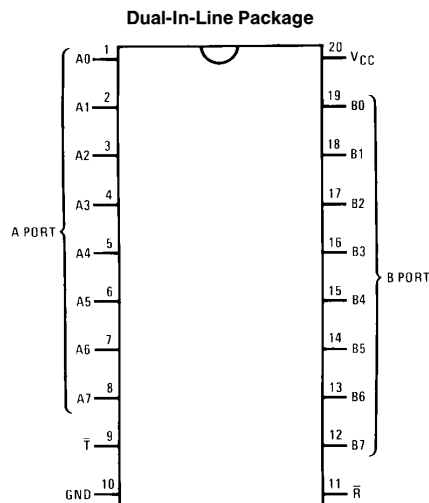


Logic Table

Control Inputs		Resulting Conditions	
Transmit	Receive	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

TRI-STATE® is a registered trademark of National Semiconductor Corporation.



Top View

Order Number DP8307AN
See NS Package Number N20A

DP8307A 8-Bit TRI-STATE Bidirectional Transceiver (Inverting)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Lead Temperature (soldering, 4 sec.)

260°C

Storage Temperature

−65°C to +150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V _{IH}	Logical “1” Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$		2.0			V
V _{IL}	Logical “0” Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$				0.7	V
V _{OH}	Logical “1” Output Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$ $V_{IL} = 0.5V$	I _{OH} = −0.4 mA I _{OH} = −3 mA	V _{CC} − 1.15 2.7	V _{CC} − 0.7 3.95		V V
V _{OL}	Logical “0” Output Voltage	$\overline{T} = 2.0V,$ $\overline{R} = V_{IL}$	I _{OL} = 16 mA I _{OL} = 8 mA		0.35 0.3	0.5 0.4	V V
I _{OS}	Output Short Circuit Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_O = 0V,$ $V_{CC} = \text{Max, (Note 4)}$		−10	−38	−75	mA
I _{IH}	Logical “1” Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IH} = 2.7V$			0.1	80	μA
I _I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V, V_{CC} = \text{Max}, V_{IH} = 5.25V$				1	mA
I _{IL}	Logical “0” Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IN} = 0.4V$			−70	−200	μA
V _{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12\text{ mA}$			−0.7	−1.5	V
I _{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	V _{IN} = 0.4V V _{IN} = 4.0V			−200 80	μA μA
B PORT (B0–B7)							
V _{IH}	Logical “1” Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$		2.0			V
V _{IL}	Logical “0” Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$				0.7	V
V _{OH}	Logical “1” Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$ $V_{IL} = 0.5V$	I _{OH} = −0.4 mA I _{OH} = −5 mA I _{OH} = −10 mA	V _{CC} − 1.15 2.7 2.4	V _{CC} − 0.8 3.9 3.6		V V V
V _{OL}	Logical “0” Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	I _{OL} = 20 mA I _{OL} = 48 mA		0.3 0.4	0.4 0.5	V V
I _{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_O = 0V,$ $V_{CC} = \text{Max, (Note 4)}$		−25	−50	−150	mA
I _{IH}	Logical “1” Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IH} = 2.7V$			0.1	80	μA
I _I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V, V_{CC} = \text{Max}, V_{IH} = 5.25V$				1	mA
I _{IL}	Logical “0” Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IN} = 0.4V$			−70	−200	μA
V _{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12\text{ mA}$			−0.7	−1.5	V
I _{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	V _{IN} = 0.4V V _{IN} = 4.0V			−200 +200	μA μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS $\bar{T}$, $\bar{R}$						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$		0.5	20	μA
I_I	Maximum Input Current	$V_{CC} = \text{Max}$, $V_{IH} = 5.25V$			1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$, $\bar{R}$		-0.1	-0.25	mA
		$\bar{T}$		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12 \text{ mA}$		-0.8	-1.5	V
POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current	$\bar{T} = \bar{R} = 2.0V$, $V_{IN} = 2.0V$, $V_{CC} = \text{Max}$		70	100	mA
		$\bar{T} = 0.4V$, $V_{INA} = \bar{R} = 2V$, $V_{CC} = \text{Max}$		100	150	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\bar{T} = 2.4V$, $\bar{R} = 0.4V$ (Figure A) $R1 = 1k$, $R2 = 5k$, $C1 = 30 \text{ pF}$		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\bar{T} = 2.4V$, $\bar{R} = 0.4V$ (Figure A) $R1 = 1k$, $R2 = 5k$, $C1 = 30 \text{ pF}$		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\bar{R}$ to A Port	$B0 \text{ to } B7 = 2.4V$, $\bar{T} = 2.4V$ (Figure B) $S3 = 1$, $R5 = 1k$, $C4 = 15 \text{ pF}$		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\bar{R}$ to A Port	$B0 \text{ to } B7 = 0.4V$, $\bar{T} = 2.4V$ (Figure B) $S3 = 0$, $R5 = 1k$, $C4 = 15 \text{ pF}$		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\bar{R}$ to A Port	$B0 \text{ to } B7 = 2.4V$, $\bar{T} = 2.4V$ (Figure B) $S3 = 1$, $R5 = 1k$, $C4 = 30 \text{ pF}$		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\bar{R}$ to A Port	$B0 \text{ to } B7 = 0.4V$, $\bar{T} = 2.4V$ (Figure B) $S3 = 0$, $R5 = 5k$, $C4 = 30 \text{ pF}$		24	35	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\bar{T} = 0.4V$, $\bar{R} = 2.4V$ (Figure A) $R1 = 100\Omega$, $R2 = 1k$, $C1 = 300 \text{ pF}$		12	18	ns
		$R1 = 667\Omega$, $R2 = 5k$, $C1 = 45 \text{ pF}$		8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\bar{T} = 0.4V$, $\bar{R} = 2.4V$ (Figure A) $R1 = 100\Omega$, $R2 = 1k$, $C1 = 300 \text{ pF}$		15	23	ns
		$R1 = 667\Omega$, $R2 = 5k$, $C1 = 45 \text{ pF}$		9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\bar{T}$ to B Port	$A0 \text{ to } A7 = 2.4V$, $\bar{R} = 2.4V$ (Figure B) $S3 = 1$, $R5 = 1k$, $C4 = 15 \text{ pF}$		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\bar{T}$ to B Port	$A0 \text{ to } A7 = 0.4V$, $\bar{R} = 2.4V$ (Figure B) $S3 = 0$, $R5 = 1k$, $C4 = 15 \text{ pF}$		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\bar{T}$ to B Port	$A0 \text{ to } A7 = 2.4V$, $\bar{R} = 2.4V$ (Figure B) $S3 = 1$, $R5 = 100\Omega$, $C4 = 300 \text{ pF}$		32	40	ns
		$S3 = 1$, $R5 = 667\Omega$, $C4 = 45 \text{ pF}$		18	25	ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\bar{T}$ to B Port	$A0 \text{ to } A7 = 0.4V$, $\bar{R} = 2.4V$ (Figure B) $S3 = 0$, $R5 = 1k$, $C4 = 300 \text{ pF}$		25	35	ns
		$S3 = 0$, $R5 = 5k$, $C4 = 45 \text{ pF}$		16	25	ns

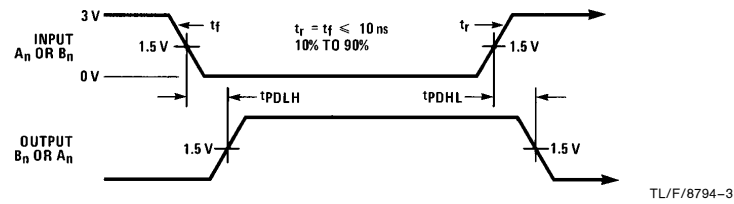
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

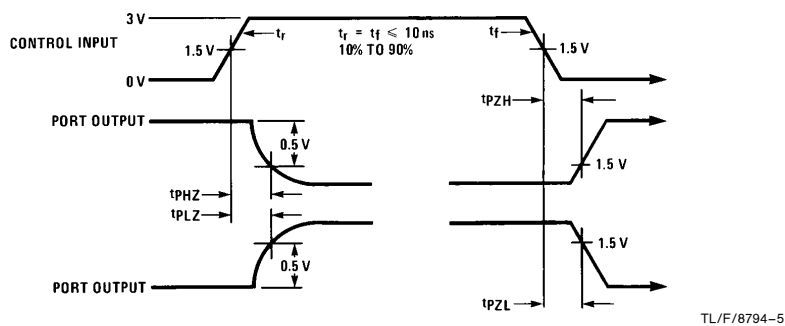
Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



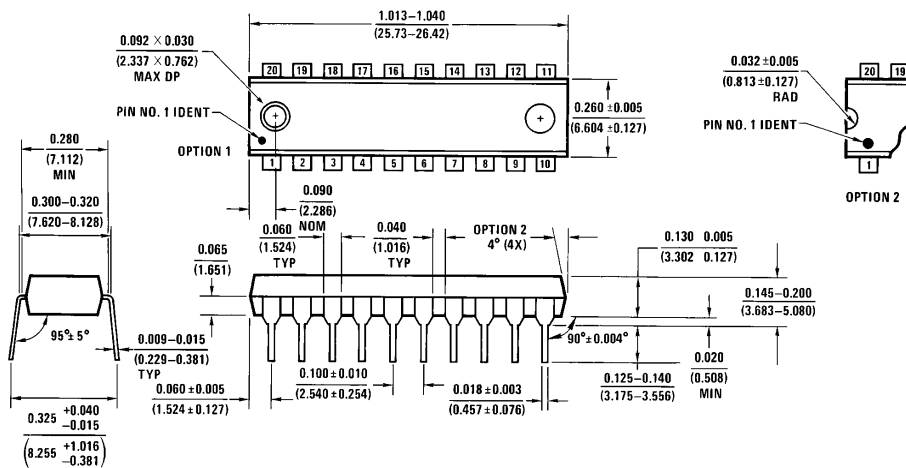
Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\bar{R}$ to A Port and $\bar{T}$ to B Port



DP8307A 8-Bit TRI-STATE Bidirectional Transceiver (Inverting)

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number DP8307AN
NS Package Number N20A

N20A (REV G)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: (800) 272-9959
 Fax: (800) 737-7018

<http://www.national.com>

National Semiconductor Europe

Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 180-530 85 85
 English Tel: +49 (0) 180-532 78 32
 Français Tel: +49 (0) 180-532 93 58
 Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.

19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2308
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.