National Semiconductor

PRELIMINARY
July 1994

TP3420A ISDN S/T Interface Device

General Description

The TP3420A is an enhanced version of the TP3420, with a number of upgraded features for compliance with the new release of ANSI T1.605-1991 and CCITT I-430. At initial power-up the device is fully backwards compatible with the TP3420 device, and modifications to the firmware are only required to take advantage of the new features.

The TP3420A S Interface Device (SID™) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced 1.0 micron double-metal CMOS process, and requires only a single +5V supply. All functions specified in CCITT recommendation I.430 (1991) and ANSI T1.605 (1991) for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as a PABX line-card or trunk-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. 2 'B' channels, each of 64 kb/s, and 1 'D' channel at 16 kb/s are available for users' data. In addition, the TP3420A provides the 800 b/s "S1", "S2" & "Q" multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by the TP3420A SID, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters (24AWG). Adaptive receive signal processing ensures low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

Features

- 2 B + D 4-wire 192 kb/s transceiver
- Selectable TE or NT mode
- Exceeds I.430 range: 1.5 km point-to-point
- Adaptive receiver for high noise immunity
- Adaptive and fixed timing options for NT-1
- Clock resynchronizer and elastic buffers for NT-2/LT
- Slave-slave mode for NT-2 trunks
- Extensive hardware support for SC1, SC2 and Q channel messaging
- Bipolar violation detection and FECV messaging
- Selectable system interface formats
- MICROWIRE™ and SCP compatible serial control interface
- TP3054/7 Codec/Filter COMBO™ compatibility
- Single +5V supply
- 20-pin package DIP, PLCC

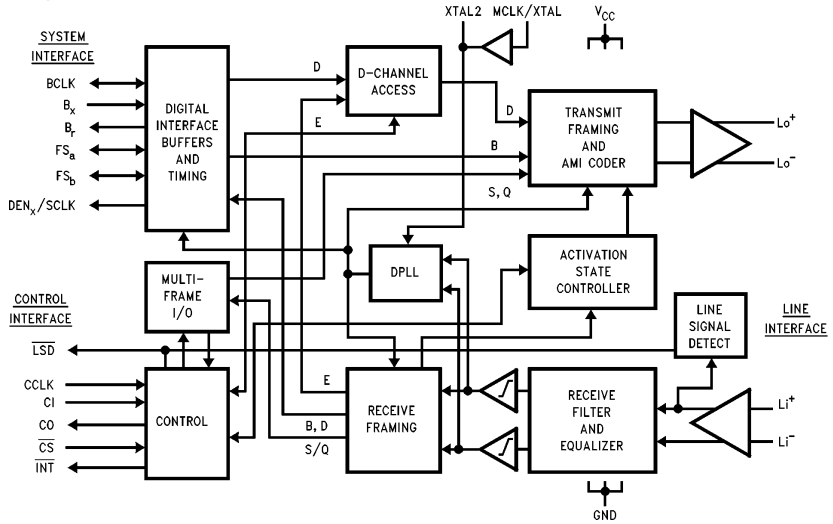
Applications

- Same Device for NT, TE and PBX Line Card
- Point-to-Point Range Extended to 1.5 km
- Point-to-Multipoint for all I.430 Configurations
- Easy Interface to:

LAPD Processor	MC68302, HPC16400
Terminal Adapter	MC68302, HPC16400
Codec/Filter COMBO™	TP3054/7 and TP3076
"U" Interface Device	TP3410

  Line Card Backplanes—No External PLL Needed
- Line Monitor Mode for Test Equipment

Block Diagram



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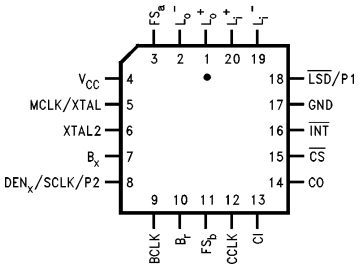
RRD-B30M115/Printed in U. S. A.

Connection Diagrams

TP3420A SID



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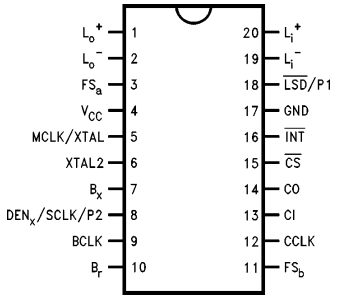
Order Number TP3420AV
See NS Package Number V20A

TP3420A SID



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Top View

Order Number TP3420AJ or TP3420AN
See NS Package Number J20A or N20A

Pin Descriptions

Name	Description
GND	Negative power supply pin, normally 0V (ground). All analog and digital signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be +5V ±5% relative to GND.
MCLK/XTAL	The 15.36 MHz Master Clock input, which requires either a crystal* to be tied between this pin and XTAL2, or a CMOS logic level clock input from a stable source. When using a crystal, a total of 33 pF load capacitance to GND must also be connected.**
XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, and 33 pF of load capacitance to GND.** If using an external master Clock via the MCLK pin, leave the XTAL2 pin unconnected.
BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data at the digital interface. When NT mode or TES mode is selected, BCLK is a TTL/CMOS input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When TEM mode is selected, this pin is a CMOS output at frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal and is synchronous with the data on B_x and B_r.
FS_a	In NT modes and TES mode, this pin is the Transmit Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into B_x. In TEM mode only, this pin is a digital output pulse whose positive indicates the start of the 'B' channel data transfer at both B_x and B_r.
FS_b (Pin 11)	In NT modes and TES mode, this pin is the Receive Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time of the device for receive 'B' and 'D' channel data out from B_r. In TEM mode only, when digital interface Format 1 is selected, this pin is an 8-bit wide pulse which indicates the active slot for the B2 channel on the digital interface. The DCKE command will alter the function of this pin. See Table I.a for details.
B_x	TTL/CMOS input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	CMOS output for 'B' and 'D' channel data received from the line, which is synchronous with BCLK. When not shifting data, this pin is TRI-STATE®.
DEN_x/p2 (Pin 8)	In TEM mode, this pin by default is a CMOS output which is normally low and pulses high to indicate the active bit-times for 'D' channel Transmit data at the B_x input. It is intended to be gated with BCLK to control the shifting of data from layer 2 device to the TP3420A transmit buffer. In NT modes, this pin by default is a pulse output (DEN_x) which occurs in every 8 KHz frame and indicates the location of D channel data input on the B_x pin. In TES mode, this pin by default is an output synchronized clock (SCLK) at the frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal, and is intended to be used as the BCLK source. This pin called P2 in Table I can also be programmed to provide alternate functions. See Table I for details.
CI	MICROWIRE control channel serial data TTL/CMOS input.
CO	Control channel serial data CMOS output for status information. When not enabled by $\overline{CS}$, this output is TRI-STATE.
CCLK	TTL/CMOS clock input for the Control Channel.
$\overline{CS}$	Chip Select input which enables the control channel data to be shifted in and out when pulled low. When high, this pin inhibits the Control interface.

*Crystal specification: 15.36 MHz parallel resonant; $R_s \leq 150\Omega$, $C_L = 20$ pF and $C_O < 7$ pF.
**The 33 pF includes any board capacitance.

Pin Descriptions (Continued)

Name	Description
$\overline{INT}$	Interrupt output, a latched n-channel open-drain output signal which is normally high impedance, and goes low to indicate a change of status of the loop transmission system.
$\overline{LSD}$/P1 (Pin 18)	In all modes, this pin by default is the Line Signal Detect output, an n-channel open-drain output which is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to ''wake-up'' a microprocessor from a low-power idle mode. This output is high impedance when the device is powered up. This pin P1 in Table I can also be programmed to provide alternate functions. See Table I for details.
L_o+, L_o-	Transmit AMI signal differential outputs to the line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in I.430.
L_i+, L_i-	Receive AMI signal differential inputs from the line transformer. The L_i- pin is also the internal voltage reference pin, and must be decoupled to GND with a 10 μf capacitor in parallel with a 0.1 μF ceramic capacitor.

ALTERNATE PIN FUNCTIONS

With a MICROWIRE command PINDEF (B'1110 0 x2 x1 x0) the pin signal functions of these pins can be changed to provide alternate functions (see Table I and the MICROWIRE command in Table III). ''*'' indicates the default pin function after a device mode selection. Power-up default device mode is NTA.

TABLE I. Alternate Pin Function Assignment

Device Mode	P2 - Pin 8		P1 - Pin 18	
	Function	x_2	Function	x_1, x_0
TEM	DENx*	0*	$\overline{LSD}$	00*
	SCLK	1	DENr	01
			SCLK	10
			DENx	11
TES	DENx	0	$\overline{LSD}$	00*
	SCLK*	1*	DENr	01
			SCLK	10
			DENx	11
NTA NTF	DENx*	0*	$\overline{LSD}$	00*
	SCLK	1	DENr	01
			SCLK	10
			DENx	11
MMA	DENx*	0*	$\overline{LSD}$	00*
	SCLK	1	DENr	01
			SCLK	10
			DENx	11

PINDEF command is coded as X'EX (i.e. $11100x_2x_1x_0$).
*Default pin function after device mode selection.

SIGNAL DESCRIPTION

SCLK is an output synchronized clock at the frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal, and is intended to be used as the BCLK source.

LSD is the Line Signal Output, an n-channel open-drain output that is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to ''wake-up'' a microprocessor from a low-power idle mode. This output is a high impedance when the device is powered up.

DENr is a CMOS output that is normally low and pulses high to indicate the active bit times for 'D' channel Receive data at the B_r output pin. It is intended to be gated with BCLK to control the shifting of data from the TP3420A receive buffer to a layer 2 device.

DENx is a CMOS output that is normally low and pulses high to indicate the active bit times for D channel Transmit data at the B_x input. It is intended to be gated with BCLK to control the shifting of data from a layer 2 device to the TP3420A's transmit buffer. In NT mode, this pulse occurs every 8 kHz frame and indicates the location of D channel data input on the B_x pin.

ADDITIONAL PIN CONFIGURATION

The TP3420A in TEM mode can be configured to interface with the Motorola layer-2 devices such as the MC68302 and the MC145488. A PINDEF (X'E1) command followed by a DCKE (X'F1) command will alter the TP3420A pin functions as shown in Table Ia. Other configurations of PINDEF are not supported.

TABLE Ia

Pin Number	Pin Function
8	DTCK
11	TxD
18	DRCK

Where:

- DCLK is a burst clock output intended to be used as a clock source for the transmitter of an HDLC device.
- TxD is an input being sampled on the rising edge of DCLK during the active D-channel timeslot.
- DRCK is a burst clock output which pulses 2 BCLK periods every 8 kHz frame. This output is intended to be used as a clock source for the receiver of an HDLC device. The D-channel data at B_r is transmitted on the falling edge of the DRCK.

Functional Description

DEVICE MODES

The TP3420A can be programmed into one of four possible modes. For NT applications select NT Adaptive timing (NTA) for all wiring configurations except a Short Passive Bus, for which NT Fixed Timing (NTF) should be selected. In TE applications, select TE Master mode (TEM) for the device to be the master (source) of clocks at the digital interface, or select TE Slave mode (TES) for the digital interface to accept clocks from the system.

Functional Description (Continued)

Selection of these modes is described in the section on Control Register instructions.

POWER-ON DEVICE CONDITIONS

Following the initial application of power, the TP3420A SID enters the power-down (de-activated) state, in which all the internal circuits including the Master oscillator are inactive and in a low power state except for the Line-Signal Detect circuit; the line outputs L_o+/L_o- are in a high impedance state and the Digital System Interface is inactive. All bits in the Control Register power-up as indicated in Table 1. In both NT and TE modes, a Line-Signal Detect circuit monitors the line while the device is powered-down, to enable loop transmission to be initiated from either end.

POWER-OFF DEVICE CONDITION

When power to the TP3420A is turned off, the Line outputs L_o+/L_o- go into high impedance state, hence if a TE on a passive bus lost power its transmit impedance still meets the specification without any external relay (see AN665 for external protection components). The receiver impedance also remains in specification.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate-Mark Inversion (AMI) coding with inverted binary is used, as illustrated in *Figure 1*. This coding rule requires that a binary ONE is represented by 0V high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty-cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c.-balanced line signal.

The frame format used in the TP3420A SID follows the CCITT recommendation specified in I.430 and illustrated in *Figure 2*. Each complete frame consists of 48 bits, with a line bit rate of 192 kb/s, giving a frame repetition rate of 4 kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0^+ bit followed by a 0^- balance bit to indicate the start of a frame, and forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to the Terminal Equipment (TE) transmission direction the frame contains an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE. The last bit of this frame is used as a frame balancing bit. In the TE to NT direction, d.c.-balancing is carried out for each channel, as illustrated in *Figure 2*.

LINE TRANSMIT SECTION

The differential line-driver outputs, L_o+ and L_o-, are designed to drive a transformer with an external termination resistor. A suitable 2:1 transformer, terminated in 50Ω, results in a signal amplitude of nominally 750 mV pk on the line which fully complies with the I.430 pulse mask specifications. When driving a binary 1 symbol the output presents a high impedance in accordance with I.430. When driving a $0+$ or $0-$ symbol a voltage-limited current source is turned on. Short-circuit protection is included in the output stage; over-voltage protection is required externally, see the Applications section.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 transformer, or a 1:2 transformer of the same type used for the transmit direction. At the front-end of the receive section is a continuous filter which limits the noise bandwidth. To correct pulse attenuation and distortion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a ''flat'' channel response with maximum eye opening over a wide spread of cable attenuation characteristics. This equalizer is always enabled when either TE mode or NT Mode Adaptive Sampling is selected, but is disabled for short passive bus applications when NT Mode Fixed Sampling is selected. An adaptive threshold circuit maximizes the Signal-to-Noise ratio in the eye at the detector for all loop conditions.

In NTF mode the receive baud sampling point is fixed relative to the transmit baud clock. This ensures accurate sampling of received pulses with differential delays on a passive bus, thus extending the short passive bus range to over 250m of low capacitive cable.

In NTA and TE modes, the receive baud sampling is adaptive. In these modes, a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Clocks for the digital interface timing may either be derived from this recovered clock, as in TE mode Digital System Interface Master, or may be slaved to an external source, as in the T-interface side of an NT-2 (TES mode). In TES and NT modes, re-timing circuitry on the TP3420A allows the MCLK frequency to be plesiochronous (i.e., free-running) with respect to the network clock, i.e. the 8 kHz FS_a input. With a tolerance on the MCLK oscillator of 15.36 MHz ±100 ppm, the lock-in range of the DPLL allows the network clock frequency to deviate up to ±50 ppm from nominal.

When the device is powered-down (either on initial powering-on of the device or after using a PDN command), a Line-Signal Detect circuit is enabled to detect the presence of incoming data if the far-end starts to activate the loop. The LSD circuit is disabled by a Power-Up (PUP) command.

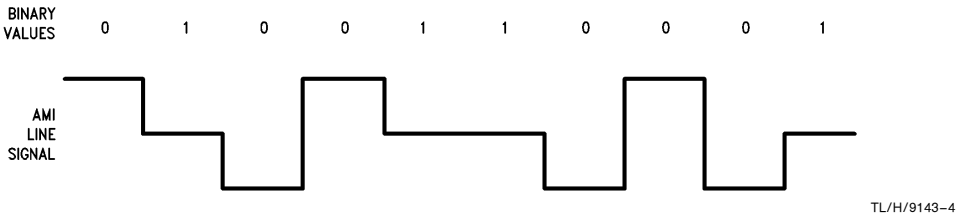

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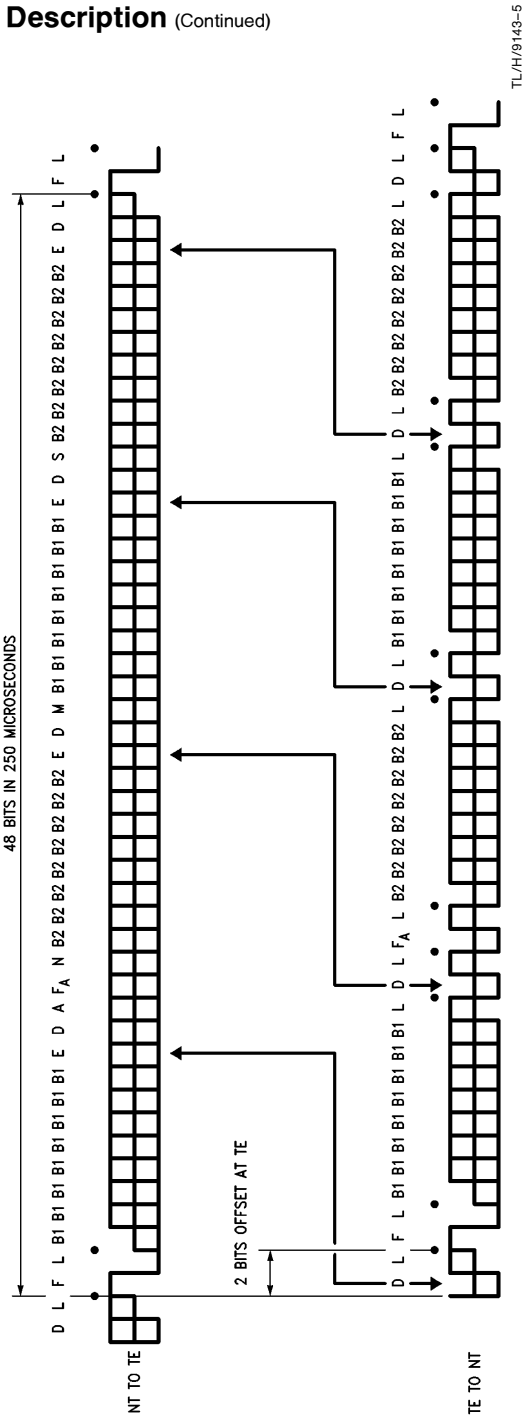
FIGURE 1. Inverted AMI Line-Coding Rule

Functional Description (Continued)



Legend:

F	= Framing bit	N	= bit set to a binary value N = $\overline{F_A}$
L	= DC Balancing bit	B1	= bit within B-channel 1
D	= D-channel bit	B2	= bit within B-channel 2
E	= D-echo-channel bit	A	= bit used for activation
F_A	= Auxiliary framing bit or Q Channel bit	S	= S Channel bit
M	= Multiframe Sync bit		

• Dots mark the boundaries of those parts of the frame that are independently DC-balanced

FIGURE 2. Frame Format

Functional Description (Continued)

DIGITAL SYSTEM INTERFACE

The Digital System Interface (DSI) on the TP3420A combines 'B' and 'D' channel data onto common pins to provide maximum flexibility with minimum pin count. Several multiplexed formats of the B and D channel data are available as shown in *Figure 3*. Selection is made via the Control Register.

NTA, NTF and TES modes: at this interface, phase skew between transmit and receive frames may be accommodated when the device is a slave at the Digital Interface (NT and TES Modes) since separate frame sync inputs (Figure 3a), FS_a and FS_b, are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface. The serial shift rate is determined by the BCLK input, and may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. Thus, for applications on a PABX line-card (in NT mode), the 'B' and 'D' channel slots can be interfaced to a TDM bus and assigned to a time-slot.

TEM mode: in TE Master Mode (TEM), FS_a is an output (Figure 3b) indicating the start of both transmit and receive 'B' channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the format selected, see Table IV.

TES mode: for applications such as the network side of an NT-2, e.g. a PBX trunk card, the TE Slave (TES) Mode is provided. This ''slave-slave'' mode allows the transmission side of the device to be a slave to the received frame timing, while the Digital System Interface is also in a slave mode i.e. FS_a, FS_b and BCLK are inputs. The Digital System Interface includes elastic buffers which allow any arbitrary phase relationship between each FS input and the received I.430 frame.

JITTER ABSORPTION AND PHASE WANDER BUFFERS

The TP3420A has an improved serial data buffer circuit to handle larger amounts of phase wander exceeding the specification of 18 μs pk-to-pk, regardless of the phase difference between the transmit and receive frames. A SLIP indicator interrupt is generated to inform the CPU if the phase deviation between two clocks exceeds the boundary of the circuit, causing the data buffers to adjust the internal delay to accommodate this. Under some, but not all, circumstances this will result in data errors as the slip occurs. Separate interrupt status values (SLIP—TX and SLIP—RX) indicate the clock slippage in the transmit buffer or the receiver buffer.

TES Mode also provides a synchronized clock output (SCLK) which is phase-locked to the received line signal; SCLK may be used as the BCLK source.

TABLE II. DSI Format Rates

Format	BLCK as DSI Master (Output)*	BCLK as DSI Slave (Input)
1	2.048 MHz	256 kHz–4.096 MHz
2	256 kHz	256 kHz–4.096 MHz
3	512 kHz	512 kHz–4.096 MHz
4	2.56 MHz	256 kHz–4.096 MHz

*__Note:__ also SCLK output in TES Mode.

MICROWIRE CONTROL INTERFACE

A serial interface, which can be clocked independently from the 'B' and 'D' channel system interface, is provided for microprocessor control of various functions in the TP3420. This port can be used when the device is powered up or powered down. All data transfers consist of a single byte shifted into the Control Register via the CI pin, simultaneous with a single byte shifted out from the Status Register via the CO pin.

Data shifts in to CI on rising edges of CCLK and out from CO on falling edges when $\overline{CS}$ is pulled low for 8 cycles of CCLK. An Interrupt output, $\overline{INT}$ goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising CCLK edge after $\overline{CS}$ goes low. Interrupt Source(s) occurring while another is still pending are stored in a stack and read in sequence, by causing another interrupt at the end of the current $\overline{CS}$ cycle ($\overline{INT}$ can go low only when $\overline{CS}$ is high). When reading the Status Register the CI input is also enabled, therefore a ''dummy'' command e.g. NOP(X'FF) must be loaded into CI as CO is read.

Each source of an Interrupt event (*e.g.,* EI, AI, SLIP) in the device has an internal latch, such that the occurrence of that event is stored until read from the status register. Multiple events will be reported in turn by the device in a circular manner. There is no priority criteria. If multiple occurrences of the same event occur (*e.g.,* EI, followed by AI and then EI) and if left unserviced, than the second occurrence (of EI in this example) will over-write the first. Also if a multiframe interrupt such as MFR1 interrupt is not serviced before a second occurrence of the MFR1 interrupt, then the second value in the M1–M4 bits will overwrite the first. The DI interrupt clears all pending interrupts and indicating the reset state of the device. The LSD interrupt is generated independently and is only valid while the device is in low power mode (PDN). A PUP command resets the line signal detect circuit and the LSD interrupt. A PDN command resets and re-enables the LSD circuit and interrupt.

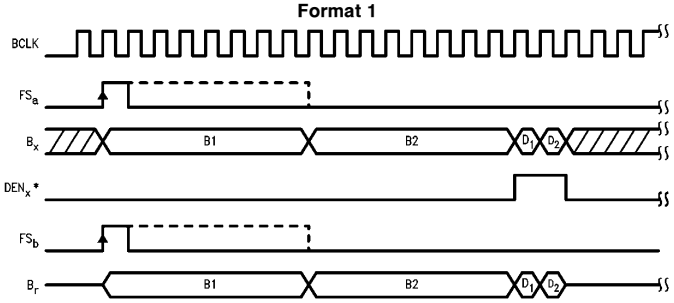
Figure 4 shows the timing for this interface, and Tables III and IV list the control functions and status indicators.

FLEXIBLE MICROWIRE PORT

The MICROWIRE port of the TP3420A has been enhanced such that it can connect to standard MICROWIRE master devices (such as National's microcontrollers of the HPC and COP families) as well as the SCP interface master from the Motorola microcontroller family. SCP is the Serial Control Port on devices such as the MC68302 or the MC145488 HDLC. See the MICROWIRE port timing diagram and the applications section.

Functional Description (Continued)

Format 1



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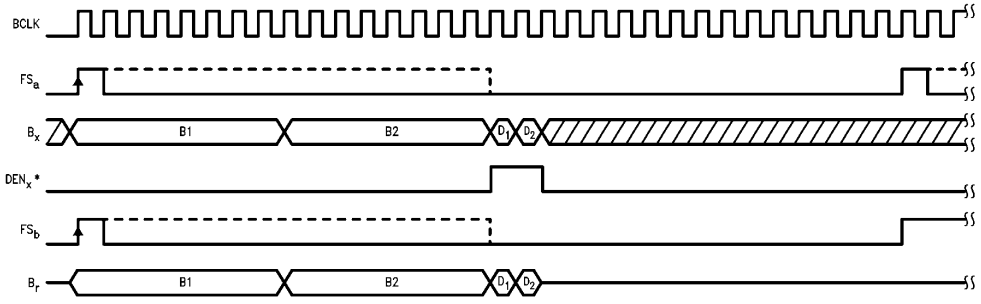
Format 2



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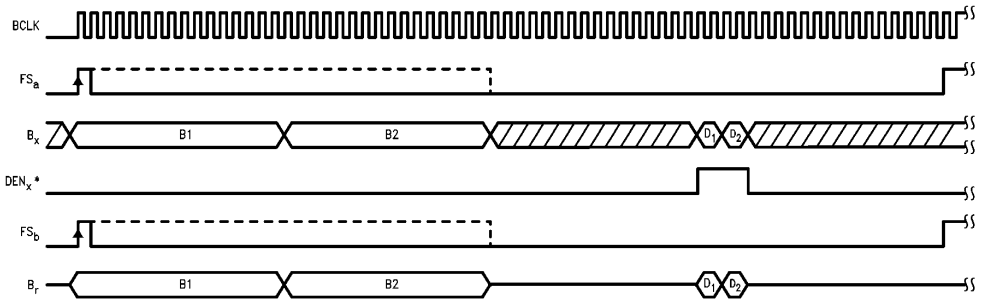
Format 3



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Format 4

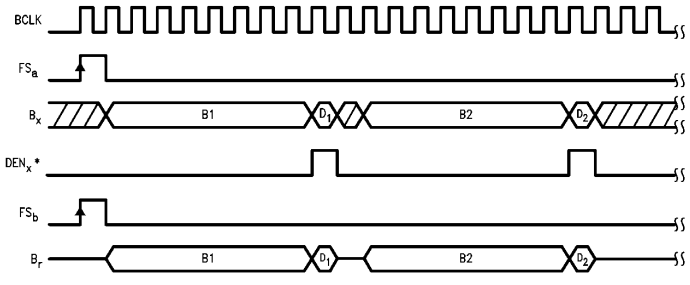

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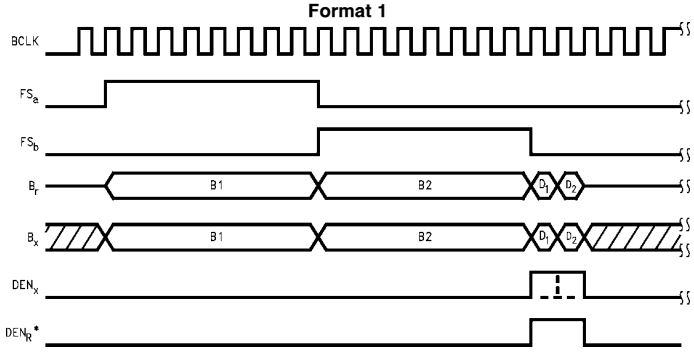
FIGURE 3a. Digital System Interface Formats in NT and TES* modes (DSI Slave)

Note: *In TES mode, DENx outputs SCLK synchronized to the S interface. Format 1, SCLK = 2.048 MHz, Format 2, SCLK = 256 kHz, Format 3, SCLK = 512 kHz, Format 4, SCLK = 2.56 MHz.

Functional Description (Continued)

Format 1



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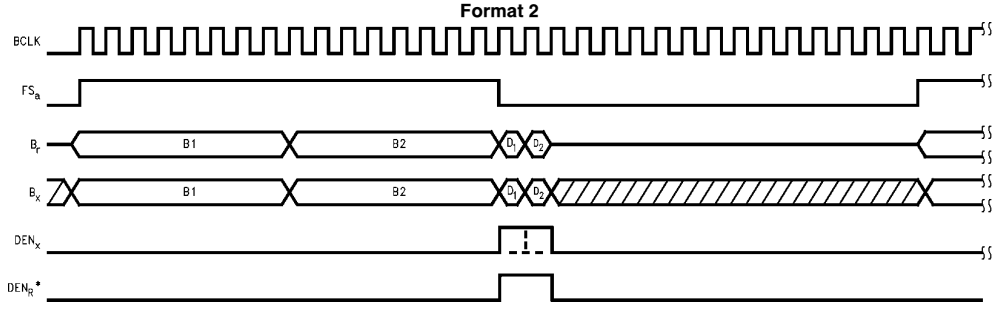
Format 2



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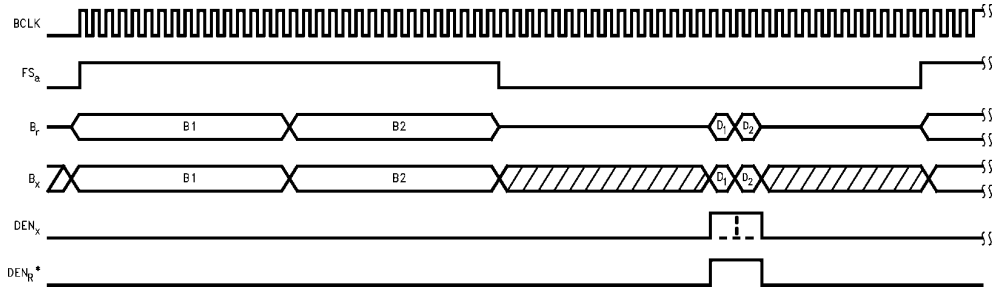
Format 3



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Format 4

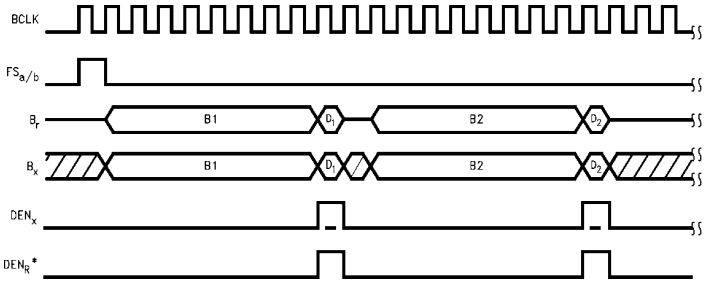

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FIGURE 3b. Digital System Interface Formats in TEM mode (DSI Master)

*__Note:__ DENR signal is available on pin 18 after using the PINDEF command (see Table I).

Functional Description (Continued)

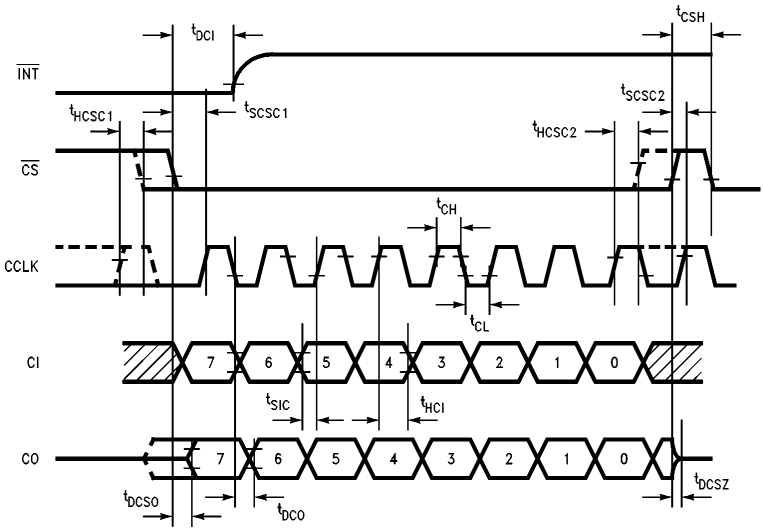

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FIGURE 4. TP3240A Enhanced MICROWIRE Control Interface Timing

Functional Description (Continued)

TABLE III. Control Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Activation/Deactivation									
No Operation	NOP	1	1	1	1	1	1	1	1
*Power-Down	PDN	0	0	0	0	0	0	0	0
Power-Up	PUP	0	0	1	0	0	0	0	0
Deactivation Request	DR	0	0	0	0	0	0	0	1
Force INFO2 (NT only)	FI2	0	0	0	0	0	0	1	0
Monitor Mode Activation	MMA	0	0	0	1	1	1	1	1
Activation Request	AR	0	0	0	0	0	0	1	1
Device Modes									
*NT Mode, Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode, Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Mode, Digital System Interface Slave (Note 1)	TES	0	0	0	0	0	1	1	0
TE Mode, Digital System Interface Master	TEM	0	0	0	0	0	1	1	1
Digital Interface Formats									
*Digital System Interface Format 1	DIF1	0	0	0	0	1	0	0	0
Digital System Interface Format 2	DIF2	0	0	0	0	1	0	0	1
Digital System Interface Format 3	DIF3	0	0	0	0	1	0	1	0
Digital System Interface Format 4	DIF4	0	0	0	0	1	0	1	1
BCLK Frequency Settings									
Set BCLK to 2.048 MHz	BCLK1	1	0	0	1	1	0	0	0
Set BCLK to 256 kHz	BCLK2	1	0	0	1	1	0	0	1
Set BCLK to 512 kHz	BCLK3	1	0	0	1	1	0	1	0
Set BCLK to 2.56 MHz	BCLK4	1	0	0	1	1	0	1	1
B Channel Exchange									
*B Channels Mapped Direct, B1 to B1, B2 to B2	BDIR	0	0	0	0	1	1	0	0
B Channels Exchanged, B1 to B2, B2 to B1	BEX	0	0	0	0	1	1	0	1
D Channel Access									
D Channel Request, Class 1 Message	DREQ1	0	0	0	0	1	1	1	0
D Channel Request, Class 2 Message	DREQ2	0	0	0	0	1	1	1	1
D Channel Access Control									
Enable D-Channel Access Mechanism, TE Mode (Note 2)	DACCE	1	0	0	1	0	0	0	0
Disable D-Channel Access Mechanism, TE Mode (Note 2)	DACCD	1	0	0	1	0	0	0	1
Force Echo Bit to 0	EBIT0	1	0	0	1	0	1	1	0
Force Echo Bit to Inverted Received D Bit	EBITI	1	0	0	1	0	1	1	1
*Reset EBITI and EBIT0 to Normal Condition	EBITNRM	1	0	0	1	1	1	0	0
D Channel Clock Enable	DCKE	1	1	1	1	0	0	0	1
End of Message Interrupt									
*EOM Interrupt Enabled	EIE	0	0	0	1	0	0	0	0
EOM Interrupt Disabled	EID	0	0	0	1	0	0	0	1

* Indicates initial state following Power-on initialization.

Note 1: Slave-slave mode.

Note 2: DACCD is the power up default in TES mode and DACCE is the power up default in TEM mode.

Functional Description (Continued)

TABLE III. Control Register Functions (Continued)

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Multiframe Circuit and Interrupt									
Enable SC1/Q Messaging and MFR1 Interrupt	MIE1	0	0	0	1	0	0	1	0
*Disable SC1/Q Message and Interrupt	MID1	0	0	0	1	0	0	1	1
Enable 5 ms Interrupt (Every Multiframe)	MFC1E	0	0	1	0	0	0	1	0
*Disable 5 ms Interrupt	MFC1D	0	0	1	0	0	0	1	1
Enable 30 ms Interrupt (6 Multiframes)	MFC6E	0	0	1	0	0	1	0	0
*Disable 30 ms Interrupt	MFC6D	0	0	1	0	0	1	0	1
Enable SC2 Messaging and MFR2 Interrupt	MIE2	0	0	1	0	0	1	1	0
*Disable SC2 Messaging and Interrupt	MID2	0	0	1	0	0	1	1	1
Multiframe Receive Message Validation									
Enable 3x and 1x Validation of Received Data	ENV	0	0	1	0	1	0	0	0
*Disable 3x and 1x Validation of Received Data	DISV	0	0	1	0	1	0	0	1
Multiframe Transmit Registers									
Write to Multiframe Transmit Register (SC1/Q Low Priority Messages)	MFT1L	0	0	1	1	M1	M2	M3	M4
Write to Multiframe Transmit Register (SC1/Q High Priority Messages)	MFT1H	0	1	0	0	M1	M2	M3	M4
Write to Multiframe Transmit Register (SC2 Messages)	MFT2	0	1	0	1	M1	M2	M3	M4
B1 Channel Enable/Disable									
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enable/Disable									
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
Loopback Test Modes									
Loopback B1 Towards Line Interface	LBL1	0	0	0	1	1	0	0	0
Loopback B2 Towards Line Interface	LBL2	0	0	0	1	1	0	0	1
Loopback 2B + D Towards Digital Interface	LBS	0	0	0	1	1	0	1	0
Loopback B1 Towards Digital Interface	LBB1	0	0	0	1	1	1	0	0
Loopback B2 Towards Digital Interface	LBB2	0	0	0	1	1	1	0	1
*Clear All Loopbacks	CAL	0	0	0	1	1	0	1	1
Control Device State Reading									
Enable the Device State Output on the NOCST	ENST	1	0	0	1	0	0	1	0
*Disable the Device State Output on the NOCST	DISST	1	0	0	1	0	0	1	1
Control of Additional Interrupts									
Enable the Slip and RMFE Interrupts	ENINT	1	0	0	1	0	1	0	0
*Disable the Slip and RMFE Interrupts	DISINT	1	0	0	1	0	1	0	1
Control Polarity of B Channel Data									
Invert B1 Channel Data	INVB1	1	0	0	1	1	1	0	1
Invert B2 Channel Data	INVB2	1	0	0	1	1	1	1	0
*Normal B1, B2 Data	NRMB12	1	0	0	1	1	1	1	1
Pin Signal Selection									
Redefine Pin Signals (See Table I)	PINDEF	1	1	1	0	0	x2	x1	x0

* Indicates initial state following Power-on Initialization.

Functional Description (Continued)

TABLE IV. Status Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Line Signal Detected Far-End	LSD	0	0	0	0	0	0	1	0
Activation Pending	AP	0	0	0	0	0	0	1	1
Activation Indication	AI	0	0	0	0	1	1	0	0
Error Indication	EI	0	0	0	0	1	1	1	0
Deactivation Indication	DI	0	0	0	0	1	1	1	1
End of D-ch Tx Message	EOM	0	0	0	0	0	1	1	0
Lost Contention for D-ch	CON	0	0	0	0	0	1	1	1
Multiframe Receiver Buffer 1 (SC1/Q)	MFR1	0	0	1	1	M1	M2	M3	M4
Multiframe Receiver Buffer 2 (SC2)	MFR2	0	1	0	1	M1	M2	M3	M4
Multiframe Clock (5 ms or 30 ms)	MFC	0	0	0	0	0	1	0	0
Additional Interrupts after ENINT Command									
Receive Multiframe Error	RMFE	0	0	0	0	0	1	0	1
Phase Slip in Data Buffer for Bx Data	SLIP TX	0	0	0	0	1	0	0	1
Phase Slip in Data Buffer for Br Data	SLIP RX	0	0	0	0	1	0	1	0
Phase Slip for Both Bx and Br Data	SLIP TX/RX	0	0	0	0	1	0	1	1
NO Change Return Status									
*NOC Status after DISST Command	NOC	0	0	0	0	0	0	0	0
NOC Status after ENST Command See Table V for Device State Decoding	NOCST	1	S3	S2	S1	0	0	0	0

* Indicates initial state following Power-on Initialization.

STATUS INDICATOR DESCRIPTIONS

LSD — This interrupt indicates that the far-end of the line is attempting to Activate the interface. May be used as an alternative to the $\overline{\text{LSD}}$ pin to ''wake-up'' a microprocessor.

AP — If set, indicates that either INFO 1 frames have been identified in an NT receiver, or INFO 2 or INFO 4 frames have been identified in a TE receiver. Requires an AR control instruction to allow Activation to be completed.

EOM — This interrupt occurs when the closing flag of a D-channel message has been transmitted by a TE on the S interface, indicating successful completion of a packet. The Interrupt associated with this bit can be disabled via the Control Register if desired.

CON — This interrupt occurs when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.

AI — This interrupt indicates that the interface has been successfully Activated in response to an Activation Request.

EI — Set when loss of frame alignment is detected.

DI — If set, indicates that the interface has been Deactivated.

MFR1 — This interrupt indicates when the Multiframe SC1/Q channel data buffer requires servicing, see Multiframe Maintenance section. The MID1 command disables this interrupt.

MFR2 — This interrupt indicates when the Multiframe SC2 channel data buffer requires servicing, see Multiframe Maintenance section. The MID2 command disables this interrupt.

MFC — This status interrupt provides a transmit multiframe clock. It can be selected to occur on every multiframe boundary (5 ms) by the MFC1E command or on each 6 multiframe boundary (30 ms) by the MFC6E command. This interrupt can be used to synchronize the SC1/Q and SC2 multiframe transmit messages.

RMFE — A bipolar Violation or DC balance error causes this Receive Multiframe Error Interrupt in both NT and TE modes. At the NT end, upon receiving the RMFE interrupt, the local microcontroller must inform the TEs with a FECV message (via the MFT1H register). The NT or the TE end can keep a count of RMFE interrupts to monitor the line block error rate at its receiver.

SLIP — This interrupt indicates if the clock phase shift in the jitter/wander buffers exceeded the phase shift limit and changed the internal data buffer delay to accommodate it. One interrupt is generated and is coded as X'09 for Tx buffer slip: X'0A for Rx buffer slip: and X'0B for both Tx and Rx buffer slip.

NOC — This NOC status is returned for every command when there is no change of status to be reported. It is read in the power-up default state and after the DISST command. No interrupt is generated.

NOCST — This status response occurs only after the ENST command. The NOCST status is returned in response to any subsequent command when there is no status change that needs to be reported with an interrupt. It contains the device activation state information, see the section on Activation State machine access.

Functional Description (Continued)

CONTROL REGISTER INSTRUCTIONS

ACTIVATION/DEACTIVATION

PUP — This power-up command enables all analog circuitry, starts the XTAL and resets the state machines to the de-activated state, i.e. transmitting INFO 0 (no signal). It also inhibits the LSD output.

PDN — This power-down command immediately forces the device to a low power state, without sequencing through any of the de-activation states. It should therefore only be used after the TP3420A has been put in a known state, e.g. in a TE after a DI status indication has been reported. It also enables the LSD circuit.

AR — Activation Request initiates the specified Activation sequence. It is recommended that an AR be delayed at least 2 ms after the device is powered-up using the PUP command.

DR — Deactivation Request, which forces the device through the appropriate deactivation sequence specified in I.430. Should be used at the NT end only.

FI2 — Effective only in NT modes, and only after Activation has been completed, this instruction forces the NT to transmit INFO 2 frames instead of INFO 4, normally to allow testing at the U interface. Provided INFO 3 is still being received from the TE(s), an AP Status Interrupt will be generated and loop synchronization maintained, but 2B + D transmission is inhibited. To restore full loop activation, with the NT sending INFO 4, an AR command is required in the normal way.

MMA — Intended for test equipment applications, this instruction allows the receive line interface (Li±) to be connected to the TE-to-NT direction twisted pair and to activate on the received INFO 3 signals while being the master of the DSI. The received 2B + D can then be passively monitored (the line transmit output Lo± would not be connected). TE Master mode must be selected first (TEM).

DEVICE MODES

NTA — NT Mode, Adaptive Sampling should be selected when the device is in an NT on any wiring configuration up to the maximum specified length for operation. Multiple terminals, if required, must be grouped within approximately 100 meters of each other (depending on cable capacitance, see I.430). The Digital System Interface is a slave to external BCLK and FS sources.

NTF — NT Mode Fixed Sampling may be selected when the device is in an NT on a passive bus wiring configuration up to approximately 200 meters in length (depending on cable type). In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple terminals (nominally up to 8) to be connected anywhere along the passive bus. Again, the DSI is a slave to external BCLK and FS sources.

TEM — TE Mode DSI Master should be selected when the device is in a TE. The TP3420A is then the source of the BCLK and FS signals, and access to the Transmit D channel, including the priority and contention resolution control, is enabled as described in the section on TE Mode D-Channel Access.

TES — TE Mode DSI Slave, otherwise known as "Slave-slave" mode, should be selected when the device is used on the T-interface side of an NT-2. The TP3420A System Interface is then driven by BCLK and FS sources in the NT-2. Data buffers and a clock re-synchronizer enable this interface to function with jittering sources for BCLK and FS. All D Channel access control circuitry is disabled, i.e. D Channel data at the Bx input is continuously transmitted to the line; there is no monitoring of the D-echo channel from the network direction, and DREQ instructions are ignored. Also, the SCLK function is enabled at the DEN_x/SCLK pin.

DIGITAL INTERFACE FORMATS

DIF1) DIF2) DIF3) DIF4) — These instructions select the format of the Digital Interface timing, see *Figures 3a* and *3b*.

BCLK FREQUENCY SETTINGS

$\overline{BCLK1}$ $\overline{BCLK2}$ $\overline{BCLK3}$ $\overline{BCLK4}$ — These instructions change the frequency of a selected Digital Interface Format. They should only be used after the Digital Interface Format has been selected. However, if another DIF command is applied after this command, it will override the BCLK setting.

The default BCLK settings for the DIF formats are as follows:

DIF1 ⟶ BCLK1

DIF2 ⟶ BCLK2

DIF3 ⟶ BCLK3

DIF4 ⟶ BCLK4

B CHANNEL CONTROL

BDIR) BEX) — These commands provide for the exchange of data between the B1 and B2 channels as it passes through the device, (Note 1).

Note 1: When enabling a B channel in conjunction with the BEX Command, the channels are referenced at the Digital System Interface, not the line interface e.g. to connect the B1 slot on the DSI with the B2 slot on the line interface, use the BEX and B1E commands.

B1E) B1D) B2E) B2D) — When either or both B channels are disabled, binary 1s are transmitted on the line in those B channel bit positions, regardless of data at the Bx input, and the Br output is TRI-STATE in those bit positions.

INVB1, INVB2 NRMB12 — These commands allow control over the polarity of the data transmitted over the B1 and B2 channel. The default or the NRMB12 command sets the data to be operated in normal mode. See section on operation over restricted channels.

Functional Description (Continued)

D CHANNEL ACCESS

DREQ1) DREQ2) This is a request from Layer 2 device to the TP3420A (in the TE modes) to attempt to transmit a D channel message at the S interface. Use DREQ1 to select the access priority for a Class 1 message (Q.931 Signaling), or DREQ2 for a Class 2 message.

DACCE) DACCD) DACCD is the power-up default condition in TES mode, and DACCE is the power-up default condition in TEM mode. The D channel Access algorithm can be enabled (by DACCE) or disabled (DACCD) in both TES mode or TEM mode. The D support a passive bus network lines. The DENx pin signal provides the flow control strobe according to the access algorithm.

DCKE) This command alters pin signals to provide direct D-channel flow control with certain HDLC devices. Pin 8 provides gated (DEN_X) DTCK, Pin 18 provides gated (DEN_R) DRCK, and Pin 11 inputs TxD data.

See applications note to interface with MC68302 for use of this command.

EIE Enable EOM interrupt.

EID Disable EOM interrupt.

EBITI, EBIT0, EBITNRM These commands allow control over the D-Echo bit generated in the NT mode device. The default state or the EBITNRM command sets Echo bit to its normal condition which is to reflect the received D bit back out to the TEs as the Echo bit. The EBIT0 command forces the Echo bit to be set to ''0'' on every frame going back to the TEs. The EBITI command forces the transmitted Echo bit to be inverted from that which is computed from incoming D bits.

LOOPBACK TEST MODES

Three classes of loopback mode are available on the SID, selected by writing the appropriate Control instruction.

LBS This loopback at the system interface loops the two B channels and the D channel from the B_x input to the B_r output. It may be set either when the device is activated, in which case it is transparent (i.e. the channels are also transmitted to the line), or when it is deactivated.

LBL1/2 These loopbacks turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1/2 These loopbacks at the Digital System Interface loop the B1 (LBB1) or the B2 (LBB2) channel data from the B_x input to the B_r output. The B_x input data is also sent to the line transmit output.

CAL This command clears all loopbacks.

EXTERNAL SELF-ACTIVATING LOOPBACK

A quick self-test of the device is possible by connecting together the line sides of the transmit and receive transformers. NTA or NTF mode must be selected, and the device can then be activated by the normal command sequence (Note 2).

Note 2: This test mode is not possible by direct connection of $L_o\pm$ and $L_i\pm$ pins due to incompatible internal bias voltages.

MULTIFRAME TRANSMIT AND RECEIVE REGISTERS

MFT1L) MFT1H) MFT2) MFR1) MFR2) MIE1) MID1) MID2) With the device in TE Mode, data entered in M1, M2, M3 and M4 bits of MTF1L is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT Mode, data entered (via MFT1L, MFT1H) in the M bit positions is transmitted towards the TE in multiframe bit positions S11, S12, S13 and S14 respectively. Data entered via MFT2 command in the M bit positions is transmitted in multiframe bit positions S21, S22, S23, S24 respectively. The Multiframe Channel and Interrupts (MFR1, MFR2) must be enabled by the MIE1, MIE2 to use these channels. The MID1, MID2 commands will disable the interrupts MFR1, MFR2 (and in NT mode only, it will also disable the multiframing clock to the TEs). See also the section on Multiframe Maintenance Channel.

MULTIFRAME MESSAGE REPETITION AND VALIDATION

MFC1E) MFC6E) MFC1D) MFC6D) These commands control the frequency of the MFC Interrupt that is used as an aid to the software to transmit multiframe commands. If both MFC1E and MFC6E commands are set, then the MFC Interrupt will occur every multiframe (5 ms). The interrupt may be disabled with MFC1D, MFC6D. The MFC6E command also enables the internal 6 multiframe counter that ensures that every MFT1L command is sent for 6 consecutive multiframes before sending another command loaded in the MFT1L register. The MFC6D also disables the internal 6 multiframe counter. See also the section on Multiframe Maintenance Channel.

ENINT This command enables the RMFE and SLIP interrupts and thus accesses new features of TP3420A.

DISINT Disables RMFE and SLIP interrupts.

ENV) DISV) ENV enables the 3-times validation of certain SC1/Q and SC2 channel messages (Table VII) before generating the MFR1 and MFR2 interrupt respectively. DISV disables this circuit so that the MFR1 and MFR2 interrupts are generated whenever there is a change in the received multiframe word in either channel.

ENST) DISST) ENST enables the state of the internal Activation State machine to be reported to the microcontroller by the NOCST response to any MICROWIRE command thereafter. The DISST causes the NOCST to be replaced by the normal NOC status. See the section on Activation State machine access.

PINDEF This command is used to choose alternate pin functions on Pins 8 and 18. Please see Table I for the selection values.

ACTIVATION STATE MACHINE ACCESS

The TP3420A has a mechanism which allows the microcontroller to read the internal activation state of the chip. The MICROWIRE command ENST (Enable Status) X'92 enables the device state information to be output as a MICROWIRE status word NOCST (1,S3,S2,S1,0,0,0,0) in response to any subsequent MICROWIRE command. However, if a state change interrupt occurs, e.g., an AP (Activation Pending)

Functional Description (Continued)

then the interrupt status value is returned, otherwise the NOCST status is returned. See Table V below to relate the values of the S3, S2, S1 bits to internal activation state of the device.

TABLE V. TP3420A Activation State Table

NT	TE	S3	S2	S1
G1	F1	0	0	0
G1.1	F2	0	0	1
G1.2	F3	0	1	0
G2	F4	0	1	1
—	F5	1	0	0
—	F6	1	0	1
—	F7	1	1	0
G3	F8	1	1	1

A clean way of monitoring the device state is to write a ENST command, followed immediately by a DISST (Disable Status) command. The NOCST status returned at the end of the DISST contains the actual state of the device. Subsequent MICROWIRE commands will be responded by NOC (0,0,0,0,0,0,0,0). This method makes it easy for the software to keep track of when to expect the device state via the NOCST.

Another method would be to repeat the NOP command a couple of times after a ENST command and observe that the device state information (through the NOCST) is repeated to be sure of the state of the device.

IDENTIFYING A TP3420A FROM A TP3420 DEVICE

The TP3420A on power-up default is functionally compatible with a TP3420 device, and hence software written for a TP3420 is applicable for a TP3420A device. Additional device features may be invoked by MICROWIRE commands. A simple way of identifying a TP3420A from a TP3420 is as follows:

Upon application of power, write ENST followed by DISST MICROWIRE commands to the device and evaluate the NOCST status word. If the device is a TP3420A the value should be 1000000, indicating the device is in F1/G0 state. A TP3420 device will ignore the ENST/DISST commands and return the normal NOC (00000000) status back.

MAINTENANCE LOOPBACKS

The TP3420A supports all the ANSI T1.605 and I.430 loopback modes and some additional loopback modes to allow greater flexibility in performing fault isolation.

1) B1 digital loopback (using LBB1 command) with any FSa/FSb relationship in all TE or NT modes.
2) B2 digital loopback (LBB2) with any FSa/FSb relationship in all TE or NT modes.
3) Contiguous B1 + B2 (128 kbit/s) digital loopback (LBB1, LBB2) in TEM mode and in NT/TES modes if FSa is phase synchronous with FSb.
4) Contiguous B1 + B2 + D (144 kbit/s) digital loopback (LBD) in TEM mode and in NT/TES modes if FSa is phase synchronous with FSb.
5) B1 line loopback (using LBL1) with any FSa/FSb relationship in all TE or NT modes.
6) B2 line loopback (using LBL2) with any FSa/FSb relationship in all TE nor NT modes.
7) Contiguous B1 + B2 (128 kbit/s pipe) line loopback (LBL1, LBL2) with equal delay, available in TEM mode, and in NT/TES modes if FSa is phase synchronous with FSb.

Note that a line loopback for the D channel is not specified in the CCITT I.430 or the T1-605 specification, to ensure that D channel signaling is transparently passed end-to-end.

ACTIVATION/DEACTIVATION: TP3420A IN NT MODE

Activation (i.e. transmission and loop synchronization) may be initiated from either end of the loop.

Activation initiated from the NT: to initiate Activation from the NT, the TP3420A must be powered up, using a PUP command, followed (Note 3) by an AR instruction to the Control Register. Network timing, i.e., an 8 kHz input to FS_a, must be present at this time. The device then begins to send data framed as INFO 2 type, in which bits in the B, D and D-echo channels are set to binary 0. These frames are detected by the TE, which replies with data framed as INFO 3 type, synchronized to received frames. A flywheel circuit in the TP3420A NT searches for 3 consecutive correctly formatted receive frames to acquire frame synchronization. If Multiframing is enabled (MIE), 60 correct frames (3 multiframes) are required to achieve full loop synchronization. When it is correctly in sync with received frames, the NT interrupts the control processor with Status Indication type AP. A second AR command is required to cause the NT to send INFO 4 frames, in which the B and D channels are enabled for transmission; Status Indication type AI is then set, and the $\overline{INT}$ output is pulled low to indicate Activation complete.

Note 3: A delay of $\geq$2 msecs is recommended to ensure that all internal circuits have settled.

Activation initiated by a TE: when Activation is initiated by a TE, the TP3420A in NT mode will detect the incoming INFO 1 signal and, if it is powered-down will pull the $\overline{LSD}$ pin and $\overline{INT}$ low, either of which can be used to ''wake-up'' a microprocessor. A PUP command must then be written to power-up the TP3420. Upon identifying the INFO 1 signal, the device will set Status Indication type AP and pull $\overline{INT}$ low to indicate that Activation is pending. No INFO 2 frames will be transmitted until a Control instruction type AR is written to the device, which allows the Activation sequence to proceed as described above.

Once Activated, loss of frame alignment is assumed by the TP3420A when a time which is equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the NT does detect alignment loss it will start to transmit INFO 2. At this point the Error Indication (EI) primitive is set, the $\overline{INT}$ output is pulled low and the receiver searches to identify the incoming signal and attempt to re-acquire loop synchronization. If it successfully re-establishes synchronization with the incoming signal (INFO 3 frames), a further interrupt is generated with Status Indication type AI and re-activation can be completed by sending an AR command. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, Status Indicator EI is set and $\overline{INT}$ pulled low, with the transmitted frames changed to INFO 2. Deactivation can then be completed by a DR command, following which Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

If required, a PDN instruction may be written to the Control Register to power-down the device and enable the LSD output.

Functional Description (Continued)

I.430 recommends 2 timers should be available in an NT. An Activation Request to the TP3420A should be associated with the start of an external Timer 1, if required. Timer 1 should be stopped when the AI interrupt is generated following successful Activation. If Timer 1 expires before AI is generated, however, Control Instruction type DR should be written to the device to force de-activation. Timer 2, which is specified to prevent unintentional reactivation, is not required since the TP3420A can uniquely recognise INFO 1 frames.

ACTIVATION/DEACTIVATION: TP3420A IN TE MODE

Activation initiated by the TE: to activate the loop with the TP3420A at the TE end the device must first be powered-up by a PUP command, followed (Note 3) by a Control Instruction type AR, which is the Activation Request to begin transmission of INFO 1 frames after verifying that INFO 0 is being received from the NT. INFO 1 is a continuous pattern of 0+, 0−, and 6 '1's repeated. At this point the TE is running from its local oscillator and is not receiving any sync information from the NT. When the NT recognises this ''wake-up'' signal, it begins to transmit INFO 2, synchronized to the network clock (following activation of the ''U'' interface, if applicable). This enables the phase-locked loop in the TE's receiver to correctly identify bit timing from the NT and to synchronize its own transmission to that of the NT. On identifying INFO 2 for 3 consecutive frames, the TE changes its transmit data to INFO 3 and awaits the return of INFO 4 from the NT. Identification of INFO 4 completes the Activation sequence, so Status Indication type AI is set, and the $\overline{INT}$ output pulled low.

Activation initiated from the NT: when Activation is initiated by the NT, if the TP3420A in TE mode is powered down, it will pull the $\overline{LSD}$ pin and $\overline{INT}$ low on receiving a line signal. Either of these can be used to ''wake-up'' a microprocessor. A PUP command is required to enable the device to power-up, identify the received signal, and acquire bit and frame synchronization. Once INFO 2 has been identified, the TP3420A will pull $\overline{INT}$ low, with Status Indication type AP set, to alert the microprocessor that Activation is pending. The microprocessor must respond by writing Control Instruction type AR in order for Activation to proceed. INFO 3 frames are then transmitted. Finally, an AI Status Indication interrupt is generated when the NT replies with INFO 4 frames.

As in NT mode, once Activated, loss of frame alignment is assumed by the TP3420A when a time equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the TE does detect alignment loss it will cease transmitting immediately. At this point the Error Indication (EI) primitive is set in the Status Register, the $\overline{INT}$ output is pulled low and the receiver searches to re-acquire loop synchronization if INFO 2 or INFO 4 frames are still being received. If synchronization is re-established, a further interrupt is generated, with Status Indication type AI. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated, Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

I.430 does not provide for Deactivation to be initiated by a TE. However, a Power-down state may be forced if required, normally after Deactivation has been established by the network.

If required, an external Timer 3 should be started when an Activation Request is sent to the TP3420. The subsequent AI interrupt, indicating Activation is complete, should be used to stop the timer. If the timer expires before an AI is generated, Control Instruction type DR must be written to the device to force the transmission of INFO 0.

TE MODE D-CHANNEL ACCESS

In TE Master mode and optionally in TES mode, the TP3420A SID arbitrates access for Layer 2 Transmit frames to the D-channel bit positions in accordance with the I.430 Priority Mechanism (I.430 Section 6.1). This mechanism is to resolve contention for the D channel towards the network when 2 or more TEs are connected to a Passive Bus. The shifting of D-channel transmit data from the Layer 2 device into the SID buffer is controlled by gating the DEN_X output with BCLK. When no Layer 2 frame is pending, ''1''s are always transmitted by the SID in D-bit positions at the S interface. DEN_X output pulses are inhibited and no D-channel data is shifted into the B_X input. An external Layer 2 device requiring to start transmission of a packet should first prime its Transmit buffer such that the opening flag is ready to be shifted across the digital interface. Then a DREQ command will initiate the D-channel access sequence. DREQ commands require either that a Priority Class 1 (signalling) packet, or a Priority Class 2 packet, is selected.

In response to the DREQ command, the DEN_X output is enabled to pre-fetch the opening flag from the Layer 2 device into the D-channel buffer. (Note: it is not necessary to flush the Layer 2 HDLC transmitter prior to clocking out the opening flag; the TP3420A will continue the pre-fetch until the flag is uniquely recognized.) Meanwhile, the Priority Counter checks that no other TE connected to the S interface (in a point-to-multipoint wiring configuration) is transmitting in the D-channel. This is assured by counting consecutive ''1''s in the E-bit position of frames received from the NT. At least 8 consecutive ''1''s must be detected before transmission of the pending D-channel frame begins, in accordance with Table VI.

TABLE VI. D-Channel Access Criteria

Number of Consecutive ''1''s in the E-Channel	D-Channel Access
7	Abort. Possible re-try by the transmitting TE.
8	Signalling packet (Priority Class 1) may begin (Note 1).
9	Signalling packet may begin unconditionally.
10	Any packet type may begin (Priority Class 2) (Note 2).
11	Any packet type may begin unconditionally

Note 1: Only if, since the SID last transmitted a complete Class 1 packet, a sequence of $\geq$ 9 consecutive ''1''s has been detected in the E-channel.

Note 2: Only if, since the SID last transmitted a complete packet of either class, a sequence of $\geq$ 11 consecutive ''1''s has been detected in the E-channel.

If another TE is active in the D-channel, DEN_X pulses are inhibited once the opening flag is in the Transmit buffer, to prevent further fetching of transmit data from the Layer 2 device until D-channel access is achieved. As soon as the

Functional Description (Continued)

required number of consecutive E-channel ''1''s has been counted, the leading 0 of the opening flag is transmitted in the next D-bit position towards the NT. DEN_x pulses are also re-enabled in order to shift D-channel bits from the Layer 2 device into the SID transmit buffer. No interrupts are necessary for local flow control between the Layer 2 processor and the TP3420.

During transmission in the D-channel the TP3420A SID continues to compare each E-bit received from the NT with the D-channel bit previously transmitted before proceeding to send the next D-bit. In the event of a mis-match, a contention for the previous D-bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and ''1''s are transmitted in all following D-bit positions. Status Indication type CON is set, and the $\overline{INT}$ output is pulled low to interrupt the Layer 2 transmit processor. DEN_x output pulses are again inhibited.

In order to retransmit the lost packet, the Layer 2 device must begin as before, by priming its Transmit buffer with the packet header and writing a DREQ command into the Control Register.

DEN_x pulses stop immediately after receiving the closing flag on the B_x input from the layer 2 device.

Successful completion of a transmit packet is detected by the TP3420A when the closing flag is transmitted in the D channel. '1's are then transmitted in the following D bit positions. The $\overline{INT}$ output is pulled Low (if enabled), with Status Indication type EOM set, to indicate the End of Message. Also, the Priority Access counters are decremented to the lower priority level within each priority class, in accordance with the I.430 algorithm. Priority is subsequently restored to the higher level when the specified number of consecutive 1's (9 or 11) is detected in the D-echo-bit position.

D-CHANNEL ACCESS ALGORITHM IN TES MODE

Two MICROWIRE commands in the TP3420A provide the option of enabling or disabling the D channel access algorithm, for Passive Bus applications while in the TES and TEM mode. An example of this would be for support of passive bus off a PBX trunk line. The commands are DACCE (Access Algorithm Enable) and DACCD (Access Algorithm Disable). The power-up default condition for TES mode is to disable the D channel access mechanism, and for TEM mode is to enable the D channel access mechanism.

ECHO-BIT CONTROL IN NT MODE

For certain applications it is desirable to be able to control the E-bit sent from the NT device towards the TE. Three MICROWIRE commands are provided to control this. The EBIT0 command forces the E bit to 0 continuously to simulate the effect of a busy D channel. The D channel access algorithm can be verified by releasing the E-bit control using the EBITNRM command. Alternatively, it is possible to invert the outgoing E-bit from the actual computed E-bit within the NT (EBITI). This method too has the effect of forcing the D-channel to appear busy. The EBITNRM command is again used to set the E-bit control back to normal condition.

INVERT B1 AND B2 DATA CHANNELS TO OPERATE OVER RESTRICTED FACILITIES

On ''restricted'' network transmission facilities (such as certain T1 links), the transmission of an ''all ZEROs'' octet is not permitted. So, the data originating from a TE has to be restricted.

The HDLC protocol inherently restricts the number of contiguous ''1''s to 7, as in the abort character (11111110). An idle HDLC channel is filled with ''1''s, repeated aborts or repeated flags (01111110). On operation over restricted facilities, the idle character must NOT be continuous ''1''s, but can be aborts or flag characters. This ensures that the maximum contiguous ''1''s is restricted to 7. By inverting the entire HDLC bit stream (''1''s with ''0''s), the data contains a maximum of 7 contiguous ''0''s which can then be transferred across the network having restricted facility links.

Data in each of the B channels can be inverted independently with the use of the INVB1 and INVB2 commands. The data is inverted in both transmit and receive directions in a B channel. The NRMB12 command resets the B1 and B2 channel data stream to normal operation. The D channel data is always considered to be using unrestricted facilities and does not need to provide an inverted bit stream.

MULTIFRAME MAINTENANCE CHANNELS (SC1, SC2 AND Q WORDS)

Each direction of transmission across the S interface includes low-speed (800 bit/s) channels for loop maintenance, accessed through the control interface of the TP3420A. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table VII. One word is transmitted downstream (NT-to-TE) in the SC1 sub-channel 1, and one word is transmitted upstream (TE-to-NT) in the complementary Q channel every multiframe. There are 4 additional sub-channels (each of 800 bits/s) SC2, SC3, SC4 and SC5 allocated in the downstream direction.

The 1991 version of ANSI T1.605 defines the use of only the SC1 and SC2 in the NT to TE direction (Section 8.6 of ANSI T1.605-1991), and the Q channel in the TE to NT direction. It also adds a distinction between high and low priority messages in the SC1/Q channel. The SC1/Q channels are complementary channels used to perform loop maintenance functions. The Q channel is used by a TE to request maintenance modes (such as loopbacks) and the SC1 channel is used by the NT to respond to the requests. Messages transferred through these channels must be assigned either as high priority or low priority, which determines the order of transmission. The TP3420A provides hardware support to handle these messages. SC2 is an additional information channel in the NT to TE direction, supplying line condition status of the network to the TEs.

The use of any of the channels is optional and may be enabled individually.

CONTROL OF MULTIFRAMING CLOCK AND INDICATION

With the device in NT mode, the MIE1 (or the MIE2) command enables the transmission of the Multiframe identification algorithm (reversal of the FA/N bits every 5th frame and the M bit set to ''1'' every 20th frame) and enables the MFR1 (or the MFR2) interrupts. The algorithm is present during INFO 2 and INFO 4 frames. In TE modes the MIE1 (or the MIE2) command only enables the MFR1 (or the MFR2) interrupt, since the device will always search for and synchronize to the multiframing identification bits if the NT is sending them.

Functional Description (Continued)

The MID1 and MID2 commands disable the transmission of the Multiframe identification algorithm in NT mode and disable the MFR1 and MFR2 interrupts in both NT and TE modes. The MIE1, MIE2, MID1 and MID2 commands should only be written to the device when it is deactivated (either power-up or powered down). The Multiframe Transmit Registers should also be loaded with the appropriate ''Idle'' messages before activation, by means of the MFT1L and MFT2 instructions.

VALIDATION OF RECEIVED MULTIFRAME MESSAGES

The TP3420A includes logic to validate incoming SC1/Q and SC2 messages for the specified number of consecutive receptions before generating the MFR1 or MFR2 interrupts. The validation of the received messages is enabled with ENV command and disabled with the DISV command. If enabled by the ENV command, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR1 interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word.

The validation algorithm implemented in the TP3420A conforms to the ANSI T1.605-1991 specification and is indicated in Table VII. When a 3x message is received an interrupt is generated after 3 complete consecutive and identical multiframe words have been received. No more interrupts will be generated until the received message changes. Some messages (such as FECV, LOP) have to be validated only once to generate the MFR1 interrupt. All undefined codes in SC1/Q are validated 1 time and reported to the CPU with the MFR1 interrupt. All SC2 messages (defined or undefined) are validated 3 times before generating the MFR2 interrupt.

If the 3x checking is disabled by the DISV command, a change in the received SC1, SC2 or Q word generates MFR1 or MFR2 interrupts.

Note, however, that no other action is taken by the TP3420A in response to received SC1, SC2 or Q channel codes (e.g. loopbacks are not automatically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constraints from the device, and to use the unassigned codes for other functions.

SC1/Q Transmit Registers

For both NT and TE modes, the TP3420A has two registers to transmit a SC1/Q channel message through two MICROWIRE commands: MFT1L and MFT1H. Normally the message in MFT1L is transmitted continually. However a high priority message may be loaded in the MFT1H register and transmitted once only. The MFT1H register is double buffered so that it can accept two message loads within 5 ms, but not more than 3 messages within 10 ms.

A 6x multiframe counter (30 ms) in the TP3420A is enabled by the MFC6E command, and disabled with the MFC6D command. When the counter is enabled (MFC6E), an interrupt MFC is generated locally every 30 ms and internal logic ensures that the MFT1L messages are transmitted 6 times unless interrupted by an MFT1H message.

Alternatively, if the software chooses to keep count of repetitions of transmitted multiframe messages, the command MFC1E can be used to cause the interrupt MFC at every multiframe boundary (5 ms). The 6x transmit logic is then disabled. If both MFC6E and MFC1E commands are loaded, the MFC1E command has precedence and causes the 1x (5 ms) interrupt. It is expected that the user will prefer the 30 ms interrupt to control transmission of multiframe messages because it reduces the processor load considerably, as outlined below and in examples in the Appendix A.

Software Table of SC1 Messages

The software in the NT should keep a table of SC1 messages to be communicated to the TE, and use the MFC (30 ms) interrupt as a synchronous timer to load SC1 messages. Using X'3X command for SC1 messages, the software must write the appropriate Low Priority message to the MFT1L register within 30 ms of the interrupt. The message is then transmitted on the next 6x multiframe boundary and is repeated 6 times. If the MFT1L register is not updated by a new MICROWIRE command from the CPU within 30 ms, the data from the MFT1L register is re-transmitted another 6 times.

Transmission of SC1H - High Priority Messages

In the NT mode, commands such as LP, FECV, and DTSE are considered to be High Priority messages. These are loaded through the MFT1H register and sent out once on the next multiframe boundary. In the following multiframe this message gets replaced with the contents of MFT1L, the Low Priority Register. At every multiframe boundary, the device checks whether the MFT1H register has a new message; if it has, that message is sent once, otherwise the contents of the MFT1L register are sent.

In TE modes on the receive side, the high priority messages on the SC1 channel (LP, ST, FECV and DTSE) are accepted as valid on the first occurrence and the MFR1 interrupt is generated to indicate the status (see Table VII).

Transmission of QH - High Priority Messages

In TE modes, a Loss of Power condition is conveyed to the NT by writing the LP command in the MFT1H register for a ''one shot'' high priority message which overrides any other Q channel message. Write the LP message in the MFT1L register to ensure continuing transmission of the LP messages. Normal maintenance commands such as LB1 Request are written to the MFT1L register.

SC2 Channel Messages

With the MFC6E enabled, the TP3420A guarantees the 6x transmission of SC2 messages according to the ANSI 1991 spec. The software should load an SC2 message in to the MFT2 register within 30 ms of the MFC interrupt. The multiframe word for the SC2 stream is then transmitted on the next 6x boundary and repeated 6 times. If the register is not updated by another MFT2 message within 30 ms, then the device will re-cycle the existing message in the SC2 register, i.e. re-transmit it 6 times.

Functional Description (Continued)

TABLE VII
Codes for SC1, SC2 and Q Channel Messages with 3X Checking Enabled

SCI Messages	NT-to-TE					TE-to-NT				
	Received at TE				Number of Repetitions before MFR1 $\overline{INT}$	Received at NT				Number of Repetitions before MFR1 $\overline{INT}$
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (NORMAL)	0	0	0	0	3	1	1	1	1	3
LP Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Self Test Pass	0	0	1	0	3	—	—	—	—	—
STF Self Test Fail	0	0	0	1	3	—	—	—	—	—
ST Self Test Request (Note 1)	—	—	—	—	—	0	0	0	1	3
STI Self Test Indication	0	1	1	1	3	—	—	—	—	—
FECV Far End Code Violation	1	1	1	0	1		—			—
DOI Disruptive Operation Indication	0	0	1	1	3		—			—
DTSE-IN	1	0	0	0	1	—	—	—	—	—
DTSE-OUT	0	1	0	0	1	—	—	—	—	—
DTSE-IN&OUT	1	1	0	0	1	—	—	—	—	—
Loopbacks										
LB1 Request	—	—	—	—	—	0	1	1	1	3
LB1 Indication	1	1	0	1	3	—	—	—	—	—
LB2 Request	—	—	—	—	—	1	0	1	1	3
LB2 Indication	1	0	1	1	3	—	—	—	—	—
LB1/2 Request (Note 2)	—	—	—	—	—	0	0	1	1	3
LB1/2 Indication	1	0	0	1	3	—	—	—	—	—
Loss-of-Received-Signal Indication	1	0	1	0	3	—	—	—	—	—
Unassigned	All Other Codes				1	All Other Codes				1
	Received at TE				Number of Repetitions before MFR2 $\overline{INT}$					
	S21	S22	S23	S24						
All SC2 Messages	All Codes				3					

Note 1: The code ''0001'' will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Note 2: The code ''0011'' will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.

Functional Description (Continued)

BIPOLAR VIOLATION DETECTION AND FECV MESSAGING VIA THE SC1 CHANNEL

NT Mode

A Receive Multiframe Error (RMFE) detector circuit in the TP3420A identifies any multiframes in which one or more bipolar violations is received, indicating a bit in error. If one or more line code violation errors occur in a received multiframe (5 ms), the TP3420A generates the RMFE (Receive Multiframe Error) interrupt. The microcontroller has to send the Far End Code Violation, FECV (1110) word over the SC1 channel through the MFT1H register. The FECV message is then sent once, after which the SC1 channel reverts to sending the message from the MFT1L register.

The RMFE circuit detects frame code violations in 16 frames (out of 20 frames in the multiframe) not containing the multiframe Q bit data and detects correct DC balancing in all 20 frames, including the frames containing the multiframe data. The RMFE detector is operational whether multiframing messaging is used or not. The RMFE interrupt is disabled by default on power-up. It is normally enabled after activation is completed by writing the ENINT command.

TE Mode

When the TE end device receives an FECV message in the SC1 channel, it is validated on a single occurrence, and the device generates the MFR1.

If one or more line code violation errors occur in the received multiframe, the device will generate the RMFE interrupt. The microcontroller may then keep a count of frame errors being received. Currently, there is no provision in T1-605 for informing the NT about the errors received at the TE end.

The RMFE circuit detects frame code violations as well as DC balancing in all 20 frames in the multiframe. In the TE received frames, the S bit (for SC1, SC2, etc.) is independent of the auxiliary framing pulses. The RMFE detector is operational whether multiframing messaging is used or not. The RMFE interrupt is disabled by default on power-up. It is normally enabled after activation is completed by writing the ENINT command.

Applications Information

While the pins of the TP3420A SID are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

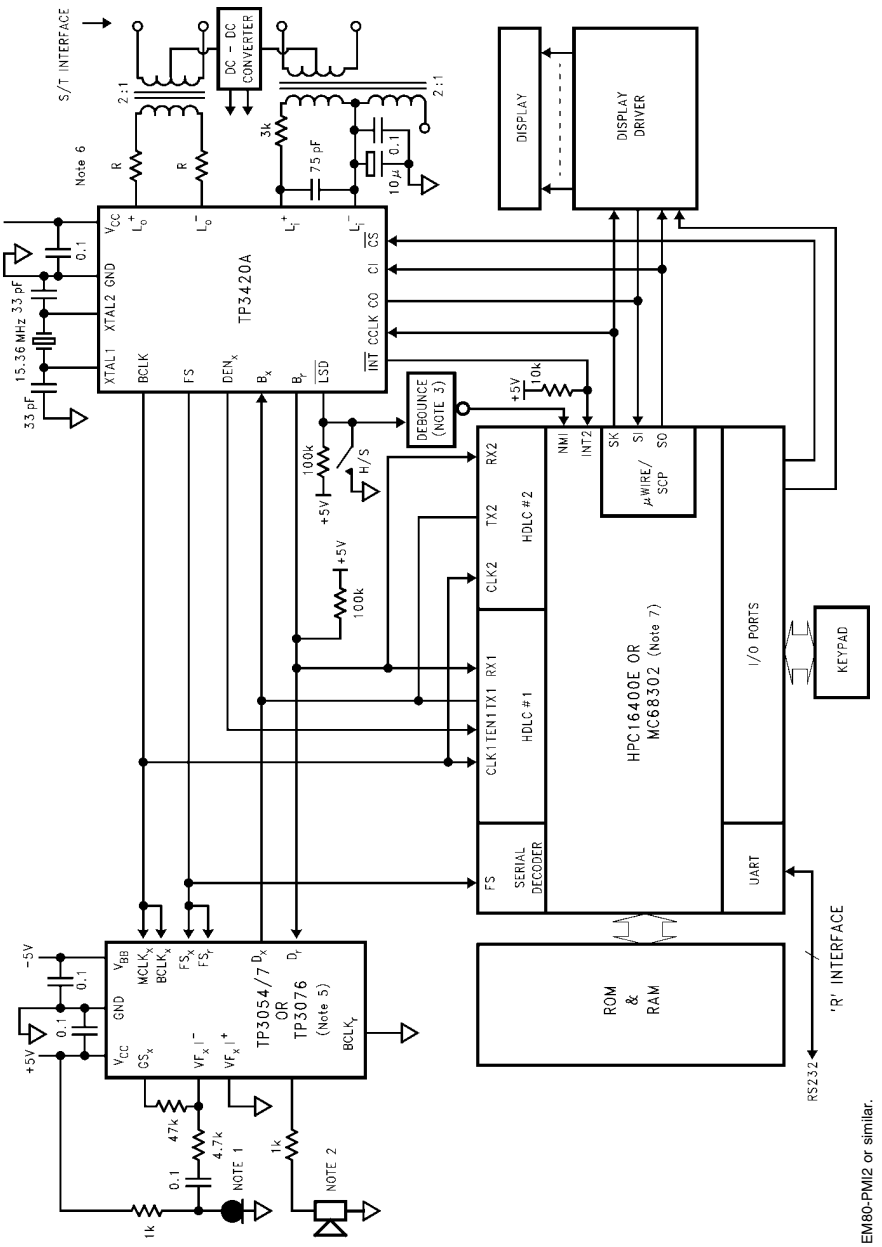
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 0.1 μF should be connected from this common point to V_{CC}. Taking care with the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

1. keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components.
2. keep the connections between the device and the components on the $L_i\pm$ inputs short; the L_i- capacitors should be connected close to the device pins.
3. keep the connections between the device and the transformers short.

Figure 5 shows a typical application of the TP3420A in an ISDN Terminal.

For more in-depth information on a variety of applications, Application Note AN665 is a comprehensive guide to the hardware and software required to meet the I.430 interface specification. Performance measurements, demonstrating compliance with I.430 and ANSI transmission requirements, are also included. For additional information on firmware for the maintenance message channels see Appendix A of this datasheet.

Typical Applications



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Note 1: Primotype EM80-PMI2 or similar.
Note 2: Primotype DH31 or similar.
Note 3: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.
Note 4: See TP3420A User's Manual for Line Interface Protection.
Note 5: The TP3076 Programmable Combos also require the MICROWIRE Port to be connected.
Note 6: R = 22Ω when using a PE64995 transmit transformer and a connecting cord. See AN-872 (TP3420A Line Interface Circuit Considerations) for more details.
Note 7: See additional applications note for detailed connections to MCG8302.

FIGURE 5. Typical Application in a TE and/or TA

Typical Applications (Continued)

POPULAR MICROWIRE FORMATS

The TP3420A enhanced MICROWIRE port supports two popular formats used in typical terminal equipment applications.

1) CCLK idling LOW when the $\overline{CS}$ pin is inactive HIGH, pulsing LOW/HIGH/LOW for 8 clocks then returning back to LOW for idle condition. Data is output on the CO pin on the negative edge and data is sampled in on the positive edge of CCLK. This format (shown in *Figure 6a*) is normally used with NSC's microcontrollers from the HPC or the COP8 family.

2) CCLK idling HIGH when the $\overline{CS}$ pin is inactive HIGH, pulsing HIGH/LOW/HIGH for 8 clocks, then returning back to HIGH for idle condition. Data is output on the CO pin on the negative edge and data sampled in on the positive edge of CCLK. This format (shown in *Figure 6b*) is normally used with other alternate microcontrollers in the industry.

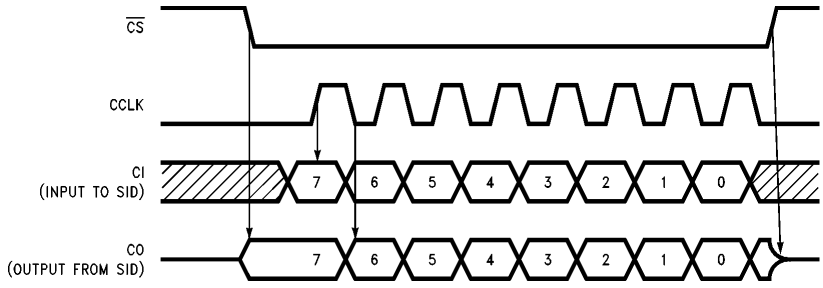

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FIGURE 6a. TP3420A Normal MICROWIRE Clock Format

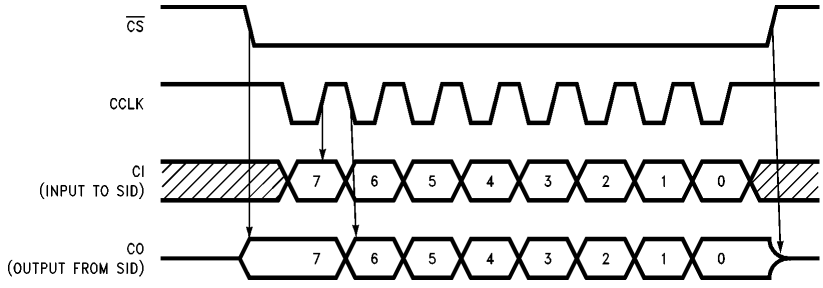

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FIGURE 6b. TP3420A Alternate MICROWIRE Clock Format

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_0	V_{CC} + 1V to GND − 1V
Voltage at any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to +150°C
Current at L_0	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating	2000V

Electrical Characteristics

Unless otherwise noted: limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5%, and T_A = 0°C to 70°C. This data sheet is still preliminary and parameter limits are subject to change based on further characterization testing.

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs	**2.2**			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Input	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	B_r, I_L = 3.2 mA All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	B_r, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA All Outputs, I_L = −100 μA	**2.4** **2.4** **V_{CC} − 0.5**			V V V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	B_r, $\overline{INT}$, $\overline{LSD}$, CO GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
R_{Li}	Differential Input Resistance	GND < L_i+, L_i− < V_{CC}	200			kΩ
CL_{L0}	Load Capacitance	Between L_o+ and L_o−			200	pF
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	All Outputs Open-Circuit			1.20	mA
$I_{CC}1$	Power Up Current	As Above, Device Deactivated (Note 1)			25	mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude	R_L = 270Ω Between L_o+ and L_o− (Note 2)	**±1.90**		**±2.14**	Vpk
	Transmit Pulse Unbalance	0+ Relative to 0−			**±5**	%
	Input Pulse Amplitude	Differential Between L_i+ and L_i−	**±175**			mVpk
	Output Impedance when Transmitting Binary Zeroes	50Ω Load	100			Ω
		400Ω Load (Note 3)		14		Ω

Note 1: When the device is activated and driving a correctly terminated line, I_{CC1} increases by several mA. A worst-case data pattern, consisting of all binary 0's, increases I_{CC1} by approximately 8 mA.

Note 2: The pulse amplitude at the L_o± pins allows for approximately 1 dB transformer insertion loss to meet the 0.75V pulse mask test when the line is terminated in 50Ω.

Note 3: Using a 2:1 PE64995 transformer and a connecting cord. See AN-872 (TP3420A Line Interface or Circuit Considerations) for more details.

Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MCLK SYSTEM CLOCK (See *Figure 4*)						
F_{MCK}	Master Clock Frequency Master Clock Tolerance		 −100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
t_{MH}, t_{ML}	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	**20**			ns
t_{MR}, t_{MF}	Rise and Fall Time of MCLK	Used as a Logic Input			**10**	ns
MICROWIRE CONTROL INTERFACE (See *Figure 4*)						
t_{CH}	CCLK High Duration		**50**			ns
t_{CL}	CCLK Low Duration		**50**			ns
t_{SIC}	Setup Time, CI Valid to CCLK Edge		**30**			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		**20**			ns
t_{DCSO}	Delay Time from $\overline{CS}$ Low to CO Valid	Bit C7 only			50	ns
t_{DCO}	Delay Time from CCLK Edge to CO Data Valid				50	ns
t_{DCSZ}	Delay Time from $\overline{CS}$ High to CO TRI-STATE				30	ns
t_{SCSC1}	Setup Time, from $\overline{CS}$ Low to CCLK Edge High		30			ns
t_{HCSC1}	Hold Time, $\overline{CS}$ High from CCLK Edge High		**40**			ns
t_{HCSC2}	Hold Time, $\overline{CS}$ Low from CCLK Edge High		**50**			ns
t_{SCSC2}	Setup Time, $\overline{CS}$ High to CCLK Edge High		**50**			ns
t_{CSH}	Duration of $\overline{CS}$ High		1			μs
t_{DCI}	Delay Time $\overline{CS}$ Low to $\overline{INT}$ High-impedance				**250**	ns
DIGITAL SYSTEM INTERFACE (See *Figure 7*)						
F_{BCK}	Bit Clock Frequency		256		4096	kHz
t_{BH}, t_{BL}	Clock Pulse Width Hi & Low for BCLK	$V_{IH} = 2.2V$ $V_{IL} = 0.7V$	**60**			ns
t_{BR}, t_{BF}	Rise and Fall Time of BCLK				15	ns
$t_{FSa/b}$	Frame Sync Frequency			8		kHz
t_{SBC}	Set up Time, B_x Valid to BCLK Low	All Modes	**30**			ns
t_{HCB}	Hold Time, B_x Valid from BCLK Low	All Modes	**20**			ns
t_{DCD}	Delay Time, BCLK Transition to DTCK Transition	TEM, DCKE Mode	0		40	ns
t_{SDT}	Setup Time, TxD Valid to BCLK Low	TEM, DCKE Mode	30			ns

Timing Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL SYSTEM INTERFACE (See *Figure 7*) (Continued)						
t_{HDT}	Hold Time, BCLK Low to TxD Invalid	TEM, DCKE Mode	20			ns
t_{HCFH}	Hold Time, BCLK High to FS_a and FS_b High (Inputs)	NT and TES Modes only	**0**			ns
t_{SFC}	Set up Time, FS_a and FSb Inputs to BCLK Low	NT and TES Modes only	**50**			ns
t_{HCFL}	Hold Time, BCLK Low to FS_a and FS_b Low (Inputs)	NT and TES Modes only	**20**			ns
t_{DBFR}	Delay Time, FS_b Input to B_r Valid	NT and TES Modes, Bit 1 only			**80**	ns
t_{DBF}	Delay Time, BCLK High to FS_a and FS_b Transitions (Outputs)	TEM mode only			**50**	ns
t_{DCB}	Delay Time, BCLK High to Data Valid	All Modes			**80**	ns
t_{DCBZ}	Delay Time, BCLK Low to Data Invalid	All Modes (Last Bit Only)	10*		**120**	ns
t_{DCD}	Delay Time, BCLK High to DEN_x Transition	TEM Mode only			**40**	ns

* This parameter can be extended by connecting a 10 kΩ pull-up resistor and a 10 pf pull-down capacitor to B_r.

Timing Diagrams

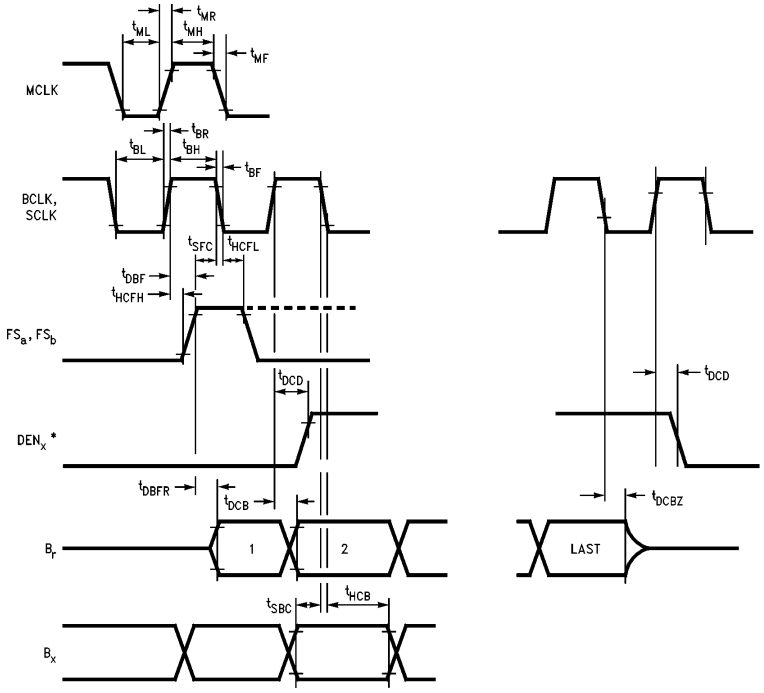

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FIGURE 7. Timing Details for Digital System Interface

Timing Diagrams (Continued)

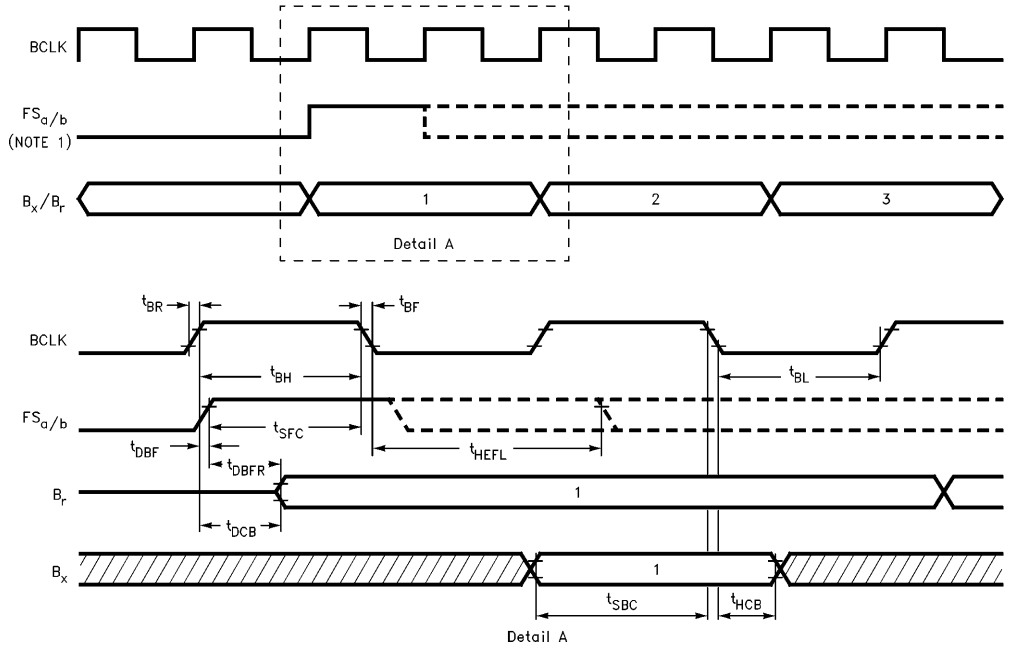

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FIGURE 8. Timing Details for Digital System Interface

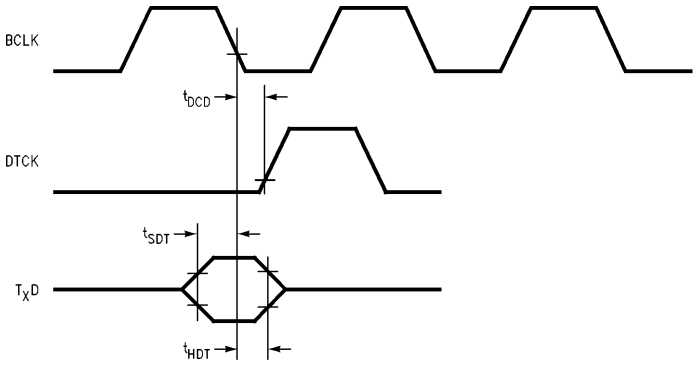

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FIGURE 9. Timing Details for TEM, DCKE Mode

Definitions and Timing Conventions

DEFINITIONS

V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as t_{Dxxyy}[|H|L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

Appendix A

FIRMWARE GUIDELINES FOR HANDLING SC1/Q AND SC2 MAINTENANCE MESSAGES

This application note describes software guidelines that make use of TP3420A hardware features designed to support the handling of the newly defined maintenance channels SC1/Q and SC2. Please refer to the TP3420A datasheet and the T1.605-1991 specification for explanations of the SC1/Q and SC2 messages.

SC1 TRANSMITTER CONTROL IN NT UNIT

The microcontroller software must keep a list of flags for SC1 messages of lower priority that need to be sent for 6 frames, in the following priority order as they occur: ST reports, LB indications, LRS, DOI, IDLE. These messages should be sent through the MFT1L register. The software should also keep a list of flags for the high priority messages that have to be sent once in the following priority order: LP, FECV, and DTSE commands. These messages should be sent through the MFT1H register. As part of the TP3420A initialization, the software should write the MFC6E command to cause the device to generate the MFC interrupt every 30 ms, and this interrupt status should be used to synchronize the SC1L and any SC2 messages.

Events and conditions that cause SC1 messages to be generated arise from 3 different sources, the S interface loop, the U interface loop or from within the NT unit itself. S Loop conditions can cause the RMFE indication to indicate a code violation that must be reported to the TE by the FECV message. U loop conditions are communicated to the TE by the LRS, DOI and the DTSE messages. The NT local microcontroller will generate the messages for the ST reports, LB indications, LP and the IDLE.

Each 30 ms tick, the software should service the list of flags and go down the priority chain. The command (for MFT1L register) corresponding to the highest flag is sent to the MFT1L register and the flag is reset. The MFT1L commands may be updated at every 30 ms tick if any of the relevant flags are set. If a DTSE interrupt is received from the U interface, this command is immediately loaded into the MFT1H register. Similarly, a local RMFE interrupt should be responded with a FECV command through the MFT1H register immediately. A double buffer has been implemented in the MFT1H register to ensure that 2 commands can be queued and each will be sent for 1 multiframe. The device has 2 4-bit register FIFOs. At every multiframe boundary, MFT1H FIFO is checked to see if it contains new data; if yes the data is sent out from the MFT1H FIFO, if not, then the data from the MFT1L register is sent.

If both the buffers are full, then a third load to the MFT1H register will cause the first buffer to be overwritten by the second and the second buffer to be loaded with the third load. This way if a DTSE and FECV are already loaded, and the power on the NT1 starts to fail, the software can still write a LP command in the MFT1H register as well as the MFT1L register. This ensures that the commands will be sent out at the earliest moment and will continue until the power is completely lost.

Whenever a MFT1H command is written, a software flag FL__EXT (extend SC1L) should be set. This flag informs the software that 1 occurrence of the present 6x repetition of the SC1L messages was overwritten by a message from SC1H, and hence it is necessary to extend the MFT1L command for another 30 ms to guarantee 6x tranmission. This flag is reset after the next 30 ms tick.

Example

Assume Software flags and buffers are defined as:

SC1L__PB - software variable, indicating previous data sent via the SC1L channel
SC1L__NB - software variable, indicating the next value to be sent via the SC1L channel
FL__EXT - Flag to Extend SC1L command for another 30 ms.
MFT1L, MFT1H and MFT2, are the device registers.

The sequences of events shown below indicate activity on the SC1 channel on the line and the actions required by the local microcontroller at each 30 ms (MFC status interrupt) ticks.

SC1 Messaging Sequence

Time (ms)	SC1 I430 Frame Content	Actions Required
0 (MFC INT)	(IDLE)	if FL__EXT flag not set, check for new flags on SC1L, assume LRS. Check for SC2 channel. Send SC2 command > MFT2. SC1__NB(IDLE)> SC1__PD, SC1 command(LRS) > SC1__NB, SC1__NB(LRS) > MFT1L.
5	(IDLE)	
10	(IDLE)	
15	(IDLE)	
20	(IDLE)	
25	(IDLE)	

Appendix A (Continued)

Time (ms)	SC1 I430 Frame Content	Actions Required
0 (MFC INT)	(LRS)	if FL__EXT flag not set, check for new flags on SC1L, assume IDLE. Check for SC2 channel Flags. Send SC2 command as appropriate. SC1__NB(LRS) > SC1__PB, SC1L command(IDLE) > SC1__NB, SC1__NB > MFT1L(IDLE).
5	(LRS)	
10	(LRS)	Assume DTSE-IN Interrupt from UID, Send DTSE > MFT1H register. Set the FL__EXT. SC1L__PB > MFT1L (LRS).
15	(DTSE)	
20	(LRS)	RMFE in Interrupt from local SID, FECV > MFT1H, SC1L__PB > MFT1L(LRS). Set FL-EXT.
25	(FECV)	
0 (MFC INT)	(LRS)	if FL__EXT flag set, do not check for new flags on SC1L, but check for SC2 channel. Reset FL__EXT. Send SC2 command as appropriate, SC1L__NB (IDLE) > MFT1L.
5	(LRS)	
10	(LRS)	DTSE-IN Interrupt from UID, DTSE > MFT1H register. Set FL__EXT, SC1L__PB > MFT1L register. Also RMFE in Interrupt from local SID, FECV > MFT1H register. Set FL__EXT. SC1L__PB > MFT1L register. Now the FECV command is queued in the MFT1H register.
15	(DTSE)	
20	(FECV)	
25	(LRS)	
0 (MFC INT)	(LRS)	if FL__EXT flag set, do not check for new flags on SC1L, but check for SC2 channel. Reset FL__EXT. Send SC2 command as appropriate. SC1L__NB (IDLE) > MFT1L
5	(LRS)	
10	(LRS)	
15	(LRS)	
20	(LRS)	
25	(LRS)	
0 (MFC INT)	(IDLE)	if FL__EXT flag not set, check for new flags on SC1L, assume LB1I. Check for SC2 channel. Send SC2 command as appropriate. SC1__NB(IDLE) > SC1__PB, SC1 command (LBL1I) > SC1__NB, SC1__NB(LB1I) > MFT1L.
5	(IDLE)	
10	(IDLE)	
15	(IDLE)	
20	(IDLE)	
25	(IDLE)	

Appendix A (Continued)

Time ms	SC1 I430 Frame Content	Actions Required
0 (MFC INT)	(LB1I)	if FL__EXT flag not set, Check for new flags on SC1L assume LB2I. Check for SC2 channel. Send SC2 command as appropriate. SC1__NB(LB1I) > SC1__PB, SC1 command(LB2I) > SC1__NB, SC1__NB(LB2I) > MFT1L
5	(LB1I)	
10	(LB1I)	
15	(LB1I)	
20	(LB1I)	
25	(LB1I)	
0 (MFC INT)	(LB2I)	if FL__EXT flag not set, check for new flags on SC1L, assume IDLE. Check for SC2 channel. Send SC2 command as appropriate. SC1__NB(LB2I) > SC1__PB, SC1 command (IDLE) > SC1__NB SC1__ NB(IDLE) > MFT1L.
5	(LB2I)	
10	(LB2I)	
15	(LB2I)	
20	(LB2I)	
25	(LB2I)	
0 (MFC INT)	(IDLE)	etc.

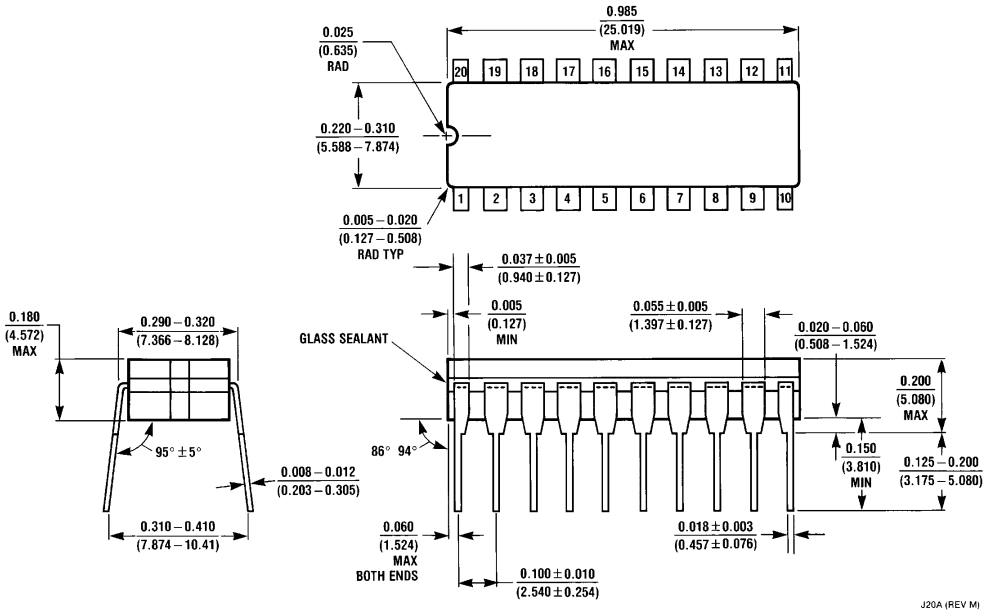
On the **TE receive side,** the LP, DTSE and FECV messages are checked once, and for **every occurrence an interrupt is generated**. The other messages are validated 3 times before an interrupt is generated. Subsequent repetitions of the command do not cause an interrupt.

SC2 CHANNEL TRANSMITTER HANDLING

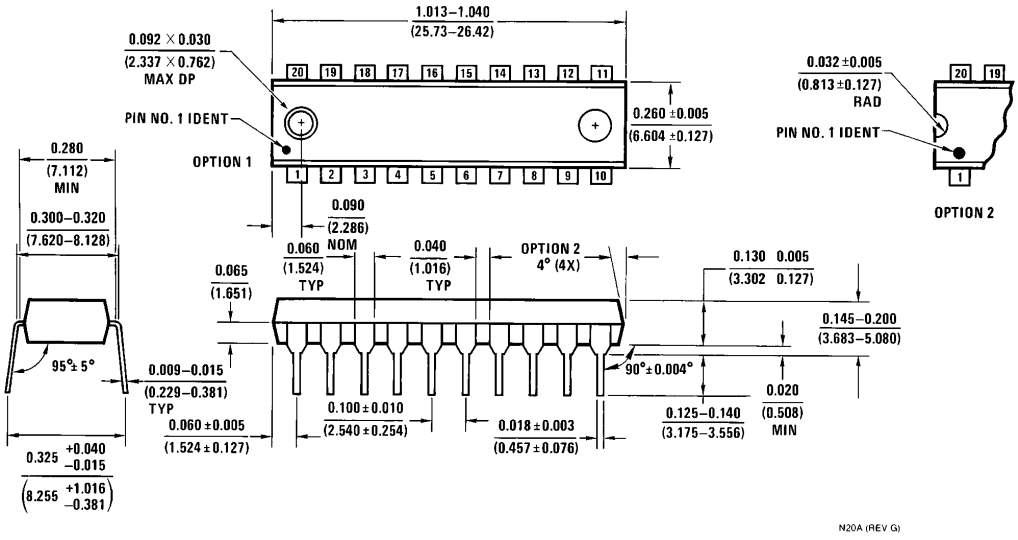
The software should keep a list of flags to indicate SC2 commands as defined in the spec. At the 30 ms tick MFC INT, the software should scan through the list of flags (top down) and, seeing the first flag, should write the appropriate command in the MFT2 register and keep the value in SC2__NB (software buffer).

On the **TE receive side**, the SC2 command is verified 3 times before an Interrupt is generated. Subsequent repetitions of the command do not cause an interrupt.

Physical Dimensions inches (millimeters)

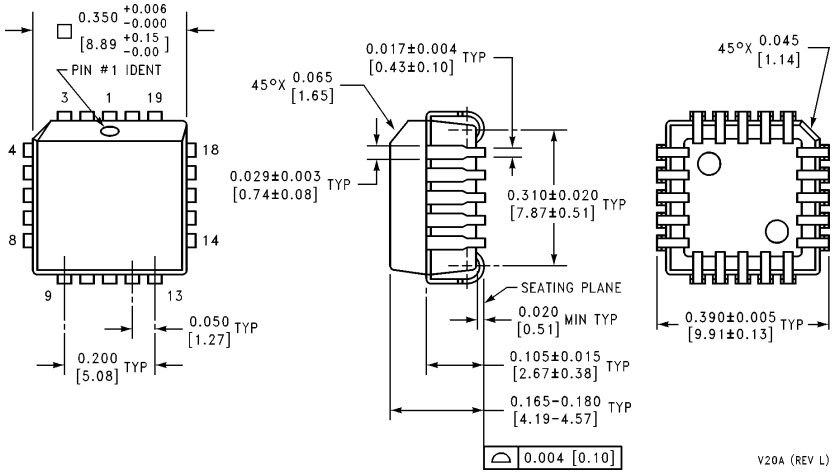


Ceramic Dual-In-Line Package (J)
Order Number TP3420AJ
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number TP3420AN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Order Number TP3420AV
NS Package Number V20A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408