National Semiconductor

September 1995

# LM6164/LM6264/LM6364
# High Speed Operational Amplifier

## General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

VIP™ is a trademark of National Semiconductor Corporation.

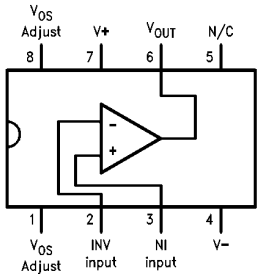
## Features

- High slew rate 300 V/μs
- High GBW product 175 MHz
- Low supply current 5 mA
- Fast settling 100 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load

## Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

## Connection Diagrams

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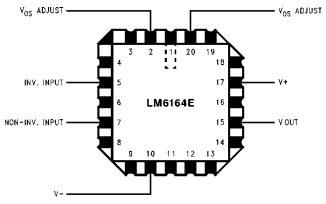
**NS Package Number J08A, M08A or N08E**

**20-Lead LCC**

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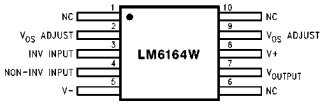
**Top View**

**NS Package Number E20A**

**10-Lead Flatpak**

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**Top View**

**NS Package Number W10A**

| Temperature Range | | | Package | NSC Drawing |
|---|---|---|---|---|
| **Military** $-55°C \le T_A \le +125°C$ | **Industrial** $-25°C \le T_A \le +85°C$ | **Commercial** $0°C \le T_A \le +70°C$ | | |
| | LM6264N | LM6364N | 8-Pin Molded DIP | N08E |
| LM6164J/883<br>5962-8962401PA | | | 8-Pin Ceramic DIP | J08A |
| | | LM6364M | 8-Pin Molded Surface Mt. | M08A |
| LM6164E/883<br>5962-89624012A | | | 20-Lead LCC | E20A |
| LM6164W/883<br>5962-8962401HA | | | 10-Pin<br>Ceramic Flatpak | W10A |

RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 6) | ±8V |
| Common-Mode Input Voltage (Note 10) | ($V^+ - 0.7V$) to ($V^- + 0.7V$) |
| Output Short Circuit to Gnd (Note 1) | Continuous |
| Soldering Information | |
| Dual-In-Line Package (N, J) | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|---|---|
| Storage Temperature Range | −65°C to +150°C |
| Max Junction Temperature (Note 2) | 150°C |
| ESD Tolerance (Notes 6 & 7) | ±700V |

## Operating Ratings

| | |
|---|---|
| Temperature Range (Note 2) | |
| LM6164 | $-55°C \le T_J \le +125°C$ |
| LM6264 | $-25°C \le T_J \le +85°C$ |
| LM6364 | $0°C \le T_J \le +70°C$ |
| Supply Voltage Range | 4.75V to 32V |

## DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM}$ = 0, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.

| Symbol | Parameter | Conditions | Typ | LM6164 | LM6264 | LM6364 | Units |
|---|---|---|---|---|---|---|---|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| $V_{OS}$ | Input Offset Voltage | | 2 | 4<br>**6** | 4<br>**6** | 9<br>**11** | mV max |
| $V_{OS}$ Drift | Input Offset Voltage Average Drift | | 6 | | | | µV/°C |
| $I_b$ | Input Bias Current | | 2.5 | 3<br>**6** | 3<br>**5** | 5<br>**6** | µA max |
| $I_{OS}$ | Input Offset Current | | 150 | 350<br>**800** | 350<br>**600** | 1500<br>**1900** | mA max |
| $I_{OS}$ Drift | Input Offset Current Average Drift | | 0.3 | | | | nA/°C |
| $R_{IN}$ | Input Resistance | Differential | 100 | | | | kΩ |
| $C_{IN}$ | Input Capacitance | | 3.0 | | | | pF |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_{OUT}$ = ±10V, $R_L$ = 2 kΩ (Note 9) | 2.5 | 1.8<br>**0.9** | 1.8<br>**1.2** | 1.3<br>**1.1** | V/mV min |
| | | $R_L$ = 10 kΩ | 9 | | | | |
| $V_{CM}$ | Input Common-Mode Voltage Range | Supply = ±15V | +14.0 | +13.9<br>**+13.8** | +13.9<br>**+13.8** | +13.8<br>**+13.7** | V min |
| | | | −13.5 | −13.3<br>**−13.1** | −13.3<br>**−13.1** | −13.2<br>**−13.1** | V min |
| | | Supply = +5V (Note 4) | 4.0 | 3.9<br>**3.8** | 3.9<br>**3.8** | 3.8<br>**3.7** | V min |
| | | | 1.5 | 1.7<br>**1.9** | 1.7<br>**1.9** | 1.8<br>**1.9** | V max |
| CMRR | Common-Mode Rejection Ratio | $-10V \le V_{CM} \le +10V$ | 105 | 86<br>**80** | 86<br>**82** | 80<br>**78** | dB min |
| PSRR | Power Supply Rejection Ratio | $\pm 10V \le V\pm \le \pm 16V$ | 96 | 86<br>**80** | 86<br>**82** | 80<br>**78** | dB min |

**DC Electrical Characteristics** The following specifications apply for Supply Voltage = ±15V, $V_{CM}$ = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$. (Continued)

| Symbol | Parameter | Conditions | Typ | LM6164 Limit (Notes 3, 11) | LM6264 Limit (Note 3) | LM6364 Limit (Note 3) | Units |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage Swing | Supply = +5V and $R_L$ = 2 kΩ | +14.2 | +13.5<br>**+13.3** | +13.5<br>**+13.3** | +13.4<br>**+13.3** | V min |
| | | | −13.4 | −13.0<br>**−12.7** | −13.0<br>**−12.8** | −12.9<br>**−12.8** | V min |
| | | Supply = +5V and $R_L$ = 2 kΩ (Note 9) | 4.2 | 3.5<br>**3.3** | 3.5<br>**3.3** | 3.4<br>**3.3** | V min |
| | | | 1.3 | 1.7<br>**2.0** | 1.7<br>**1.9** | 1.8<br>**1.9** | V max |
| | Output Short Circuit Current | Source | 65 | 30<br>**20** | 30<br>**25** | 30<br>**25** | mA min |
| | | Sink | 65 | 30<br>**20** | 30<br>**25** | 30<br>**25** | mA min |
| $I_S$ | Supply Current | | 5.0 | 6.5<br>**6.8** | 6.5<br>**6.7** | 6.8<br>**6.9** | mA min |

## AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM}$ = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.

| Symbol | Parameter | Conditions | Typ | LM6164 Limit (Notes 3, 11) | LM6264 Limit (Note 3) | LM6364 Limit (Note 3) | Units |
|---|---|---|---|---|---|---|---|
| GBW | Gain-Bandwidth Product | F = 20 MHz | 175 | 140<br>**100** | 140<br>**120** | 120<br>**100** | MHz min |
| | | Supply = ±5V | 120 | | | | |
| SR | Slew Rate | $A_V$ = +5 (Note 8) | 300 | 200<br>**180** | 200<br>**180** | 200<br>**180** | V/μs min |
| | | Supply = ±5V | 200 | | | | |
| PBW | Power Bandwidth | $V_{OUT}$ = 20 $V_{PP}$ | 4.5 | | | | MHz |
| $T_S$ | Settling Time | 10V Step to 0.1%<br>$A_V$ = −4, $R_L$ = 2 kΩ | 100 | | | | ns |
| $\phi_m$ | Phase Margin | $A_V$ = +5 | 45 | | | | Deg |
| $A_D$ | Differential Gain | NTSC, $A_V$ = +10 | <0.1 | | | | % |
| $\phi_D$ | Differential Phase | NTSC, $A_V$ = +10 | <0.1 | | | | Deg |
| $e_{np-p}$ | Input Noise Voltage | F = 10 kHz | 8 | | | | $nV/\sqrt{Hz}$ |
| $i_{np-p}$ | Input Noise Current | F = 10 kHz | 1.5 | | | | $pA/\sqrt{Hz}$ |

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Limits are guaranteed by testing or correlation.

**Note 4:** For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, $V_{CM}$ = 2.5V, $V_{OUT}$ = 2.5V. Pin 1 & Pin 8 ($V_{OS}$ Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade $V_{OS}$.

**Note 5:** $C_L \leq 5$ pF.

**Note 6:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially $V_{OS}$, $I_{OS}$, and Noise).

**Note 7:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

**Note 8:** $V_{IN}$ = 4V step. For supply = ±5V, $V_{IN}$ = 1V step.

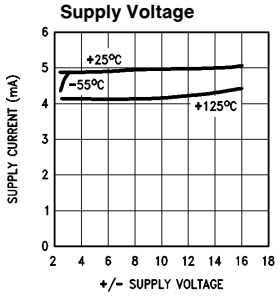
**Note 9:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

**Note 10:** The voltage between $V^+$ and either input pin must not exceed 36V.

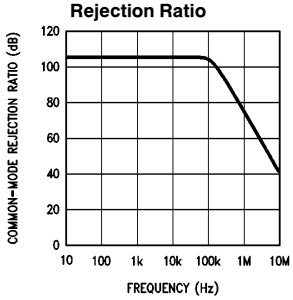
**Note 11:** A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

## Typical Performance Characteristics ($R_L$ = 10 kΩ, $T_A$ = 25°C unless otherwise specified)

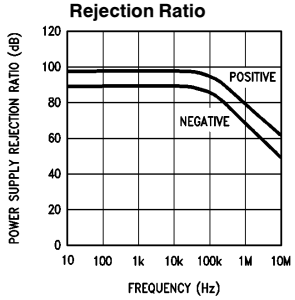
**Supply Current vs Supply Voltage**



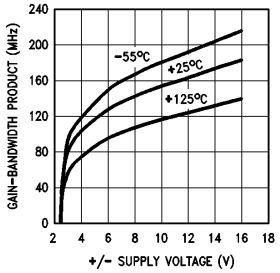

**Common-Mode Rejection Ratio**



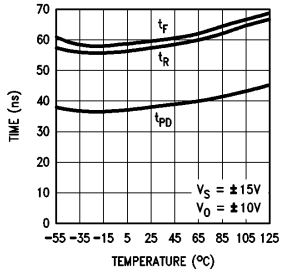

**Power Supply Rejection Ratio**



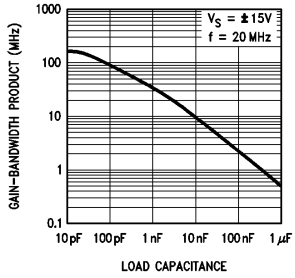

**Gain-Bandwidth Product**



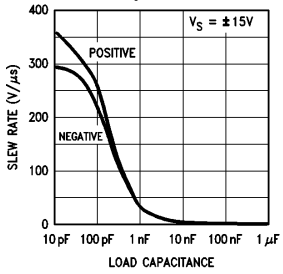

**Propagation Delay Rise and Fall Time**



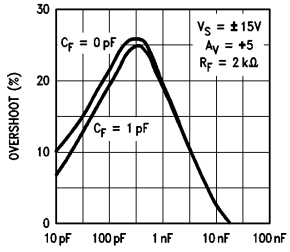

**Gain-Bandwidth Product vs Load Capacitance**



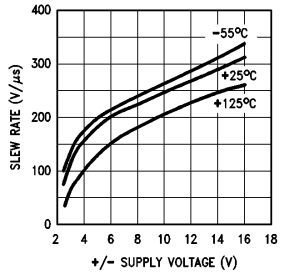

**Slew Rate vs Load Capacitance**



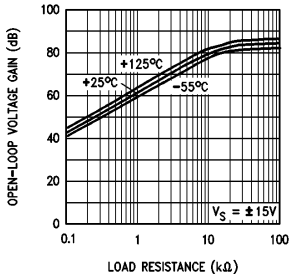

**Overshoot vs Load Capacitance**



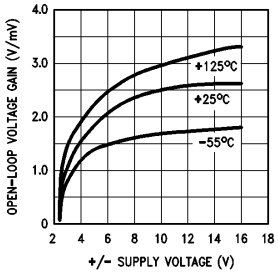

**Slew Rate**




**Voltage Gain vs Load Resistance**




**Gain vs Supply Voltage**

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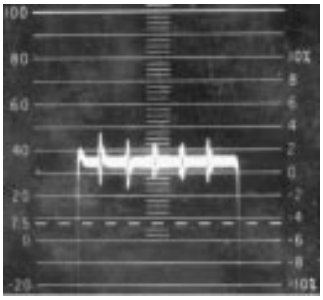
## Typical Performance Characteristics

($R_L$ = 10 kΩ, $T_A$ = 25°C unless otherwise specified) (Continued)

**Differential Gain (Note)**



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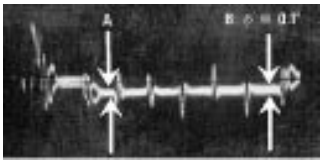
**Differential Phase (Note)**



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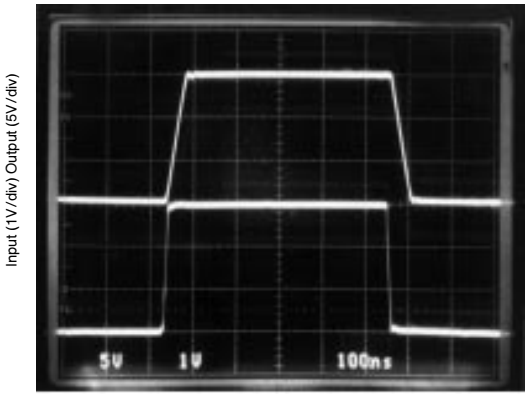
**Note:** Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

**Step Response; Av = +5**

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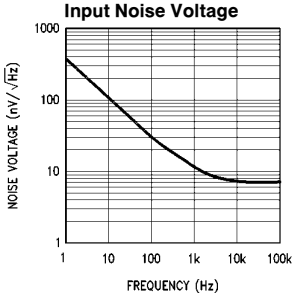
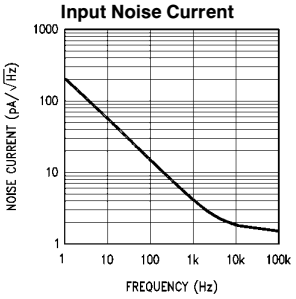
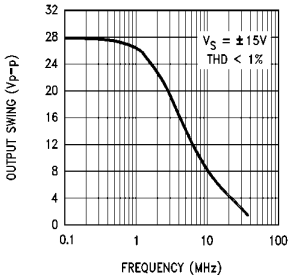
**Input Noise Voltage**




**Input Noise Current**




**Power Bandwidth**

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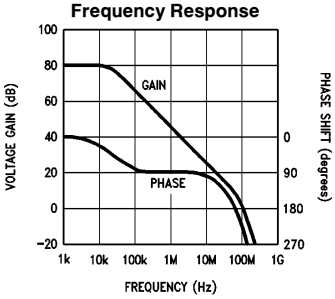
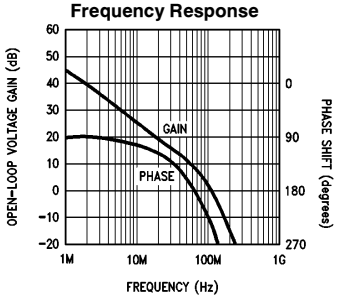
## Typical Performance Characteristics

($R_L$ = 10 kΩ, $T_A$ = 25°C unless otherwise specified) (Continued)

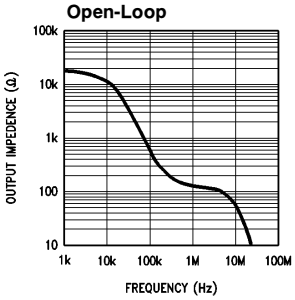
**Open-Loop Frequency Response**



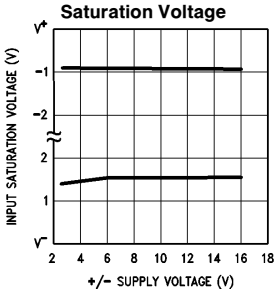

**Open-Loop Frequency Response**



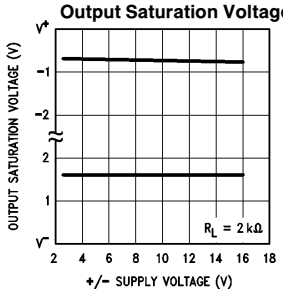

**Output Resistance Open-Loop**



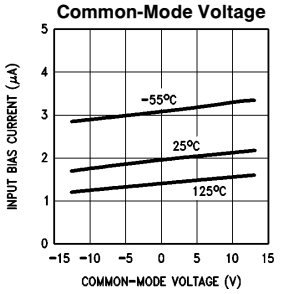

**Common-Mode Input Saturation Voltage**




**Output Saturation Voltage**




**Bias Current vs Common-Mode Voltage**

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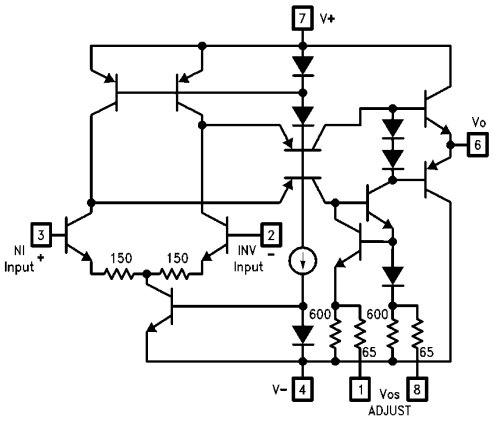
## Simplified Schematic




TL/H/9153–3

## Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced $A_{VOL}$ is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/$\mu$s), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

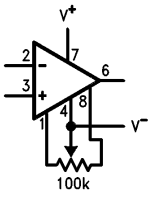
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 $\mu$F to 0.1 $\mu$F ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 $\mu$F to 10 $\mu$F (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

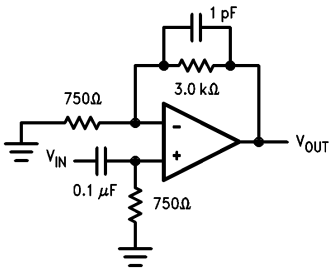
## Typical Applications

**Offset Voltage Adjustment**



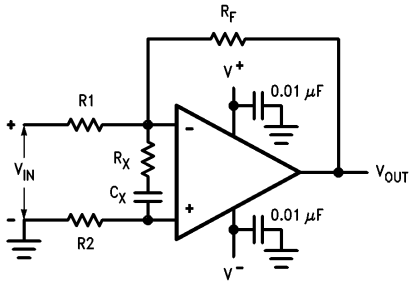

TL/H/9153–10

**Video-Bandwidth Amplifier**



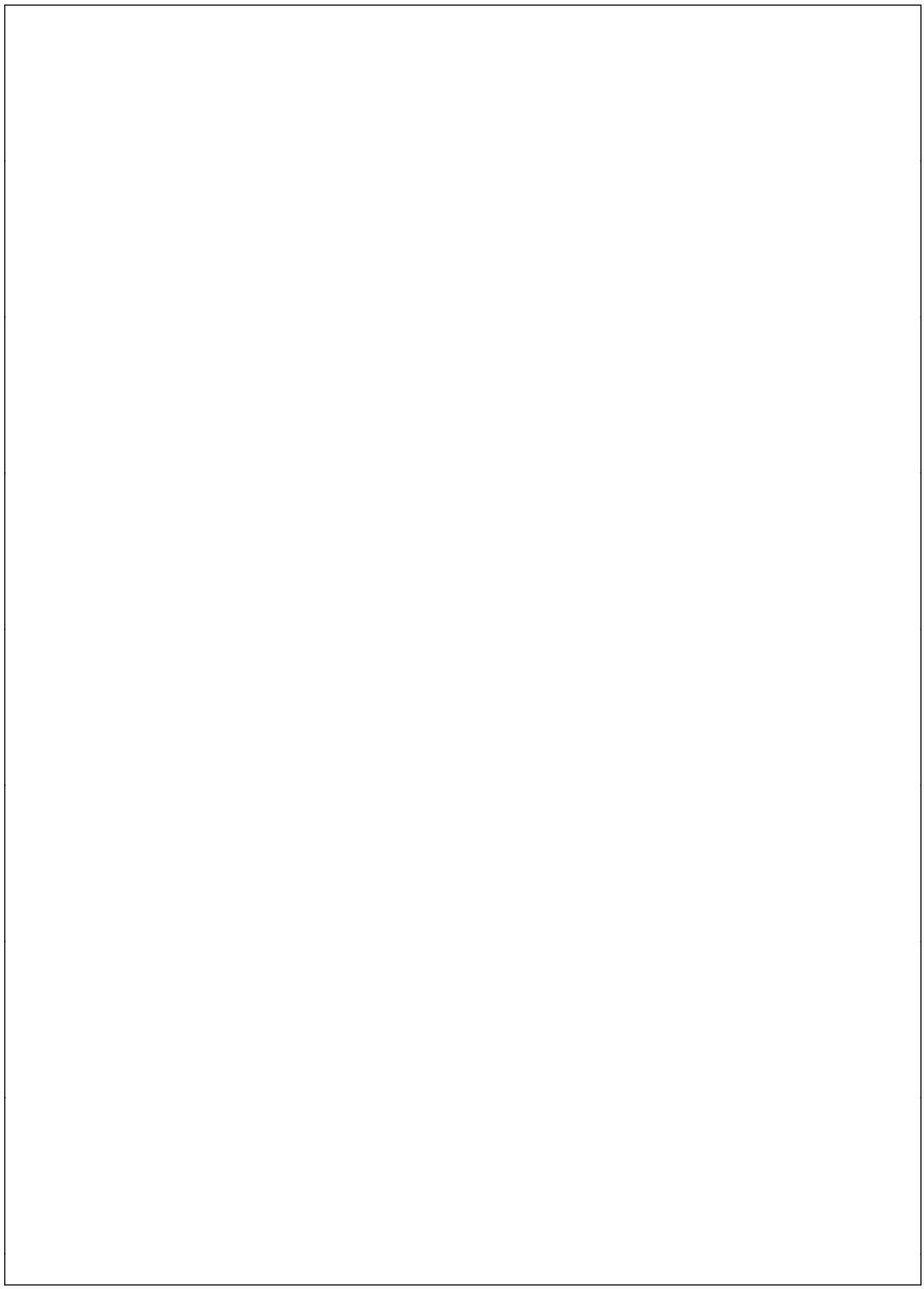

TL/H/9153–12

**Noise-Gain Compensation for Gains ≤5**

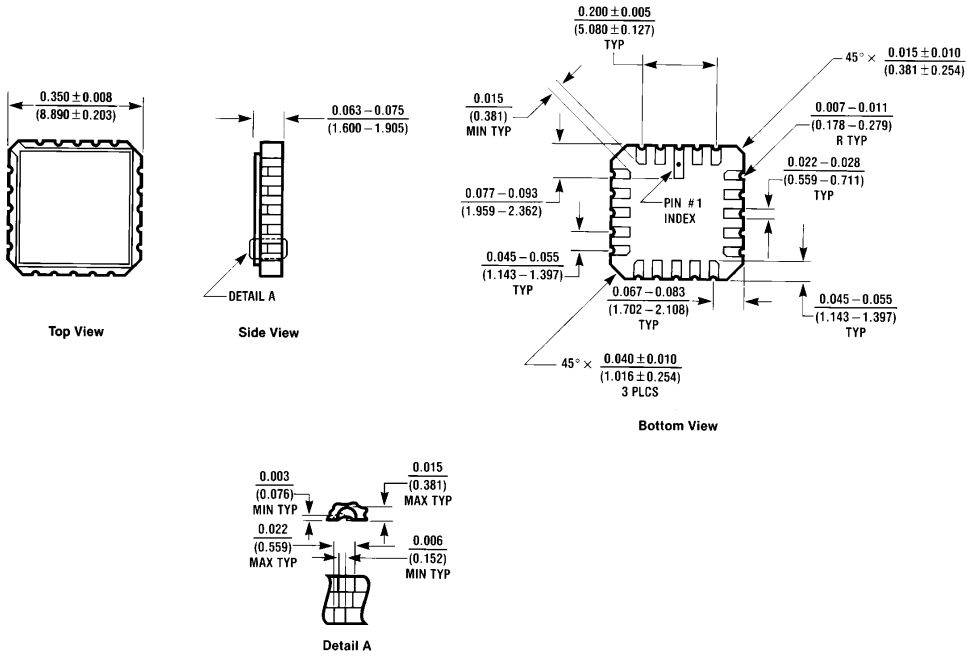



TL/H/9153–11

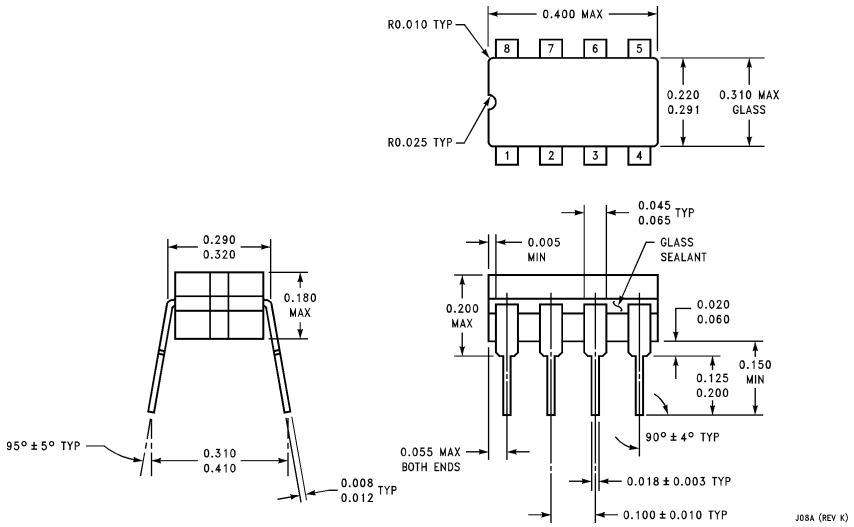
$R_X C_X \geq (2\pi \bullet 25\ \text{MHz})^{-1}$
$5\ R_X = R_1 + R_F(1 + R_1/R_2)$



## Physical Dimensions inches (millimeters)

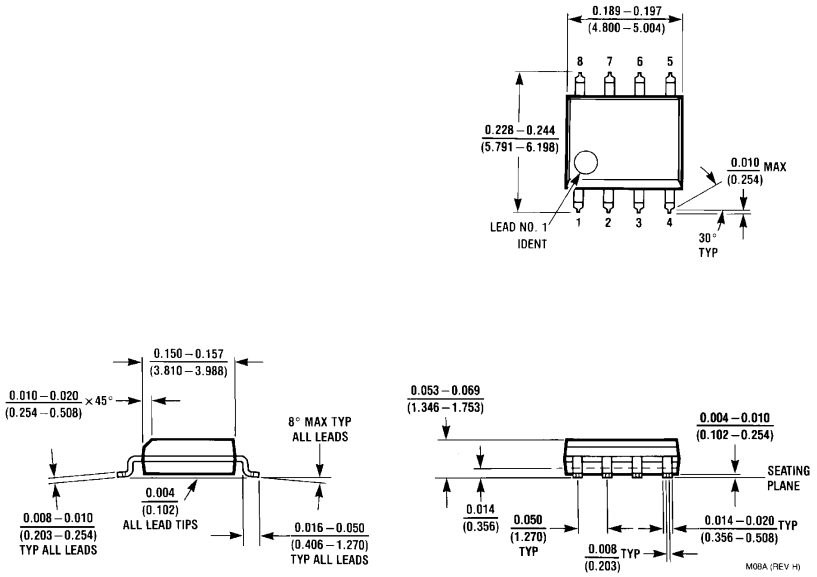



**20-Lead Small Outline Package (E)**
**Order Number LM6164E/883**
**NS Package Number E20A**

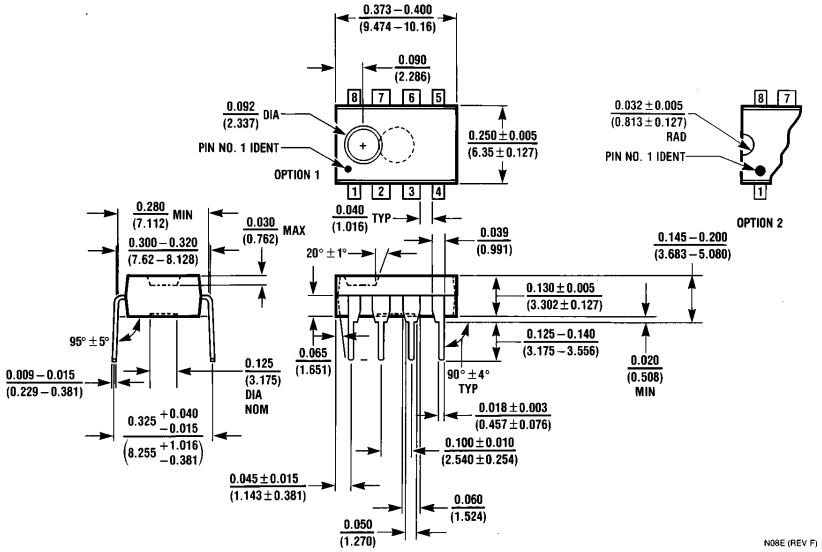



**Ceramic Dual-In-Line Package (J)**
**Order Number LM6164J/883**
**NS Package Number J08A**

## Physical Dimensions inches (millimeters) (Continued)

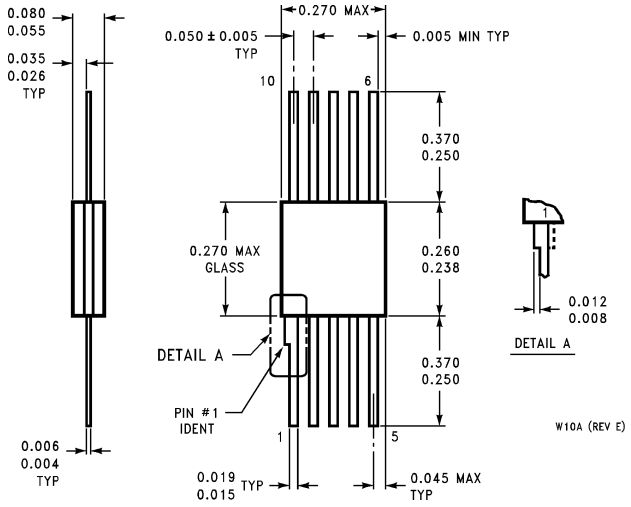



**Molded Package SO (M)**
**Order Number LM6364M**
**NS Package Number M08A**




**Molded Dual-In-Line Package (N)**
**Order Number LM6264N or LM6364N**
**NS Package Number N08E**

## Physical Dimensions inches (millimeters) (Continued)




**10-Pin Ceramic Flatpak**
**Order Number LM6164W/883**
**NS Package Number W10A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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