

DM54ALS590/DM74ALS590 8-Bit Binary Counter with Output Registers

General Description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and the storage register. The binary counter features a direct clear input (CCLR) and a count enable input (CCKEN). For cascading, a ripple carry output (RCO) is provided. Expansion is easily accomplished for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to CCK of the following stage. Both the counter and register clocks are positive edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

PRELIMINARY

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Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- \blacksquare Switching performance is guaranteed over full temperature and V_{CC} supply range



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free-Air Temperature Range	
DM54ALS	-55°C to +125°C
DM74ALS	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM54ALS590			DM74ALS590			Units	
Symbol			Min	Nom	Max	Min	Nom	Max	Units	
V _{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High Level Input Vol	tage	2			2			V	
V _{IL}	Low Level Input Vol	tage			0.7			0.8	V	
I _{OH}	High Level Output	RCO			-1			-1	mA	
	Current	Q			-1			-2.6		
I _{OL}	Low Level Output Current	RCO			8			16	– mA	
		Q			12			24		
fCCK	Counter Clock Frequency		0			0			MH	
f _{RCK}	Register Clock Frequency		0			0			MH	
t _W (CCK)	Width of Counter Clock Pulse								n	
t _W (CCLR)	Width of Counter Clear Pulse								n	
t _W (RCK)	Width of Register Clock Pulse								ns	
ts∪	Setup Time	CCKEN Low before CCK P								
		CCLR Inactive before CCK P							ns	
		CCK before RCK P (Note 1)								
t _H	Hold Time	CCKEN Low after CCK P							ns	
T _A	Free Air Operating Temperature		-55		125	0		70	°C	

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test	Min	Тур	Max	Units	
V _{IK}	Input Clamp Voltage	$V_{CC} = Min, I_I = -$			-1.5	V	
V _{OH}	V_{OH} High Level Output $V_{CC} = 4.5 \text{ to } 5.5 \text{V}, I_{OH} = -0.4 \text{ mA}$ Voltage $V_{CC} = \text{Min}, I_{OH} = \text{Max}$		V _{CC} – 2			v	
			V _{CC} = Min, I _{OH} = Max		3.2		ľ
V _{OL}	Low Level Output Voltage	$V_{CC} = Min$	54/74ALS I _{OL} = 12 mA	0.25 0		0.4	V
			74ALS I _{OL} = 24 mA		0.35	0.5	
I _{OZH}	Off-State Output Current With High Level Voltage Applied	$V_{CC} = Min, V_{IL} = V_{IH} = Min, V_O =$			20	μΑ	
I _{OZL}	Off-State Output Current With Low Level Voltage Applied	$V_{CC} = Min, V_{IL} = V_{IH} = Min, V_O =$			-20	μΑ	

Symbol	Parameter	Test	Min	Тур	Max	Units	
I	Input Current at Max Input Voltage	V _{CC} = Max, V _I =	= 7V			100	μA
IIH	High Level Input Current	V _{CC} = Max, V _I =			20	μΑ	
Ι _{ΙL}	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$				-100	μΑ
I _O	Output Drive Current	$V_{CC} = Max, V_O = 2.25V$		-30		-112	mA
Icc	Supply Current	V _{CC} = Max	Outputs High		33		
			Outputs Low		46		mA
			Outputs Disabled		44		

Symbol	Parameter	Conditions	From (Input)	DM54ALS590		DM74ALS590		Units
			To (Output)	Min	Мах	Min	Max	
f _{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5$ to 5.5V,	CCK to RCO					MHz
t _{PLH}	Propagation Delay Time Low to High Level Output	$R_{L} = 480 \Omega,$ $R_{1} = R_{2} = 500\Omega,$ $T_{1} = Min to Max$	CCK to RCO					ns
t _{PHL}	Propagation Delay Time High to Low Level Output	T _A = Min to Max	CCK to RCO					ns
t _{PLH}	Propagation Delay Time Low to High Level Output		CCLR to RCO					ns
t _{PLH}	Propagation Delay Time Low to High Level Output		RCK to Q					ns
t _{PHL}	Propagation Delay Time High to Low Level Output		RCK to Q					ns
t _{PLH}	Propagation Delay Time Low to High Level Output		G to Q					ns
t _{PHL}	Propagation Delay Time High to Low Level Output		G to Q					ns
t _{PZH}	Output Enable Time to High Level Output		G to Q					ns
t _{PZL}	Output Enable Time to Low Level Output		G to Q					ns
t _{PHZ}	Output Disable Time from High Level Output		G to Q					ns
t _{PLZ}	Output DisableTime from Low Level Output		G to Q					ns

Note 1: See Section 5 for test waveforms and output load.









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