

DS16F95, DS36F95 EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets both EIA-485 and EIA-422A standards.

The DS16F95/DS36F95 offers improved performance due to the use of L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by minimizing gate delay times. Thus, the DS16F95 and DS36F95 consume less power, and feature an extended temperature range as well as improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when $V_{CC} = 0V$. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

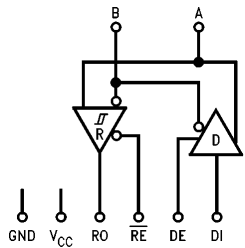
The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHz) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A
- Military temperature range available
- Qualified for MIL-STD 883C
- Standard Military Drawings (SMD) available
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagram



TL/F/9629-20

Function Tables

Driver			
Driver Input	Enable	Outputs	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver		
Differential Inputs	Enable	Output
A-B	RE	RO
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

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Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C	
'J' Package	1300 mW
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Derate 'J' package 8.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS36F95	4.75	5.0	5.25	V
DS16F95	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		+12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)				
DS36F95	0	+25	+70	°C
DS16F95	−55	+25	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -55$ mA 0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	$I_{OL} = 55$ mA 0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA			−1.3	V
$ V_{OD1} $	Differential Output Voltage	$I_O = 0$ mA			6.0	V
$ V_{OD2} $	Differential Output Voltage	$R_L = 100\Omega$, Figure 1	2.0	2.25		V
		$R_L = 54\Omega$, Figure 1	1.5	2.0		
$\Delta V_{OD} $	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , Figure 1			±0.2	V
					±0.4	
V_{OC}	Common Mode Output Voltage (Note 5)				3.0	V
$\Delta V_{OC} $	Change in Magnitude of Common Mode Output Voltage (Note 4)				±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled				mA
		$V_O = +12$ V $V_O = -7.0$ V			1.0 −0.8	
I_{IH}	Input Current HIGH	$V_I = 2.4$ V			20	μA
I_{IL}	Input Current LOW	$V_I = 0.4$ V			−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0$ V			−250	mA
		$V_O = 0$ V			−150	
		$V_O = V_{CC}$			150	
		$V_O = +12$ V			250	
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE} = 0.8$ V Outputs Enabled		28	mA
I_{CCX}					25	

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Driver Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, Figure 3	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, Figure 4	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, Figure 5		25	32	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, Figure 6		25	32	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, Figure 5		20	25	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, Figure 6		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per Figure 5 Timing per Figure 6		300		ns
t_{SKEW}	Skew (Pulse Width Distortion)	$R_L = 60\Omega$, Figure 3		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V$, $I_O = -0.4$ mA			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0$ mA	-0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$	35	50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA			-1.3	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA , Figure 2	0°C to +70°C 2.8 -55°C to +125°C 2.5			V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV, Figure 2	$I_{OL} = 8.0$ mA $I_{OL} = 16$ mA		0.45 0.50	V
I_{OZ}	High Impedance State Output	$V_O = 0.4V$ to $2.4V$			± 20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V $V_I = +12V$ $V_I = -7.0V$			1.0 0.8	mA
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$			20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$			-50	μA
R_I	Input Resistance		14	18	22	k Ω
I_{OS}	Short Circuit Output Current	(Note 9)	-15		-85	mA
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE} = 0.8V$ Outputs Enabled		28	mA
I_{CCX}			DE = 0.8V, $\overline{RE} = 2V$ Outputs Disabled		25	

COMMERCIAL

Receiver Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{ID} = 0V$ to $+3.0V$ $C_L = 15$ pF, <i>Figure 7</i>	14	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	19	24	ns
t_{ZH}	Output Enable Time to High Level	$C_L = 15$ pF, <i>Figure 8</i>		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, <i>Figure 8</i>		12	20	ns
t_{LZ}	Output Disable Time from Low Level			12	18	ns
$ t_{PLH} - t_{PHL} $	Pulse Width Distortion (SKEW)	<i>Figure 7</i>		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the $-55^\circ C$ to $+125^\circ C$ temperature range for the DS16F95 and across the $0^\circ C$ to $+70^\circ C$ range for the DS36F95. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

Note 5: In TIA/EIA-422A and TIA/EIA-485 Standards, V_{OC} , which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} .

Note 8: Refer to TIA/EIA-485 Standard for exact conditions.

Note 9: Only one output at a time should be shorted.

Order Number: DS16F95J, NS Package Number J08A

DS36F95J, NS Package Number J08A

MIL-STD 883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Ceramic 'E' Package	1800 mW
Ceramic 'J' Package	1300 mW
Ceramic 'W' Package	TBD
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Above $T_A = 25^\circ\text{C}$, derate E package, J package 8.7 mW/°C, W package 12.5 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) DS16F95	4.50	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0	+12	V
Differential Input Voltage (V_{ID})		±12	V
Output Current HIGH (I_{OH}) Driver		−60	mA
Receiver		−400	μA
Output Current LOW (I_{OL}) Driver		60	mA
Receiver		16	mA
Operating Temperature (T_A) DS16F95	−55	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input Voltage HIGH	$V_{CC} = 5.5\text{V}$	2.0		V
V_{IL}	Input Voltage LOW	$V_{CC} = 5.5\text{V}$		0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20\text{ mA}$, $V_{CC} = 4.5\text{V}$	3.0		V
V_{OL}	Output Voltage LOW	$I_{OL} = +20\text{ mA}$, $V_{CC} = 4.5\text{V}$		2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18\text{ mA}$		−1.3	V
$ V_{OD1} $	Differential Output Voltage	$I_O = 0\text{ mA}$, $V_{IN} = 0.8\text{V}$ or 2V , $V_{CC} = 5.5\text{V}$		6.0	V
$ V_{OD2} $	Differential Output Voltage	$R_L = 100\Omega$, $V_{CC} = 4.5\text{V}$, Figure 1	2.0		V
		$R_L = 54\Omega$, $V_{CC} = 4.5\text{V}$, Figure 1	1.5		V
$\Delta V_{OD} $	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , Figure 1, $V_{CC} = 4.5\text{V}$		±0.2	V
V_{OD3}	Differential Output Voltage	$V_{CM} = -7\text{V}$ to $+12\text{V}$	1.0		V
V_{OC}	Common Mode Output Voltage (Note 5)	$R_L = 54\Omega$ or 100Ω		3.0	V
$\Delta V_{OC} $	Change in Magnitude of Common Mode Output Voltage (Note 4)	$V_{CC} = 4.5\text{V}$, $R_L = 54\Omega$ or 100Ω		±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled $V_{CC} = 0\text{V}$ or 5.5V	$V_O = +12\text{V}$ $V_O = -7.0\text{V}$	1.0 −0.8	mA
I_{IH}	Input Current HIGH	$V_I = 2.4\text{V}$		20	μA
I_{IL}	Input Current LOW	$V_I = 0.4\text{V}$		−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0\text{V}$, $V_{IN} = 0\text{V}$ or 3V		−250	mA
		$V_O = 0\text{V}$, $V_{IN} = 0\text{V}$ or 3V		−150	mA
		$V_O = V_{CC}$, $V_{IN} = 0\text{V}$ or 3V		150	mA
		$V_O = +12\text{V}$, $V_{IN} = 0\text{V}$ or 3V		250	mA
I_{CC}	Supply Current	No Load, $DE = 2\text{V}$, $\overline{RE} = 0.8\text{V}$, Inputs Open		28	mA
I_{CCX}	(Total Package)	No Load, $DE = 0.8\text{V}$, $\overline{RE} = 2\text{V}$, Inputs Open		25	mA

MIL-STD 883C

Driver Switching Characteristics $V_{CC} = 5.0V$

Symbol	Parameter	Conditions	Min	Typ	$T_A = 25^\circ C$ Max	$T_A = 125^\circ C$ Max	$T_A = -55^\circ C$ Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, <i>Figure 3</i>	8.0	15	25	30	30	ns
t_{TD}	Differential Output Transition Time		8.0	15	25	30	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, <i>Figure 4</i>	6.0	12	18	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	18	25	25	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, <i>Figure 5</i>		25	35	45	45	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, <i>Figure 6</i>		25	40	50	50	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, <i>Figure 5</i>		20	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, <i>Figure 6</i>		20	30	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per <i>Figure 5</i> Timing per <i>Figure 6</i>		300				ns
t_{SKEW}	Skew (Pulse Width Distortion)	$R_L = 60\Omega$, <i>Figure 3</i>		1.0	6	12	12	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.5V$, $I_O = -0.4\text{ mA}$, $V_{CM} = -7V, 0V, +12V$ $V_{CC} = 4.5V, 5.5V$		0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0\text{ mA}$, $V_{CM} = -7V, 0V, +12V$, $V_{CC} = 4.5V, 5.5V$	-0.2		V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$, $V_{CC} = 4.5V, 5.5V$	35		mV
V_{IH}	Enable Input Voltage HIGH		2.0		V
V_{IL}	Enable Input Voltage LOW			0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18\text{ mA}$, $V_{CC} = 5.5V$		-1.3	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200\text{ mV}$, $I_{OH} = -400\text{ }\mu A$, <i>Figure 2</i> , $V_{CC} = 4.5V$	2.5		V
V_{OL}	Output Voltage LOW	$V_{ID} = -200\text{ mV}$, <i>Figure 2</i> , $V_{CC} = 4.5V$		0.45	V
		$I_{OL} = 8.0\text{ mA}$		0.50	
I_{OZ}	High Impedance State Output	$V_O = 0.4V, 2.4V$		± 20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V $V_{CC} = 5.5V$ or $V_{CC} = 0V$	$V_I = +12V$ $V_I = -7.0V$	1.0 -0.8	mA
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$		20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$		-50	μA
R_I	Input Resistance		10		k Ω
I_{OS}	Short Circuit Output Current	$V_{IN} = 1V$, $V_{OUT} = 0.0V$ (Note 9)	-15	-85	mA
I_{CC}	Supply Current (Total Package)	No Load, $DE = 2V$, $\overline{RE} = 0.8V$, Inputs Open		28	mA
I_{CCX}		No Load, $DE = 0.8V$, $\overline{RE} = 2.0V$, Inputs Open		25	

MIL-STD 883C

Receiver Switching Characteristics $V_{CC} = 5.0V$

Symbol	Parameter	Conditions	Min	Typ	$T_A = 25^\circ C$ Max	$T_A = 125^\circ C$ Max	$T_A = -55^\circ C$ Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{ID} = 0V$ to $+3.0V$ $C_L = 15$ pF, <i>Figure 7</i>	10	19	27	38	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	19	27	38	38	ns
t_{ZH}	Output Enable Time to High Level	$C_L = 15$ pF, <i>Figure 8</i>		10	20	30	30	ns
t_{ZL}	Output Enable Time to Low Level			12	20	30	30	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, <i>Figure 8</i>		12	20	30	30	ns
		$C_L = 20.0$ pF, <i>Figure 8</i> (Note 14)		12	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	$C_{IL} = 50$ pF, <i>Figure 8</i>		12	20	30	30	ns
$ t_{PLH} - t_{PHL} $	Pulse Width Distortion (SKEW)	<i>Figure 7</i>		1.0	8	16	16	ns

Ordering Number: DS16F95J/883, NS Package Number J08A
DS16F95E/883, NS Package Number E20A
DS16F95W/883, NS Package Number W10A

SMD Number: DS16F95J/883 $\longleftrightarrow$ 5962-896150PX
DS16F95E/883 $\longleftrightarrow$ 5962-8961502X
DS16F95W/883 $\longleftrightarrow$ 5962-896150HX

Parameter Measurement Information

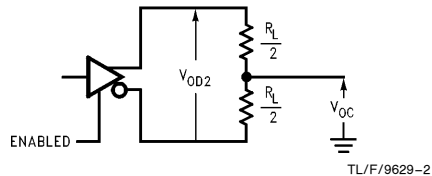


FIGURE 1. Driver V_{OD} and V_{OC} (Note 13)

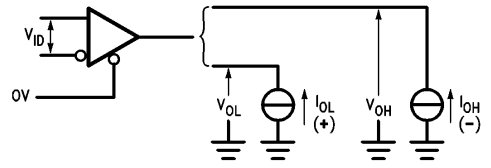


FIGURE 2. Receiver V_{OH} and V_{OL}

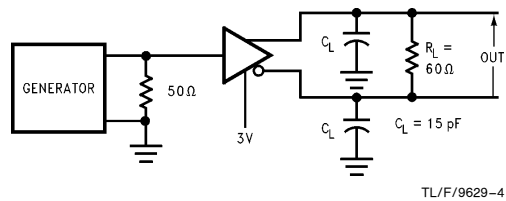


FIGURE 3. Driver Differential Output Delay and Transition Times (Notes 10, 12)

$$t_{\text{SKEW}} = |t_{\text{PLHD}} - t_{\text{PHLD}}|$$

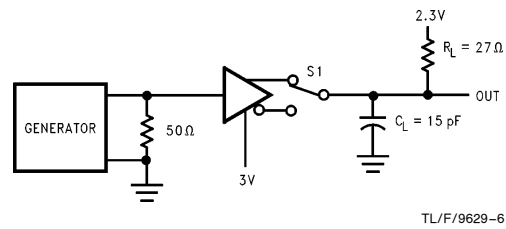


FIGURE 4. Driver Propagation Times (Notes 10, 11)

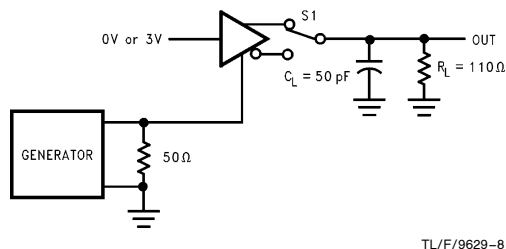


FIGURE 5. Driver Enable and Disable Times (t_{ZH} , t_{HZ}) (Notes 10, 11, 12)

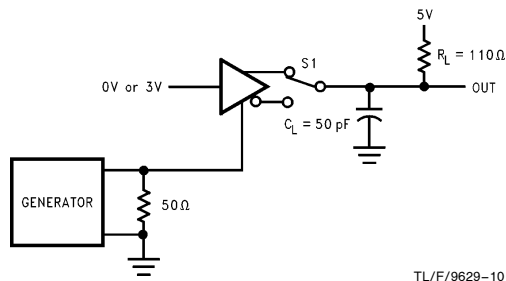
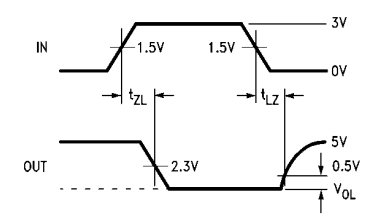
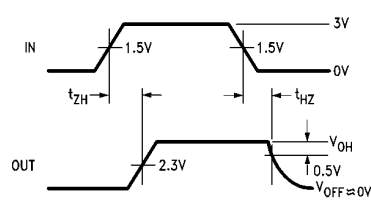
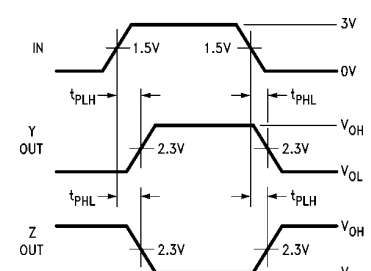
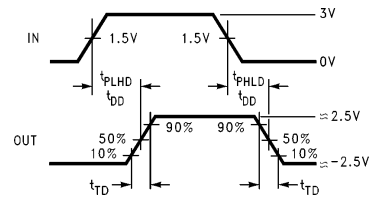
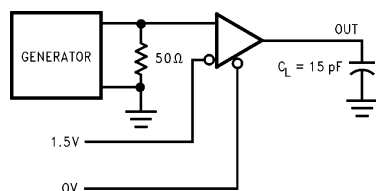


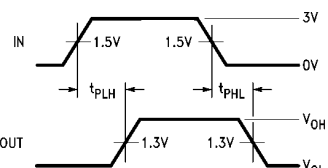
FIGURE 6. Driver Enable and Disable Times (t_{ZL} , t_{LZ} , t_{LZL}) (Notes 10, 11, 12)



Parameter Measurement Information (Continued)

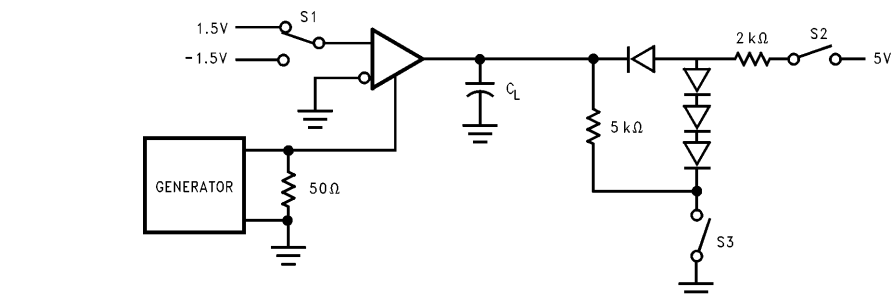


TL/F/9629-12

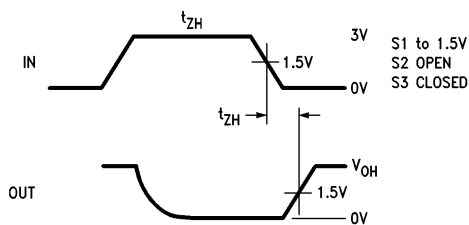


TL/F/9629-13

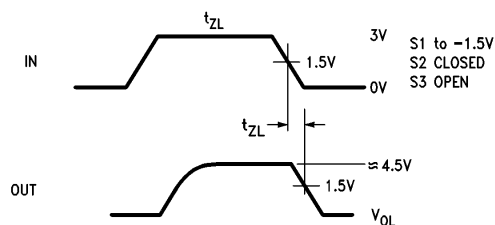
FIGURE 7. Receiver Propagation Delay Times (Notes 10, 11)



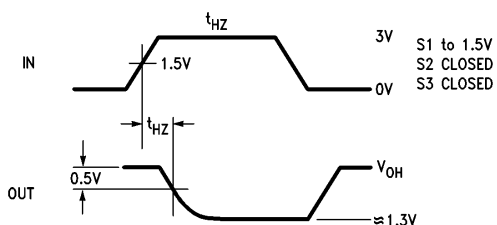
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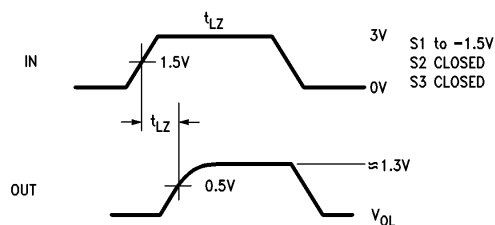
TL/F/9629-15



TL/F/9629-16



TL/F/9629-17



TL/F/9629-18

FIGURE 8. Receiver Enable and Disable Times (Notes 10, 11, 13)

Note 10: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

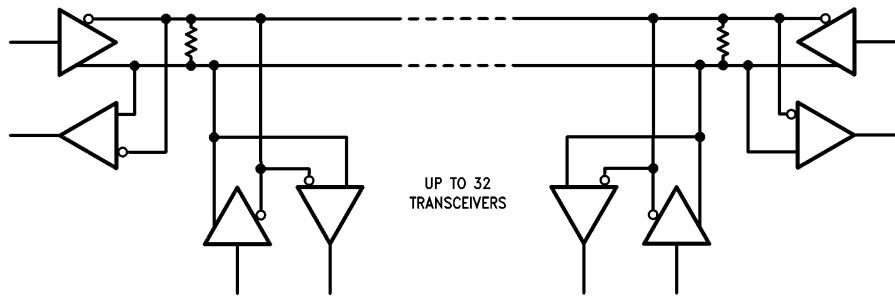
Note 11: C_L includes probe and stray capacitance.

Note 12: DS16F95/DS36F95 Driver enable is Active-High.

Note 13: All diodes are 1N916 or equivalent.

Note 14: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application



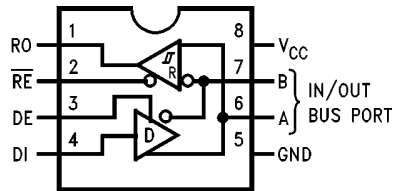
Note:

The line should be terminated at both ends in its characteristic impedance, typically 120Ω. Stub lengths off the main line should be kept as short as possible.

TL/F/9629-19

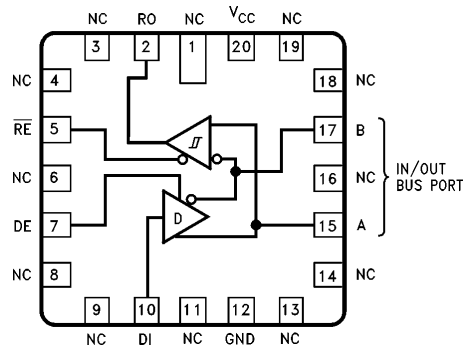
Connection Diagrams

8-Lead Dual-In-Line Package



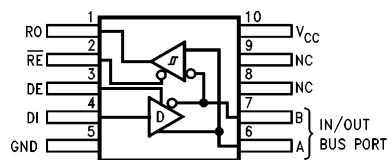
TL/F/9629-1

20-Lead Ceramic Leadless Chip Carrier



TL/F/9629-21

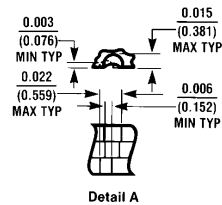
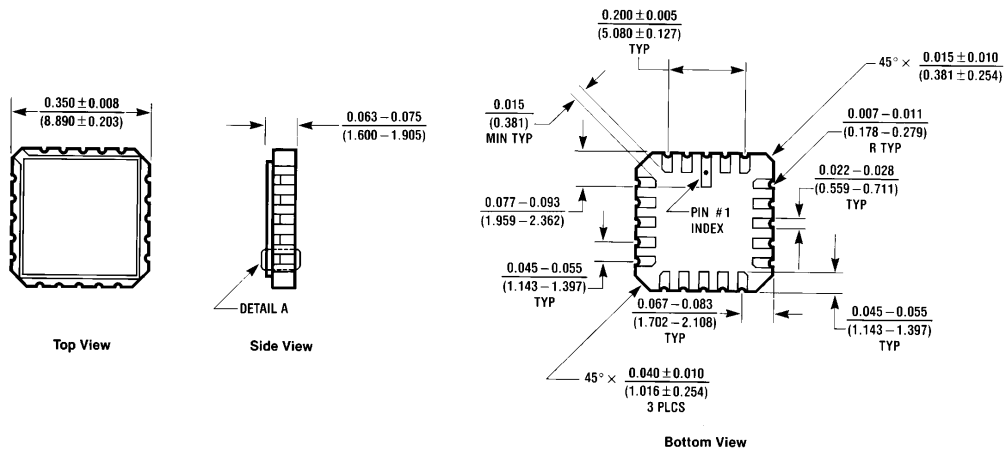
10-Lead Ceramic Flatpak



TL/F/9629-22

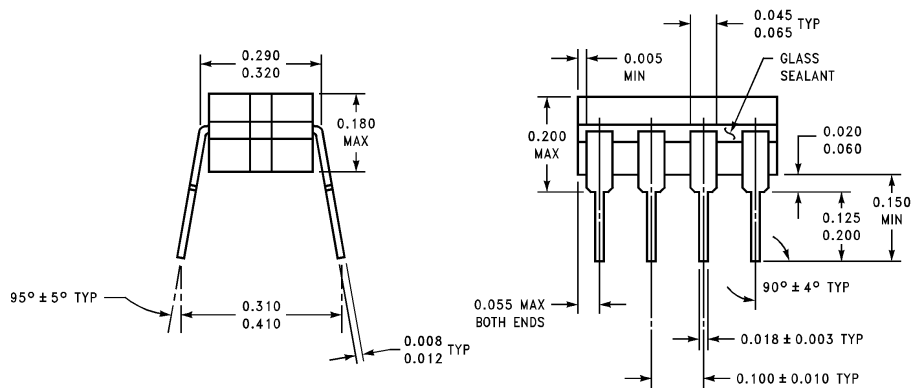
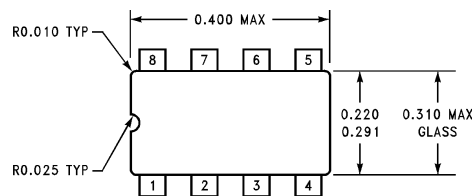
For Complete Military 883 Specifications, See RETS Data Sheet

Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (E)
 Order Number DS16F95E/883
 NS Package Number E20A

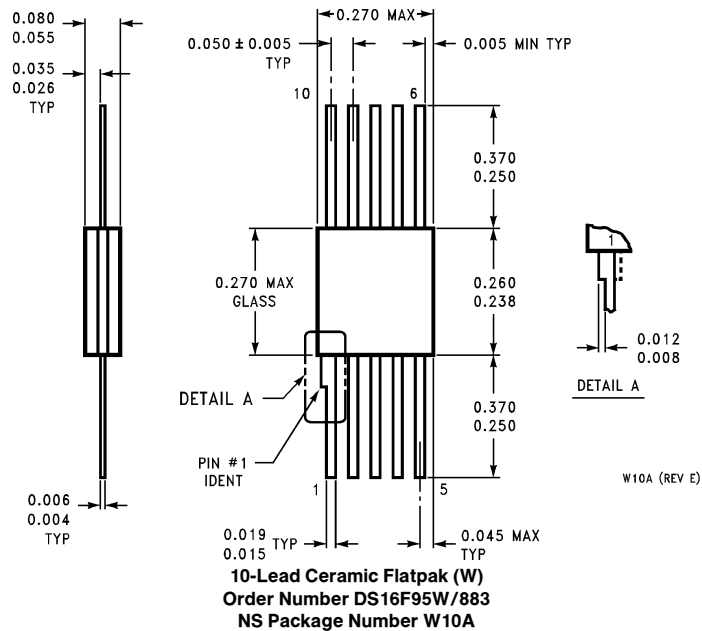
E20A (REV D)



8 Narrow Lead Ceramic Dual-In-Line Package (J)
 Order Number DS16F95, DS16F95J/883 or DS36F95J
 NS Package Number J08A

J08A (REV K)

Physical Dimensions inches (millimeters) (Continued)



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