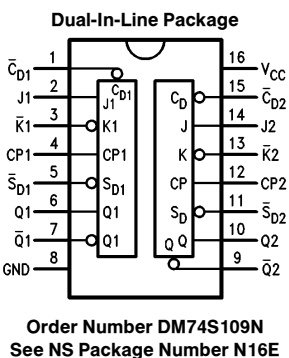


DM74S109 Dual JK Positive Edge-Triggered Flip-Flop

General Description

This device consists of two high speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'S74 data sheet) by connecting the J and K inputs together.

Connection Diagram



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Truth Table

Inputs		Outputs	
@ t_n		@ $t_n + 1$	
J	K	Q	Q
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:

LOW input to \bar{S}_D sets Q to HIGH level

LOW input to \bar{C}_D sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on \bar{C}_D and \bar{S}_D

makes both Q and \bar{Q} HIGH

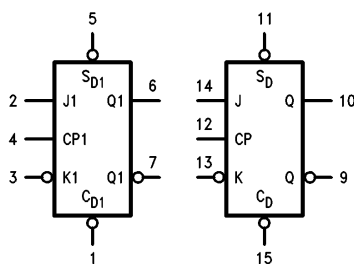
 t_n = Bit time before clock pulse

 $t_n + 1$ = Bit time after clock pulse

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Symbol


 V_{CC} = Pin 16

GND = Pin 8

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
DM74S	
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation

Recommended Operating Conditions

Symbol	Parameter	DM74S109			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			−1	mA
I _{OL}	Low Level Output Current			20	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H)	Setup Time	6.0			ns
t _s (L)	J _n or K _n to CP _n	6.0			
t _h (H)	Hold Time	0			ns
t _h (L)	J _n or K _n to CP _n	0			
t _w (H)	CP _n Pulse Width	7.0			ns
t _w (L)		6.5			
t _w (L)	C _{Dn} or S _{Dn} Pulse Width LOW	6.0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.2	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.7	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.35	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			50	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.5V			−2.0	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	−40		−100	mA
I _{CC}	Supply Current	V _{CC} = Max V _{CP} = 0V			52	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

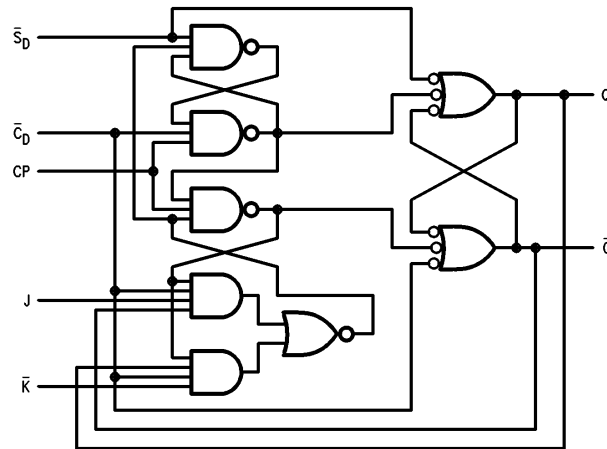
$V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15\text{ pF}$ $R_L = 280\Omega$		Units
		Min	Max	
f_{\max}	Maximum Clock Frequency	75		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or \bar{Q}_n		9.0 11	ns
t_{PLH} t_{PHL}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q_n or \bar{Q}_n		6.0 11	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

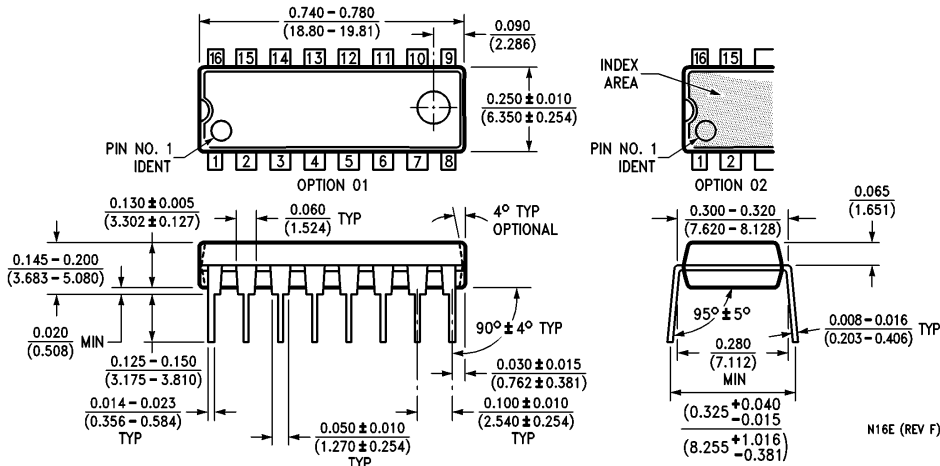
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Logic Diagram (one half shown)



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Physical Dimensions inches (millimeters)



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