Low Power RS-232C Driver and Receiver in CMOS

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.
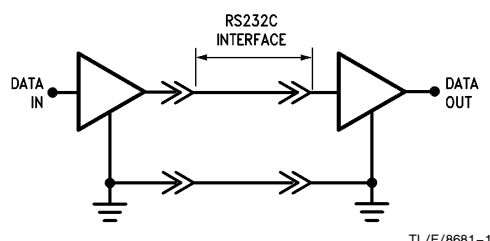

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FIGURE 1. EIA RS-232C Application

THE DRIVER

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction to 500 μA max versus 25 mA can be achieved.

The RS-232C specification states that the required driver output voltage is defined as being between $+5V$ and $+15V$ and is positive for a logic "0" ($+5V$ to $+15V$) and negative for a logic "1" ($-5V$ to $-15V$). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a $\pm 5V$ power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/μs. The inherent slew rate of the equivalent bipolar circuit DS1488/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/μs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

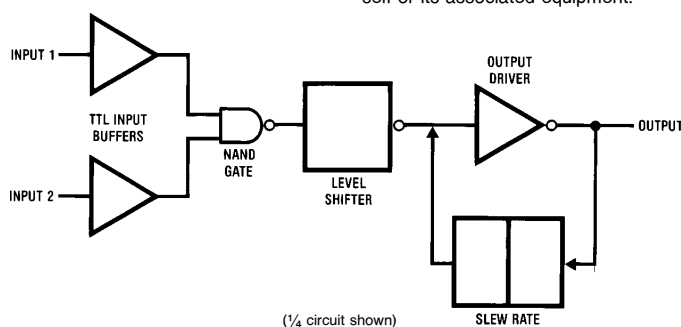(¼ circuit shown)

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FIGURE 2. DS14C88 Line Driver Block Diagram

THE RECEIVER

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (900 μA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "0" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 μs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The
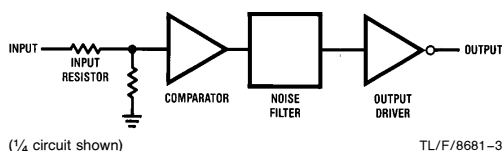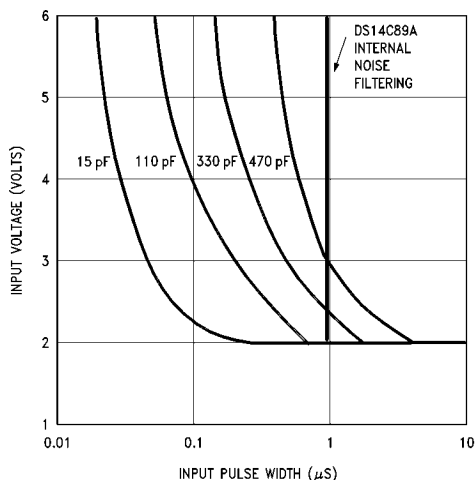

(¼ circuit shown)   TL/F/8681–3

FIGURE 3. DS14C89A Line Receiver Block Diagram

DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.

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FIGURE 4

TYPICAL APPLICATIONS

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS μP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate −9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a −9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC

converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6*. This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.
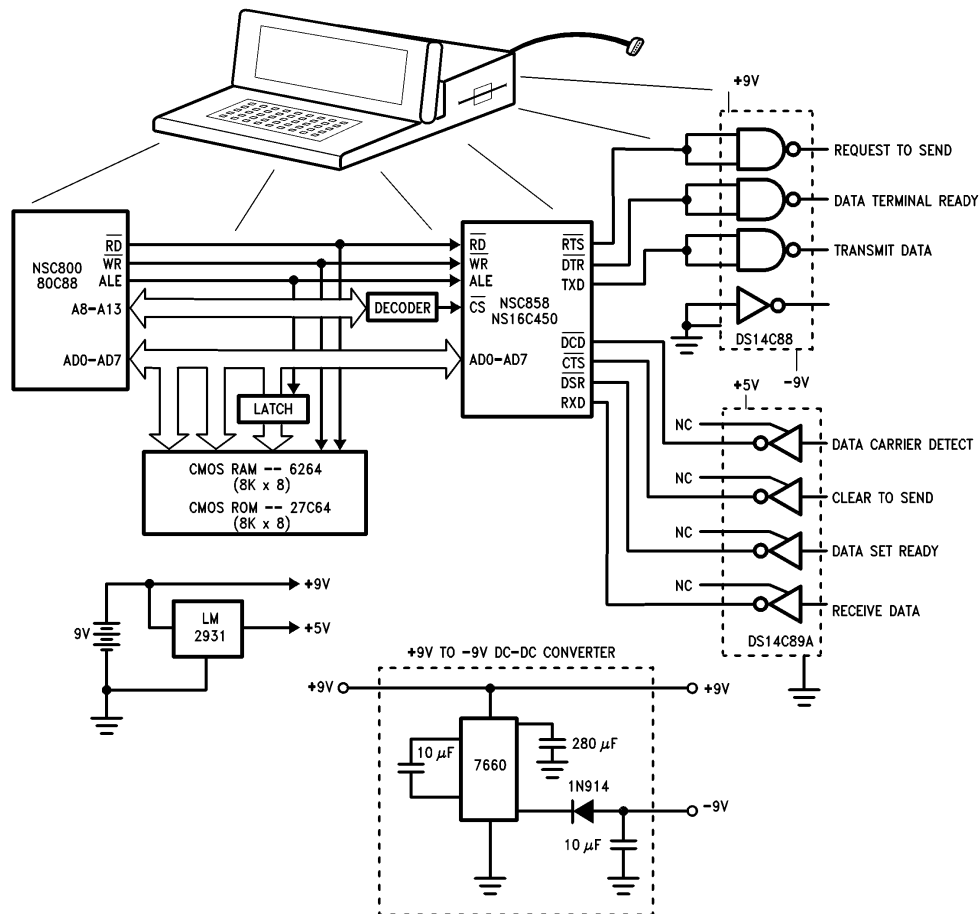
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FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART.
RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.
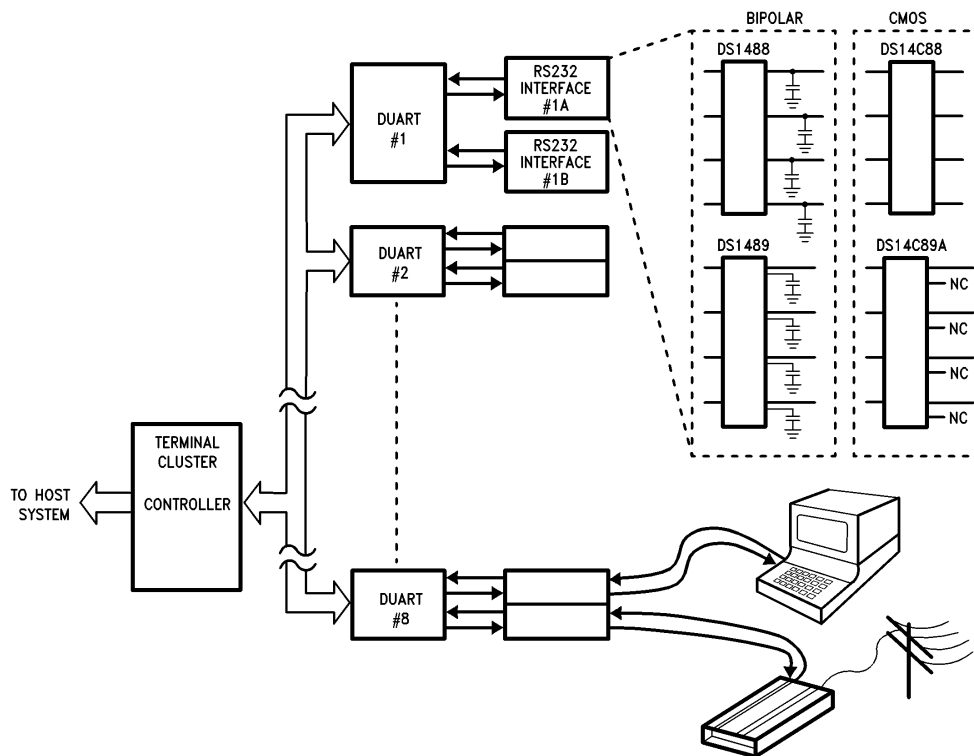
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FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

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