Ethernet/Cheapernet Physical Layer Made Easy with DP8391/92

National Semiconductor Application Note 442 Alex Djenguerian June 1986



Ethernet/Cheapernet Physical Layer Made Easy with DP8391/92

With the integration of the node electronics of IEEE 802.3 compatible local area networks now on silicon, system design is simplified. This application note describes the differences between the Ethernet and Cheapernet versions of the standard, and provides design guidelines for implementing the node electronics with National Semiconductor's DP8390 LAN chip set.

INTRODUCTION

The DP8390 chip set is designed to provide the physical and media access control layer functions of local area networks as specified in IEEE 802.3 standard. This standard is based on the access method known as carrier-sense multiple access with collision detection (CSMA/CD). In this scheme, if a network station wants to transmit, it first "listens" to the medium; if someone else is transmitting, the station defers until the medium is clear before it begins to transmit. However, two or more stations could still begin transmitting at the same time and give rise to a collision. When this happens, the two nodes detect this condition, back off for a random amount of time before making another attempt.

The IEEE 802.3 standard supports two different versions for the media, 10BASE5 (commonly known as Ethernet) and 10BASE2 (Cheapernet). These can be used separately, or together in a hybrid form. Both versions have similar electrical specifications and can be implemented using the same transceiver chip (DP8392). Cheapernet is the low cost version and is user installable. The following table compares the two:

Parameter	10BASE5 (Ethernet)	10BASE2 (Cheapernet)				
Data Rate	10 Mbit/s baseband	10 Mbits/s baseband				
Segment Length	500 m	185 m				
Network Span	2500 m	925 m				
Nodes per Segment	100	30				
Node Spacing	2.5 m (cable marked)	0.5 m min				
Capacitance per Node	4 pF max	8 pF max				
Cable	0.4 in diameter 50Ω Double Shielded Rugged N-Series Connectors	0.2 in diameter 50Ω (RG58A/U) Single Shielded Flexible BNC Connectors				
Transceiver Drop Cable	0.39 in diameter multiway cable with 15 pin D connectors 50 m max length	Not needed due to the high flexibility of the RG58A/U cable				







AN-442

© 1995 National Semiconductor Corporation TL/F/8689

RRD-B30M105/Printed in U. S. A.

Although Cheapernet is intended for local use, several 185 meter segments can be joined together with simple repeaters to provide for a larger network span. Similarly, several Cheapernet segments can be tied into a longer Ethernet "backbone". In this hybrid configuration, the network combines all the benefits of Cheapernet, flexibility and low cost, with the ruggedness and the much larger geographic range of standard Ethernet. *Figure 1* illustrates a typical hybrid LAN configuration.



PREAMBLE	SFD	DESTINATION	SOURCE	LENGTH	DATA	CRC
62-bits	2-bits	6-bytes	6-bytes	2-bytes	46-1500 bytes	4-bytes

PREAMBLE: This section consists of alternating 1 and 0 bits. As the packet travels through the network, some of these bits would be lost as most of the network components are allowed to provide an output some number of bits after being presented with a valid input.

START OF A FRAME DELIMITER (SFD): This field consists of two consecutive 1's to signal that the frame reception should begin.

DESTINATION AND SOURCE ADDRESSES: Each one of these frames is 6 bytes long and specifies the address of the corresponding node.

LENGTH: This 2 byte field indicates the number of bytes in the data field.

DATA: This field can be from 46 to 1500 bytes long. Messages shorter than 46 bytes require padding to bring the data field to the minimum length. If the data field is padded, the host can determine the number of valid data bytes by looking at the length field. Messages longer than 1500 bytes must be broken into multiple packets.

CRC: This field contains a Cyclic Redundancy Code calculation performed on the Destination address through the Data field for error control.

The shortest packet length thus adds up to be 512 bits long (excluding the preamble and the SFD). At 10 Mbit/sec this amounts to 51.2 μ s, which is twice as much as the 25 μ s maximum end-to-delay time that is allowed by the IEEE 802.3 protocol. This ensures that if a collision arises in the network, it would be recognized at all node locations.

The SNI combines the NRZ data packet received from the controller with a clock signal and encodes them into a serial bit stream using standard Manchester encoding. In this coding scheme, the first half of the bit cell contains the complementary data and the second half contains the true data. Thus a transition is always guaranteed in the middle of a bit cell.



The encoded signal appears in differential form at the SNI's output. In 10BASE5 (Ethernet) applications, this signal is sent to the transceiver or the Medium Attachment Unit (MAU) through the twisted pair Tranceiver Drop cable (also known as the Attachment Unit Interface cable). This cable typically consists of four individually shielded twisted wire pairs with an overall shield covering these individually shielded pairs. The signal pairs, which have a differential characteristic impedance of 78 $\Omega \pm 5\Omega$, should be terminated at the receiving ends. The cable can be up to 50 meters in length and have a maximum delay of 257 ns. The shields of the individual pairs should be connected to the logic ground in the Data Terminal Equipment (DTE) and the outer shield to the chassis ground. *Figure 3* shows a picture of the cable and the corresponding pin assignments.

DATA TERMINAL]	Pin IEEE 802.3 Name		Pairs	DP8391/2	Signal from	
EQUIPMENT (DTE)			ILLE 002.5 Name	Fails	Name	DTE	MAU
	MALE 15 PIN D CONNECTOR	3 10 11	DO + (Data Out +) DO - (Data Out -) DO S (DO Shield)	Transmit Pair	TX+ TX-	X X X	
\mathbf{Y}	DECONNECTOR	5 12 4	DI + (Data In +) DI - (Data In -) DI S (DI Shield)	Receive Pair	RX+ RX-	х	X X
й]	TRANSCEIVER — DROP CABLE (AU INTERFACE CABLE)	7 15 8	CO + (Control Out +) CO - (Control Out -) CO S (CO Shield)	Optional Pair		X X X	
		2 9 1	CI + (Control In +) CI - (Control In -) CI S (CI Shield)	Collision Pair	CD+ CD-	x	X X
		6 13 14	VC (Voltage Common) VP (Voltage Plus) VS (Voltage Shield)	Power Pair		X X X	
(MAU)		Shell	PG (Protective GND)			х	
	TL/F/8689-6						
	FIGURE 3. Trar	nsceive	r Cable Pin Assignments	5			

The transmitted packet from the SNI as well as all other signals (receive, collision, and DC power) must be electrically isolated from the coax in the MAU. The isolation means provided must withstand 500 V_{AC} rms for one minute for 10BASE2 and 2000 V_{AC} rms for 10BASE5. In order to detect collisions reliably, the electrical isolation is not done at the coax; instead it is done on the side of the Attachment Unit Interface. The isolation for the three signal lines can be easily provided by using three pulse transformers that come in a standard 16 pin plastic DIP from several manufacturers (Pulse Engineering, Valor Electronics). The inductance value for these transformers vary from 50 μ H to 150 μ H with the larger inductance values slowing the rise and fall times, and the smaller ones causing more voltage droop.

The Manchester encoded data from the SNI now reaches the CTI's transmit input after passing through the isolation transformer. A noise filter at this input provides a static noise margin of $-175~{\rm mV}$ to $-300~{\rm mV}$. These thresholds assure that differential Transmit (TX \pm) data signals less than $-175~{\rm mV}$ or narrower than 10 ns are always rejected, while signals greater than $-300~{\rm mV}$ and wider than 30 ns are always accepted. The $-300~{\rm mV}$ threshold provides sufficient margin since the differential drivers for the transceiver drop cable provide a minimum signal level of $\pm450~{\rm mV}$ after inductive droop, and the maximum attenuation allowed for the drop cable is 3 dB at signal frequencies. Signals meeting the squelch requirements are waveshaped and outputted to the coax medium. This is done as follows:

The transmitter's output driver is a switching current source that drives a purely resistive load of 25Ω presented by the coax to produce a voltage swing of approximately 2V. This

signal has to meet several critical electrical requirements:

RISE/FALL TIMES: The 10%–90% rise and fall times have to be 25 ns \pm 5 ns at 10 Mbit/sec. This spec helps to minimize electro-magnetic radiation by reducing the higher harmonic content of the signal and contributes to the smaller reflection levels on the coax. In addition, the rise and fall times are required to be matched to within 1 ns to minimize the overall jitter in the system.

DC LEVEL: The DC component of the signal has to be between -37 mA and -45 mA. The tolerance here is tight since collisions are detected by monitoring the average DC level on the coax.

AC LEVEL: The AC component of the signal has to be between ± 28 mA and the DC level. This specification guarantees a minimum signal at the far end of the coax cable in the worst case condition.

The signal shown in Fig. 4 would be attenuated as it travels along the coax. The maximum cable attenuation per segment is 8.5 dB at 10 MHz and 6 dB at 5 MHz. This applies for both the 500 meters of Ethernet cable and the 185 meters of Cheapernet cable. With 10 Mbit/sec Manchester data, this cable attenuation results in approximately 7 ns of edge jitter in either direction. The CTI's receiver has to compensate for at least a portion of this jitter to meet the ± 6 ns combined jitter budget. The receiver also should not overcompensate the signal in the case of a short cable. An equalizer filter in the CTI accomplishes this task. *Figure 5* shows a typical waveform seen at the far end of the cable and the corresponding differential output from the CTI's receiver.





In addition to the equalizer, an AC/DC squelch circuit at the coax input prevents noise on the cable from falsely triggering the receiver in the absence of a valid signal. The Receive differential line from the CTI should be isolated before it reaches the SNI for Manchester decoding. This signal now could have accumulated as much as ± 16.5 ns of jitter. *Figure 6* illustrates the jitter allocations for different network components and a typical signal waveform at the SNI's input. The digital phase-locked loop of the SNI can decode Manchester data with up to ± 20 ns of random jitter which provides enough margin for implementation.

The SNI converts the Manchester received packet to NRZ data and clock pulses and sends them to the controller. Upon reception, the NIC checks the destination address, and if it is valid, verifies the CRC with the one generated on board and stores the packet in the local buffer memory. The packet is then moved to the host by the NIC, and when this is completed the buffer area is reclaimed for storing new packets. If a collision occurs during this transfer process, the CTI will detect it by sensing the average DC level on the coax and will send a 10 MHz collision signal to the SNI. The SNI will translate this information to the controller in TTL form, and the transmitting controllers will backoff for different times and retransmit later. Also in case of illegally long packets (longer than 20 ms), a jabber timer in the CTI will disable the coax driver so that the "jabbering" station will

not bring down the entire network. The collision pair is activated in this case to inform the controller of the faulty condition. After the fault is removed, the jabber timer holds for 500 ms before re-enabling the coax driver.

COLLISION DETECTION SCHEMES

There are two different collision detection schemes that can be implemented with the CTI; receive, transmit modes. The IEEE 802.3 standard allows the use of receive, transmit, and transhybrid modes for non-repeater nodes for both Ethernet and Cheapernet applications. Repeaters are required to have the receive mode implementation.

RECEIVE MODE: Detects a collision between any two stations on the network with certainty at all times.

TRANSMIT MODE: Detects collisions with certainty only when the station is transmitting.

RECEIVE MODE: The receive mode scheme has a very simple truth table; however, the tight threshold limits make the design of it difficult. The threshold in this case has to be between the maximum DC level of one station (-1300 mV) and the minimum DC level of two far end stations (-1581 mV). Several factors such as the termination resistor variation, coax center conductor resistance, driver current level variation, signal skew, and input bias current of non-transmitting nodes contribute to this tight margin. On

Collision Detection Schemes								
Mode	Receive				Transmit			
No. of Stations	0	1	2	>2	0	1	2	>2
Transmitting	Ν	Ν	Y	Y	Ν	Ν	Y	Y
Non-Transmitting	Ν	Ν	Y	Y	Ν	Ν	М	Y

Truth Table for Various

 $Y \ = \ It \ will \ detect \ a \ collision, \quad N \ = \ It \ will \ not \ detect \ a \ collision,$

 $M \ = \ It \ may \ detect \ a \ collision$

top of the -1300 mV minimum level, the impulse response of the internal low pass filter has to be added. The CTI incorporates a 4 pole Bessel filter in combination with a trimmed on board bandgap reference to provide this mode of collision detection. However it would be difficult in receive mode to extend the cable length beyond the limits of the standard. It is also argued that it is not necessary for non-repeater nodes to detect collisions between other stations.

TRANSMIT MODE: In this case collisions have to be detected with certainty only when the station is transmitting. Thus, collisions caused by two other nodes may or may not be detected. This feature relaxes the upper limit of the threshold from -1581 mV to -1782 mV. As a result of this, longer cable segments can be used. With the CTI, a resistor divider can be used at the Collision Detect Sense pin (CDS) to lower the threshold from receive to transmit mode. Typical resistor values can be 120Ω from CDS to GND and 10k from CDS to V_{EE} (This moves the threshold by about -100 mV).

IMPLEMENTING A 10 BASE5 (ETHERNET) MAU WITH THE DP8392

The CTI provides all the MAU (transceiver) functions except for signal and power isolation. Signal isolation can easily be provided by a set of three pulse transformers that come in a single Dual-in-Line package. These are available from transformer vendors such as Pulse Engineering (PE64103) and Valor (LT1101). However, for the power isolation a DC to DC converter is required. The CTI requires a single -9 (\pm 5%) volt supply. This power has to be derived from the power pair of the drop cable which is capable of providing 500 mA in the 12 (-6%) to 15 (+5%) volt range. The low supply current of the CTI makes the design of the DC to DC converter quite easy. Such converters are being developed in hybrid packages by transformer manufacturers (Pulse Engineering PE64430 and Reliability Inc. 2E12R9). They provide the necessary voltage isolation and the output regulation. One can also build a simple DC to DC converter with a two transistor self oscillating primary circuit and some regulation on the secondary as shown in Figure 7.

Several areas of the PC board layout require special care. The most critical of these is for the coax connection. Ethernet requires that the CTI capacitance be less than 2 pF on the coax with another 2 pF allocated for the tap mechanism. The Receive Input (RXI) and the Transmit Output (TXO) lines should be kept to an absolute minimum by mounting the CTI very close to the center pin of the tap. Also, for the external diode at TXO (see *Figure 8*), the designer must minimize any stray capacitance, particularly on the anode side of the diode. To do this, all metal lines, especially the ground and V_{EE} planes, should be kept as far as possible from the RXI and TXO lines.

In order to meet the stringent capacitive loading requirements on the coax, it is imperative that the CTI be directly soldered to the PC board without a socket. A special lead frame in the CTI package allows direct conduction of heat from the die through these leads to the PC board, thus reducing the operating die temperature significantly. For good heat conduction the V_{EE} pins (4, 5 and 13) should be connected to large metal traces or planes.

A separate voltage sense pin (CDS) is provided for accurate detection of collision levels on the coax. In receive mode, where the threshold margin is tight, this pin should be independently attached to the coax shield to minimize errors due to ground drops. A resistor divider network at this pin can be used for transmit mode operation as described earlier.

The differential transmit pair from the DTE should be terminated with a 78 Ω differential resistive load. By splitting the termination resistor into two equal values and capacitively AC grounding the center node, the common mode impedance is reduced to about 20 Ω , which helps to attenuate common mode transients.

To drive the 78 Ω differential line with sufficient voltage swings, the CTI's collision and receive drivers need external 500 Ω resistors to V_{EE}. By using external resistors, the power dissipation of the chip is reduced, enhancing long term reliability. The only precision component required for the CTI is one 1k 1% resistor. This resistor sets many important parameters of the chip such as the coax driving levels, output rise and fall times, 10 MHz collision oscillator frequency, jabber timing, and receiver AC squelch timing. It should be connected between pins 11 (RR+) and 12 (RR-).

The DP8392 features a heartbeat function which can be externally disabled using pin 9. This function activates the collision output for a short time (10 ±5 bit cells) at the end of every transmission. It is used to ensure the controller that the collision circuitry is intact and properly functioning. Pin 9 enables CD Heartbeat when grounded, and disables it when connected to V_{EE}.

The IEEE 802.3 standard requires a static discharge path to be provided between the shield of the coax cable and the DTE ground via a 1 M Ω , 0.25W resistor. The standard also requires the MAU to have low susceptibility levels to electromagnetic interference. A 0.01 μ F capacitor will provide a

sufficient AC discharge path from the coaxial cable shield to the DTE ground. The individual shields should also be capacitively coupled to the Voltage Common in MAU. A typical Ethernet MAU connection diagram using the CTI in receive mode with the CD Heartbeat enabled is shown in Figure 8.



7

CHEAPERNET APPLICATION WITH THE DP8391 AND DP8392

The pin assignment of both the CTI and the SNI are designed to minimize the crossover of any printed circuit traces. Some of the components needed for an Ethernet like interface are not needed for Cheapernet. For instance, Cheapernet's relaxed load capacitance (8 pF, compared with 4 pF for Ethernet) obviates the need for an external capacitance isolation diode at TXO. Also, since the transceiver drop cable is not used in Cheapernet, there's no need for the 78 Ω termination resistors. Moreover, without the 78 Ω loading on the differential outputs, the pulldown resistors for both the CTI's collision and receive drivers and the SNI's transmit driver can be larger to save power. These resistors can be 1.5k instead of 500 Ω for the CTI and 500 Ω instead of 270 Ω for the SNI.

The 20 MHz crystal connection to the SNI requires special care. The IEEE 802.3 standard requires a 0.01% absolute accuracy on the transmitted signal frequency. An external capacitor between the X1 and X2 pins is normally needed to get the required frequency range. Section 3.1 of the data sheet describes how to choose the value of this capacitor.

The SNI also provides loopback capability for fault diagnosis. In this mode, the Manchester encoded data is internally diverted to the decoder input and sent back to the controller. Thus both the encoding and the decoding circuits are tested. The transmit differential output driver and the differential input receiver circuits are disabled during loopback. This mode can be enabled by a TTL active high input at pin 7.

Two different modes, half step and full step, can be selected at the SNI's transmit output. The standards require half step mode of operation, where the output goes to differential zero during idle to eliminate large idle currents through the pulse transformers. On the other hand, the differential output remains in a fixed state during idle in full step mode. The SNI thus can be used with transceivers which work in either mode. The two different modes can be selected with a TTL input at pin 5.

Figure 9 shows a typical Cheapernet connection diagram using the DP8391 and the DP8392.



The power isolation is similar here as in the Ethernet application, except the DC input is now usually 5V instead of 12V. Hybrid DC to DC converters are also being developed for this application (Ex: Pulse Engineering PE64381). Figure 10 shows a discrete implementation with 5V input and -9V output.



Lit. # 100442

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor

Japan Ltd. Tel: 81-043-299-2309 Fax: 81-043-299-2408

National Semiconductor

National Semiconductor Hong Kong Ltd. 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960

J	N	National Semiconductor Corporation	National Semiconductor Europe					
È		1111 West Bardin Road	Fax: (+49) 0-180-530 85 86					
		Arlington, TX 76017	Email: cnjwge@tevm2.nsc.com					
		Tel: 1(800) 272-9959	Deutsch Tel: (+49) 0-180-530 85 85					
		Fax: 1(800) 737-7018	English Tel: (+49) 0-180-532 78 32					
			Français Tel: (+49) 0-180-532 93 58					
7			Italiano Tel: (+49) 0-180-534 16 80					
L								

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

AN-442