High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor
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Toan Tran
Larry Kendall
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In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS (RS-422) REQUIREMENT

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s. In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 1 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

CABLE LENGTH

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* below is the guideline provided by RS-422 for data modulation rate versus cable length.

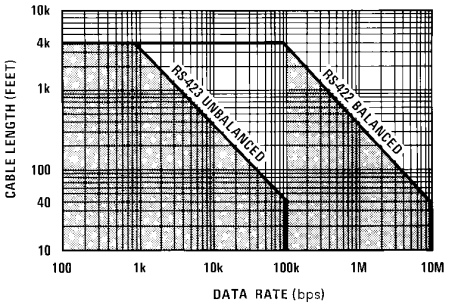

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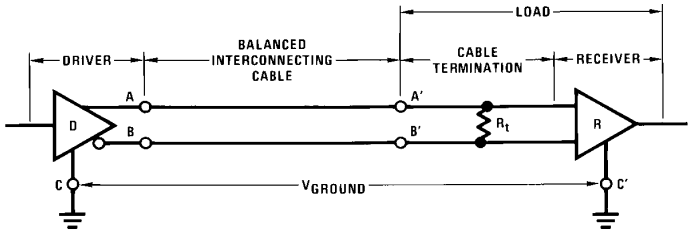
FIGURE 2. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.



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Legend:

R_t = Optional cable transmission resistance/receiver input impedance.

V_{GROUND} = Ground potential difference

A, B = Driver interface

A', B' = Load Interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. RS-422 Balanced Digital Interface Circuit

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MODULATION RATE

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbps. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 CHARACTERISTICS

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 AND DS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control *(Figure 3)*.

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

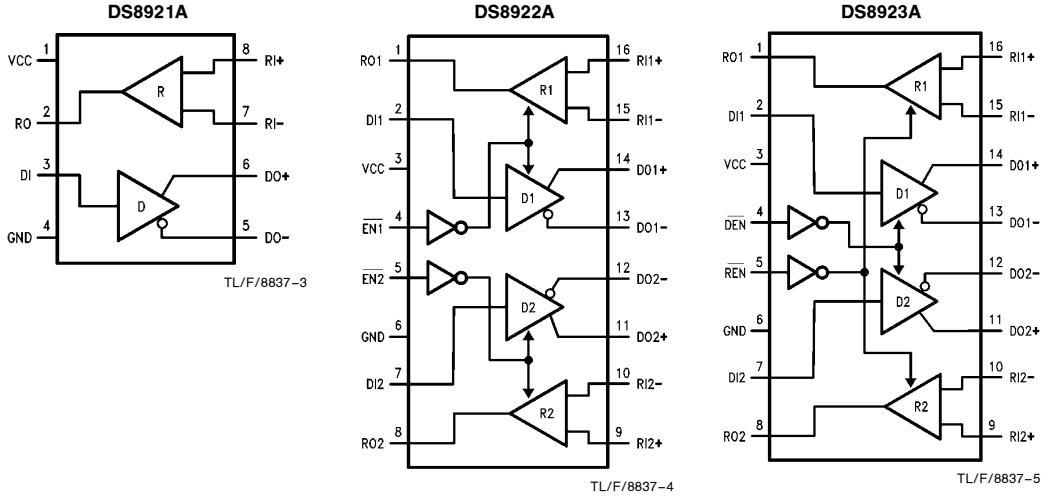
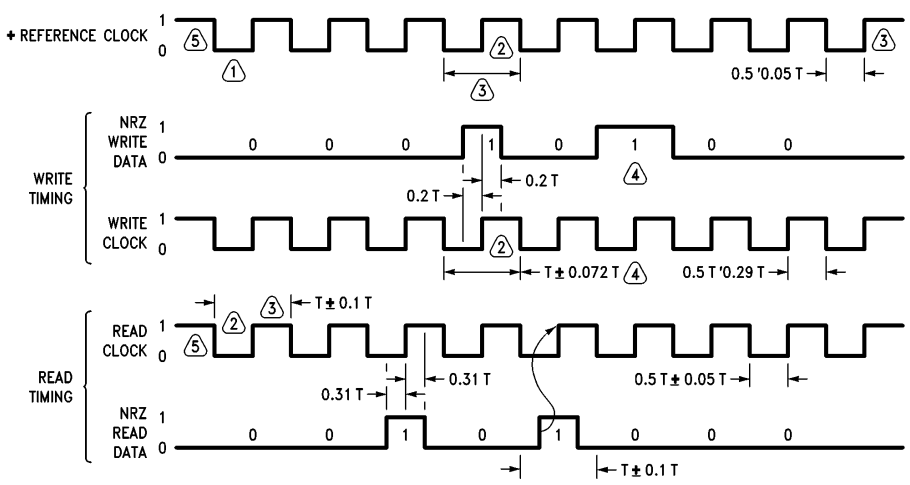


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams



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Note 1. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

Note 2. Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

Note 3. Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

Note 4. The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

Note 5. Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

FIGURE 4. ESDI Timing Diagrams

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	105			MHz
T_{PLH}	Preset or clear	Q or Q		3.3		7.5	ns
T_{PHL}				3.5		10.5	ns
T_{PLH}	Clock	Q or Q		3.5		8	ns
T_{PHL}				4.5		9	ns

FIGURE 5. 1 ns Clock Skew

ESDI ENHANCED SMALL DEVICE INTERFACE

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in *Figure 4.* This necessitates the use of National's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where $T = \frac{1}{F}$, the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T ±0.05T (50 ns ±5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 5*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 4* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408