Interfacing the DP8420A/21A/22A to the 80386

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INTRODUCTION

This application note describes how to interface the 80386 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). The 80386 is interfaced with the DP8422A in both address pipelined (Design #1) and non-address pipelined (Design #2) mode up to 50 MHz (80386-25). It is assumed that the reader is already familiar with 80386 access cycles and the DP8422A modes of operation.

I. DESCRIPTION OF DESIGN #1A and 1B, THE 80386 IN ADDRESS PIPELINED MODE, ALLOWING OPERATION UP TO 40 MHZ (80386-25) WITH ONE WAIT STATE PER ACCESS. (TWO WAIT STATES PER ACCESS AT 50 MHZ)

The #1 Designs (80386 in address pipelined mode) consist of the DP8422A DRAM controller, a single PAL® (PAL16R8D), and several logic gates. These parts interface to the 80386 as shown in the block diagrams. This design accommodates two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4 Mbit x 1 DRAMs). See *Figures 1–5*.

Design #1A differs from #1B in terms of the maximum operating frequency. Design #1A can operate up to 40 MHz, Design #1B can operate up to 50 MHz. Designs #1A and B allow 1 wait state per access for read cycles and 2 wait states per access for write cycles in address pipelined mode.

The memory banks are two way interleaved. This means that the least significant address bit (A2) is tied to the bank select input of the DP8422A (B1). Because the majority of accesses made by the 80386 will be sequential, one memory bank can be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed. This allows the memory system to be much higher performance than a non-interleaved memory system. In a non-interleaved memory system, each successive access will generally be to the same memory bank thereby requiring extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time.

In Designs 1A and 1B, the PAL (PAL16R8D) is used primarily to support the address pipelining capability of the 80386 (next address input, NA#). Since the NA# input is only allowed to drop low at the end of the current access no address latches are needed in the system. If address buffers were desired they could be used, but the DP8422A–25 would have to be used in order to meet the bank address and chip select setup times (see "80386 32 MHz Timing Calculations" section). An input is provided ($\overline{EXT\_NA}$) on the PAL for other system peripherals to have their $\overline{NA}$ inputs synchronized to the system clock (up to 50 MHz).

Designs 1A and 1B have one wait state during successive address pipelined accesses to alternating memory banks. During accesses to the same memory bank multiple wait states will be inserted to guarantee $\overline{RAS}$ precharge.

The "U2" gates need to all be part of the same chip to guarantee that "DIR" to the transceivers only changes state while enable to the transceivers is high.

If the user desires two wait states during successive address pipelined accesses (an extra wait state per access), this can be accomplished by running $\overline{RAS}0$ and $\overline{RAS}2$ through a flip-flop (clocked by CLKA) before allowing them to be input to the PAL in Design #1B. This will delay $\overline{NA}$ and $\overline{READY}$ by one CLKA clock period. In Design #1A the $\overline{WAITIN}$ input could be tied low and programmed to add 1 clock to the $\overline{DTACK}$ output.

If the user wants to do dual accessing with the DP8422A DRAM controller, address buffers (74AS244s) must be added to the address, $\overline{ECAS}0$–3, $\overline{LOCK}$, and $\overline{WIN}$ inputs. For the 32 MHz system (80386–16), the system diagram will remain unchanged, but the user will need to use the faster DP8422A–25 part.

For higher frequency dual access memory systems (above 32 MHz), these designs will have to be modified as above. Also, CLKA should be inverted (use $\overline{1Q}$ output from 74AS175). This will cause $\overline{RAS}$ to be started one half CLKA clock period later, allowing extra address and chip select setup time to the DP8422A.

II. DESCRIPTION OF DESIGN #2, (A, B, AND C). THE 80386 IN NON-ADDRESS PIPELINED MODE, ALLOWING OPERATION UP TO 40 MHZ (80386-20) WITH TWO WAIT STATES PER ACCESS (50 MHZ WITH THREE WAIT STATES)

Design #2A (80386 not using address pipelined mode) consists of the DP8422A DRAM controller, several flip-flops (74AS175), and several logic gates (see *Figure 7A*). Designs #2B, C are PAL based designs (see *Figures 7B, C*). These parts interface to the 80386 as shown in the block diagrams. This design accommodates two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4 Mbit x 1 DRAMs). See *Figures 6–10*.

The memory banks are two way interleaved. This means that the least significant address bit (A2) is tied to the bank select input of the DP8422A (B1). Because the majority of accesses made by the 80386 will be sequential, one memory bank can be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed. This allows the memory system to be much higher performance than a non-interleaved memory system. In a non-interleaved memory system, each successive access will generally be to the same memory bank thereby requiring extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time.

Designs #2A, B, C have two wait states during successive accesses to alternating memory banks. During accesses to the same memory bank multiple wait states will be inserted to guarantee $\overline{RAS}$ precharge.

If the user desires three wait states during successive accesses (an extra wait state per access), this can be accomplished by pulling $\overline{WAITIN}$ low during accesses. $\overline{WAITIN}$ should be programmed to add one clock period (CLKA) to the $\overline{DTACK}$ output. This will delay $\overline{READY}$ by one CLKA clock period.

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If the user wants to do dual accessing with the DP8422A DRAM controller address buffers (74AS244s) must be added to the address, $\overline{ECAS}0-3$, $\overline{LOCK}$ and $\overline{WIN}$ inputs. For the 32 MHz system (80386-16), the system diagram will remain unchanged, but the user will need to use the faster DP8422A-25 part.

For higher frequency dual access memory systems (above 32 MHz), design #2 will have to be modified as above. Also, CLKA should be inverted (use $\overline{1Q}$ output from 74AS175). This will cause $\overline{RAS}$ to be started one half CLKA clock period later, allowing extra address and chip select setup time to the DP8422A.

III. COMMON DESIGN FEATURES

The logic shown in these applications form a complete 80386 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

a. arbitration between Port A, Port B, and refreshing the DRAM;

b. the insertion of wait states to the processor (Port A) when needed (i.e., one wait state during address pipelined accesses (#1 Designs), two wait states during non-address pipelined accesses (Design #2), multiple wait states if an access takes place during a refresh operation or if $\overline{RAS}$ precharge is needed . . . etc.);

c. enabling address pipelining on the 80386 through the NA# input (#1 Designs only), and

d. performing byte writes and reads to the 32-bit words in memory.

The timing calculations for two designs (Designs #1 and #2) are included in this application note with the DP8422A interfaced to the 80386-16 running at 32 MHz and the 80386-20 running at 40 MHz.

Since the DP8420A/21A/22A has a column address hold time of 32 ns the minimum time between two accesses (to guarantee 0 ns row address setup time) is 150 ns (equivalent to three clock periods at 20 MHz, 150 ns).

When using the DP8420A/21A/22A at 20 MHz the user should program three clock periods of precharge. This is because two clock periods of precharge at 20 MHz will only guarantee 81 ns of $\overline{RAS}$ precharge (2 x 50 ns $-$ t_{D1}, (parameter #50 "14 ns") $-$ clock (20 MHz) to $\overline{AREQ}$ high, (approximately 5 ns for both design #1 and #2)).

In Design #2A the four gates "A1, A2, B, C" are not necessary if the system designer already has some means of correctly enabling the data transceivers. Also, in Design #2A the NOR gate that produces $\overline{READY}$ will not be needed in many systems, the $\overline{3Q}$ output of the 74AS175 could be used instead ($\overline{READY}$2.5). Though, this output would not allow quite as much $\overline{READY}$ setup time as the output of the NOR gate.

Because of the way ALE is generated to the DP8422A, two pulses of ALE may be generated during each access (see timing diagrams 3, 4, 5, 8, 9 and 10). This is not detailed in the DP8420A/21A/22A data sheet but this is permissible as long as no glitches happen after $\overline{AREQ}$ transitions low for that access. Therefore, this is a valid way of providing ALE to the DP8422A.

IV. 80386 DESIGN #1 AND #2, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 1 R1 = 1	$\overline{RAS}$ low four clocks, $\overline{RAS}$ precharge of three clocks
R2 = X R3 = X	
R4 = 0 R5 = 0 R6 = X R7 = X	No WAIT states during burst accesses
R8 = 0 R9 = X	Interleaved Mode (requires DRAMs with a column address hold time of 32 ns or less)
C0 = X C1 = X C2 = X	Select based upon the input clock frequency. Example: if the input clock frequency is 16 MHz then choose C0, 1, 2 = 0, 1, 0 (divide by eight, this will give a frequency of 2 MHz).
C3 = X	
C4 = 1 C5 = 0 C6 = 1	$\overline{RAS}$ and $\overline{CAS}$ groups selected by "B1". This mode allows two $\overline{RAS}$ and two $\overline{CAS}$ outputs to go low during an access.
C7 = 1 C8 = 1	Column address setup time of 0 ns. Row address hold time of 15 ns.
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1 B1 = 0	Fall-thru latches Access mode 0
$\overline{ECAS0}$ = 0	Non-extend $\overline{CAS}$

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either high or low voltage level (don't care condition)

V. 80386 #1 DESIGNS (AND #2 DESIGN), 32 MHZ TIMING CALCULATIONS, WITH ONE WAIT STATE PER ACCESS IN ADDRESS PIPELINED MODE, TWO WAIT STATES PER ACCESS IN NON-ADDRESS PIPELINED MODE (DP8422A-20 USES THE 16 MHZ CLOCK)

Note: Design #2 timing calculations are the same as Design #1 except for those calculations involving "CLKA", Timing calculations involving the minimum or maximum delay or skew of CLKA with respect to CLK2 should be recalculated substituting the 74AS175 parameters for the PAL parameters.

1. Maximum time to address valid (with respect to 16 MHz clock):

   40 ns (maximum time to address valid) − 2 ns ("D" speed PAL minimum delay, because 16 MHz clock is from PAL with minimum delay as skew from 32 MHz CPU clock) = 38 ns

2. Maximum time to ALE high (with respect to 16 MHz clock):

   35 ns (maximum $\overline{ADS}$ valid) + 4.5 ns (74AS02 maximum delay) − 2 ns ("D" speed PAL minimum clock delay, for skew between 32 MHz and 16 MHz clock) = 37.5 ns

   The CLKA delay to ALE through 74AS02 is similar: 31 ns (one half clock period, 16 MHz) + 4.5 ns (74AS02 maximum delay) + 1.5 ns (PAL estimated skew between low to high and high to low clock to output delay) = 37 ns

3. Minimum ALE high setup time to CLKA high (DP8422A-20 needs 16 ns):

   62.5 ns (one clock period, 16 MHz) − 37.5 ns (#2) = 25 ns

4. Minimum address setup time to CLKA high (DP8422-20 needs 20 ns):

   62.5 ns (Once clock period, 16 MHz) − 38 ns (#1) = 24.5 ns

5. Minimum $\overline{CS}$ setup time to CLKA high (DP8422-20 needs 14 ns):

   24.5 ns (#4) − 9 ns (74AS138 decoder) = 15.5 ns

6. Determining t_{RAC} ($\overline{RAS}$ access time needed by the DRAM):

   250 ns (four clock periods at 16 MHz) − 62.5 ns (one clock period) − 8 ns (PALmaximum delay low to high from CLK2 clock, clock skew) − 10 ns (data setup time) − 7 ns (74AS245) − 32 ns (CLK to $\overline{RAS}$ low) = 130.5 ns

   Therefore the t_{RAC} of the DRAM must be 130.5 ns or less.

7. Determining t_{CAC} ($\overline{CAS}$ access time needed by the DRAM):

   250 ns − 62.5 ns − 8 ns − 10 ns − 7 ns − 89 ns (CLK to $\overline{CAS}$ low) = 73.5 ns

   Therefore the t_{CAC} of the DRAM must be 73.5 ns or less. COMMON 120 ns DRAMS WILL MEET THIS t_{RAC} AND t_{CAC} PARAMETER.

8. Minimum setup of $\overline{DTACK}$0 to the PAL16R8D, DESIGN #1 ONLY, (need 10 ns):

   62.5 ns (one clock period) − 8 ns (PAL maximum delay low to high from clock, clock skew 32 MHz vs 16 MHz) − 41 ns (clock to $\overline{DTACK}$0 valid from DP8422A−20) = 13.5 ns

9A. Minimum $\overline{READY}$ setup time to $\overline{READY}$ being sampled (20 ns is needed by the 80386) DESIGN #1A and #1B:

   31.25 ns (one half clock period) − 8 ns (maximum "D" PAL clocked output delay) = 23.25 ns

9B. Minimum $\overline{READY}$ setup time to $\overline{READY}$ being sampled (20 ns is needed by the 80386) DESIGN #2:

   IF 74AS02 IS USED TO PRODUCE $\overline{READY}$:

   31.25 ns (Last one half clock period of T2) + 13 ns [17.5 ns (see in note below) − 4.5 ns (max 74AS02 Delay)] = 44.25 ns

   IF $\overline{3Q}$ OUTPUT OF 74AS175 IS USED FOR $\overline{READY}$:

   31.25 ns (Last one half clock period of T2) − 10 ns (max delay of 74AS175) = 21.25 ns

Note: $\overline{DTACK}$1.5 setup to 74AS175 input, used to generate $\overline{DTACK}$2.5 (74AS175 needs 3 ns):

   62.5 ns (one clock period at 16 MHz) − 45 ns [7.5 ns (CLKA max delay) + 33 ns (DP8422A−20 $\overline{DTACK}$1.5 max delay) + 4.5 ns (74AS02 max delay)] = 17.5 ns setup to mid T2 of last access clock period.

10. Minimum $\overline{NA}$ setup time to $\overline{NA}$ being sampled, Design #1 only (10 ns is needed by the 80386):

   31 ns (one clock period at 32 MHz) − 8 ns (maximum "D" PAL clocked output delay) = 23 ns

VI. 80386 #1 DESIGNS (AND #2 DESIGN), 40 MHZ TIMING CALCULATIONS, WITH ONE WAIT STATE PER ACCESS IN ADDRESS PIPELINED MODE, TWO WAIT STATES PER ACCESS IN NON-ADDRESS PIPELINED MODE (DP8422A−25 USES THE 20 MHZ CLOCK)

***Note: Design #2 timing calculations are the same as Design #1 except for those calculations involving "CLKA". CLKA is produced by a 74AS175 in Design #2 instead of a "D" speed PAL (Design #1). Therefore the timing calculations involving the minimum or maximum delay or skew of CLKA with respect to CLK2 should be recalculated substituting the 74AS175 parameters for the PAL parameters.

1. Maximum time to address valid (with respect to 20 MHz clock):

   32 ns (maximum time to address valid) − 2 ns ("D" speed PAL minimum delay, because 20 MHz clock is from PAL with minimum delay as skew from 40 MHz CPU clock) = 30 ns

2. Maximum time to ALE high (with respect to 20 MHz clock):

   30 ns (maximum $\overline{ADS}$ valid) + 4.5 ns (74AS02 maximum delay) − 2 ns (PAL minimum clock delay, for skew between 40 MHz and 20 MHz clock) = 32.5 ns

   The CLKA delay to ALE through 74AS02 is: 25 ns (one half clock period, 20 MHz) + 4.5 ns (74AS02 maximum delay) + 1.5 ns (PAL skew between low to high and high to low clock to output delay) = 31 ns

3. Minimum ALE high setup time to CLKA high (DP8422A−25 needs 15 ns):

   50 ns (one clock period, 20 MHz) − 32.5 ns (#2) = 17.5 ns

4. Minimum address setup time to CLKA high (DP8422A−25 needs 18 ns):

   50 ns (one clock period, 20 MHz) − 30 ns (#1) = 20 ns

5. Minimum $\overline{CS}$ setup time to CLKA high (DP8422A−25 needs 13 ns):

   20 ns (#4) − 6 ns (74AS139 two to four decoder) = 14 ns

6. Determining t_{RAC} ($\overline{RAS}$ access time needed by the DRAM):

   200 ns (four clock periods at 20 MHz) − 50 ns (one clock period) − 8 ns (PAL maximum delay low to high from CLK2 clock, clock skew) − 10 ns (data setup time) − 7 ns (74AS245) − 26 ns(CLK to $\overline{RAS}$ low) = 99 ns

   Therefore the t_{RAC} of the DRAM must be 99 ns or less.

7. Determining t_{CAC} ($\overline{CAS}$ access time needed by the DRAM):

   200 ns − 50 ns − 8 ns − 10 ns − 7 ns − 79 ns (CLK to $\overline{CAS}$ Low) = 46 ns

   Therefore the t_{CAC} of the DRAM must be 46 ns or less.

8. Minimum setup of $\overline{DTACK}$0 to the PAL16R8D, DESIGN #1 ONLY, (need 8 ns):

   50 ns (one clock period) − 8 ns (PAL maximum delay low to high from clock, clock skew 20 MHz vs 40 MHz) − 33 ns (clock to $\overline{DTACK}$0 valid from DP8422A−25) = 9 ns

9A. Minimum $\overline{READY}$ setup time to $\overline{READY}$ being sampled (11 ns is needed by the 80386) DESIGN #1:

   25 ns (one half clock period) − 8 ns (maximum "D" PAL clocked output delay) = 17 ns

9B. Minimum $\overline{READY}$ setup time to $\overline{READY}$ being sampled (11 ns is needed by the 80386) DESIGN #2:

   IF 74AS02 IS USED TO PRODUCE $\overline{READY}$:

   25 ns (Last one half clock period of T2) + 5.5 ns [10 ns (see in note below) − 4.5 ns (max 74AS02 delay)] = 30.5 ns

   IF $\overline{3Q}$ OUTPUT OF 74AS175 IS USED FOR $\overline{READY}$:

   25 ns (Last one half clock period of T2) − 10 ns (max delay of 74AS175) = 15 ns

Note: $\overline{DTACK}$ 1.5 setup to 74AS175 input, used to generate $\overline{DTACK}$2.5 (74AS175 needs 3 ns):

   50 ns (one clock period of 20 MHz) − 40 ns [7.5 ns (CLKA max delay) + 28 ns (DP8422−25 $\overline{DTACK}$1.5 max delay) + 4.5 ns (74AS02 max delay)] = 10 ns setup to mid T2 of last access clock period.

10. Minimum $\overline{NA}$ setup time to $\overline{NA}$ being sampled, Design #1 only (8 ns is needed by the 80386):

   25 ns (one clock period at 40 MHz) − 8 ns (maximum "D" PAL clocked output delay) = 17 ns

VII. 80386 DESIGN #1, PAL EQUATIONS WRITTEN IN NATIONAL SEMICONDUCTOR PLAN™ FORMAT

DESIGN #1A UP TO 40 MHz (80386-20)

PAL16R8D

CLK2 82384CLK $\overline{\text{ADS}}$ $\overline{\text{CS}}$ $\overline{\text{DTACK0}}$ $\overline{\text{EXT\_NA}}$ W B1 $\overline{\text{RESET}}$ GND

$\overline{\text{OE}}$ $\overline{\text{B0WE}}$ $\overline{\text{ADS1D}}$ CLKA $\overline{\text{READ}}$ $\overline{\text{READY}}$ $\overline{\text{NA}}$ $\overline{\text{ADS3D}}$ $\overline{\text{B1WE}}$ VCC

$\overline{\text{B1WE}}$:=$\overline{\text{ADS3D}}$*$\overline{\text{ADS1D}}$*READ*$\overline{\text{DTACK0}}$*B1
+$\overline{\text{B1WE}}$*CLKA*READ*RESET

$\overline{\text{B0WE}}$:=$\overline{\text{ADS3D}}$*$\overline{\text{ADS1D}}$*READ*$\overline{\text{DTACK0}}$*$\overline{\text{B1}}$
+$\overline{\text{B0WE}}$*CLKA*READ*RESET

$\overline{\text{ADS3D}}$:=$\overline{\text{ADS1D}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{ADS3D}}$*CLKA*RESET

$\overline{\text{NA}}$:=$\overline{\text{DTACK0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{CLKA}}$*RESET*$\overline{\text{W}}$
+$\overline{\text{DTACK0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B0WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{DTACK0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B1WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{EXT\_NA}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{NA}}$*CLKA*RESET

$\overline{\text{READY}}$:=$\overline{\text{NA}}$*$\overline{\text{ADS3D}}$*ADS1D*$\overline{\text{DTACK0}}$*CLKA*RESET
+$\overline{\text{READY}}$*$\overline{\text{ADS3D}}$*$\overline{\text{DTACK0}}$*RESET

$\overline{\text{ADS1D}}$:=$\overline{\text{ADS}}$*$\overline{\text{CLKA}}$*$\overline{\text{CS}}$
+$\overline{\text{ADS1D}}$*NA*RESET
+$\overline{\text{ADS1D}}$*CLKA*RESET

$\overline{\text{READ}}$:=$\overline{\text{CS}}$*$\overline{\text{W}}$*ADS1D*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{READ}}$*$\overline{\text{ADS1D}}$*RESET
+$\overline{\text{READ}}$*CLKA*RESET

CLKA:=$\overline{\text{82384CLK}}$

DESIGN #1B UP TO 50 MHz (80386-25)

PAL16R8D

CLK2 82384CLK $\overline{\text{ADS}}$ $\overline{\text{CS}}$ $\overline{\text{RAS0}}$ $\overline{\text{RAS2}}$ W $\overline{\text{NO\_NA}}$ $\overline{\text{RESET}}$ GND

$\overline{\text{OE}}$ $\overline{\text{B0WE}}$ $\overline{\text{ADS1D}}$ CLKA $\overline{\text{READ}}$ $\overline{\text{READY}}$ $\overline{\text{NA}}$ $\overline{\text{ADS3D}}$ $\overline{\text{B1WE}}$ VCC

$\overline{\text{B1WE}}$:=$\overline{\text{ADS3D}}$*$\overline{\text{ADS1D}}$*READ*$\overline{\text{RAS2}}$*NO_NA
+$\overline{\text{B1WE}}$*CLKA*READ*RESET

$\overline{\text{B0WE}}$:=$\overline{\text{ADS3D}}$*$\overline{\text{ADS1D}}$*READ*$\overline{\text{RAS0}}$*NO_NA
+$\overline{\text{B0WE}}$*CLKA*READ*RESET

$\overline{\text{ADS3D}}$:=$\overline{\text{ADS1D}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{ADS3D}}$*CLKA*RESET

$\overline{\text{NA}}$:=$\overline{\text{RAS0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{CLKA}}$*RESET*NO_NA*$\overline{\text{W}}$
+$\overline{\text{RAS0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B0WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{RAS0}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B1WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{RAS2}}$*$\overline{\text{ADS1D}}$*$\overline{\text{CLKA}}$*RESET*NO_NA*$\overline{\text{W}}$
+$\overline{\text{RAS2}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B0WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{RAS2}}$*$\overline{\text{ADS1D}}$*$\overline{\text{ADS3D}}$*$\overline{\text{B1WE}}$*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{NA}}$*CLKA*RESET

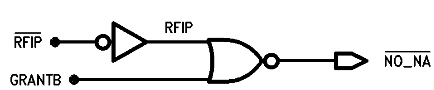
$\overline{\text{READY}}$:=$\overline{\text{NA}}$*$\overline{\text{ADS3D}}$*ADS1D*$\overline{\text{RAS0}}$*CLKA*RESET*NO_NA
+$\overline{\text{READY}}$*$\overline{\text{ADS3D}}$*$\overline{\text{RAS0}}$*RESET*NO_NA
+$\overline{\text{NA}}$*$\overline{\text{ADS3D}}$*ADS1D*$\overline{\text{RAS2}}$*CLKA*RESET*NO_NA
+$\overline{\text{READY}}$*$\overline{\text{ADS3D}}$*$\overline{\text{RAS2}}$*RESET*NO_NA

$\overline{\text{ADS1D}}$:=$\overline{\text{ADS}}$*$\overline{\text{CLKA}}$*$\overline{\text{CS}}$
+$\overline{\text{ADS1D}}$*NA*RESET
+$\overline{\text{ADS1D}}$*CLKA*RESET

$\overline{\text{READ}}$:=$\overline{\text{CS}}$*$\overline{\text{W}}$*ADS1D*$\overline{\text{CLKA}}$*RESET
+$\overline{\text{READ}}$*$\overline{\text{ADS1D}}$*RESET
+$\overline{\text{READ}}$*CLKA*RESET

CLKA:=$\overline{\text{82384CLK}}$

Logic Needed for "$\overline{\text{NO\_NA}}$" Term in Design #1B



TL/F/9730-12

Key: Reading PAL Equations Written in PLAN

EXAMPLE EQUATIONS: $\overline{\text{READ}}$:= CS_RD*ADS1D*$\overline{\text{CLKA}}$
+$\overline{\text{READ}}$*$\overline{\text{ADS1D}}$
+$\overline{\text{READ}}$*CLKA

This example reads: the output "$\overline{\text{READ}}$" will transition low on the next rising "CLK2" clock edge (given that one of the following conditions are valid, a setup time before "CLK2" transitions high);

1. the input "CS__RD" is high AND the input "$\overline{\text{ADS1D}}$" is high AND the input "CLKA" is low, OR
2. the output "$\overline{\text{READ}}$" is low AND the input "$\overline{\text{ADS1D}}$" is low, OR
3. the output "$\overline{\text{READ}}$" is low AND the input "CLKA" is high

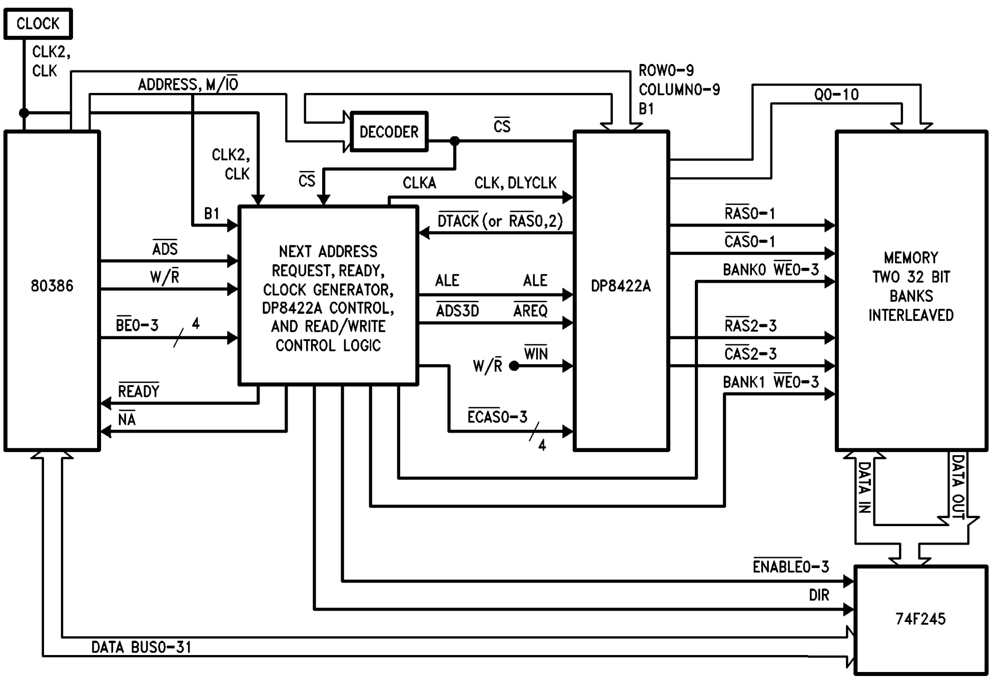


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FIGURE 1. 80386 Design #1 (A and B), System Block Diagram for Address Pipelined Mode Operation at up to 50 MHz (DP8422A Uses Half Speed Clock, CLKA)

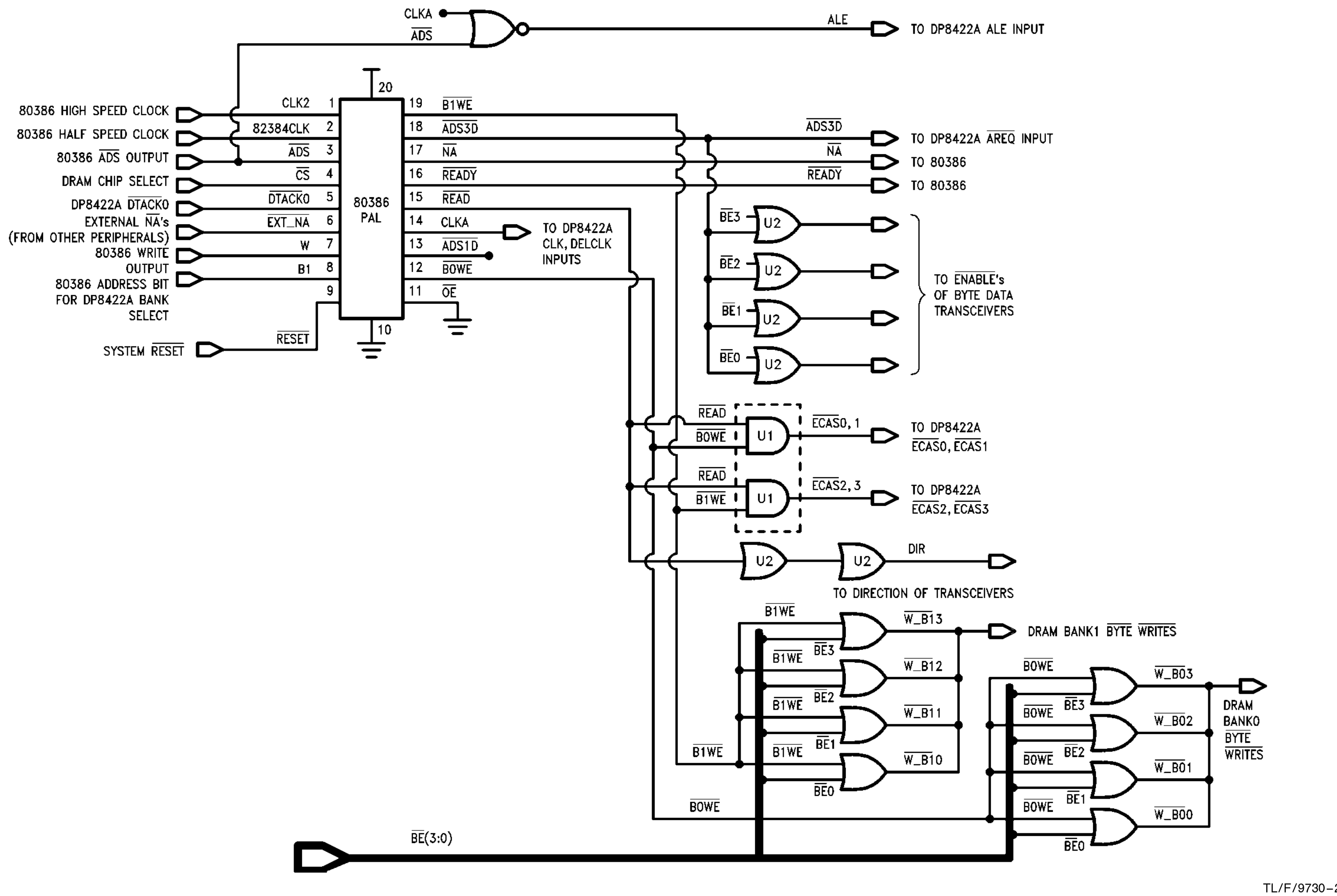

FIGURE 2. 80386/DP8422A Interface Control Logic for Design #1A

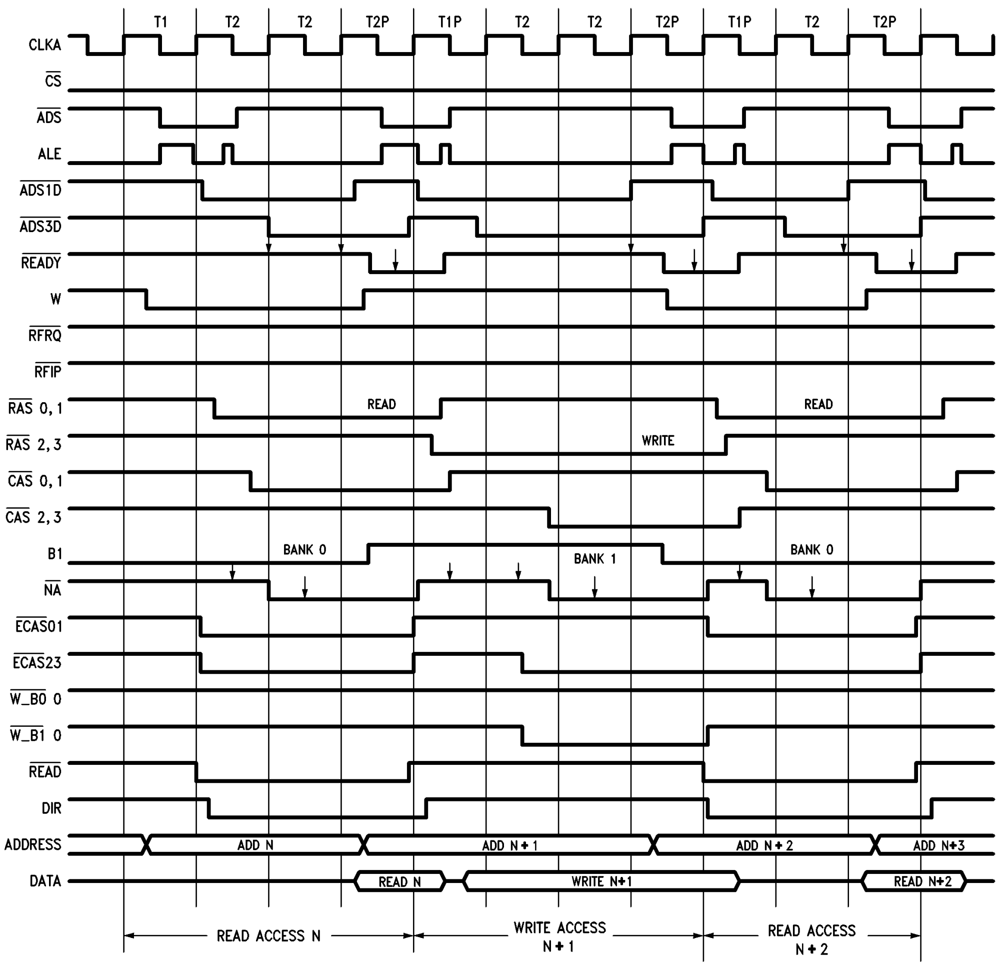

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FIGURE 3. 80386 Design #1 (A and B) Address Pipelined Timing

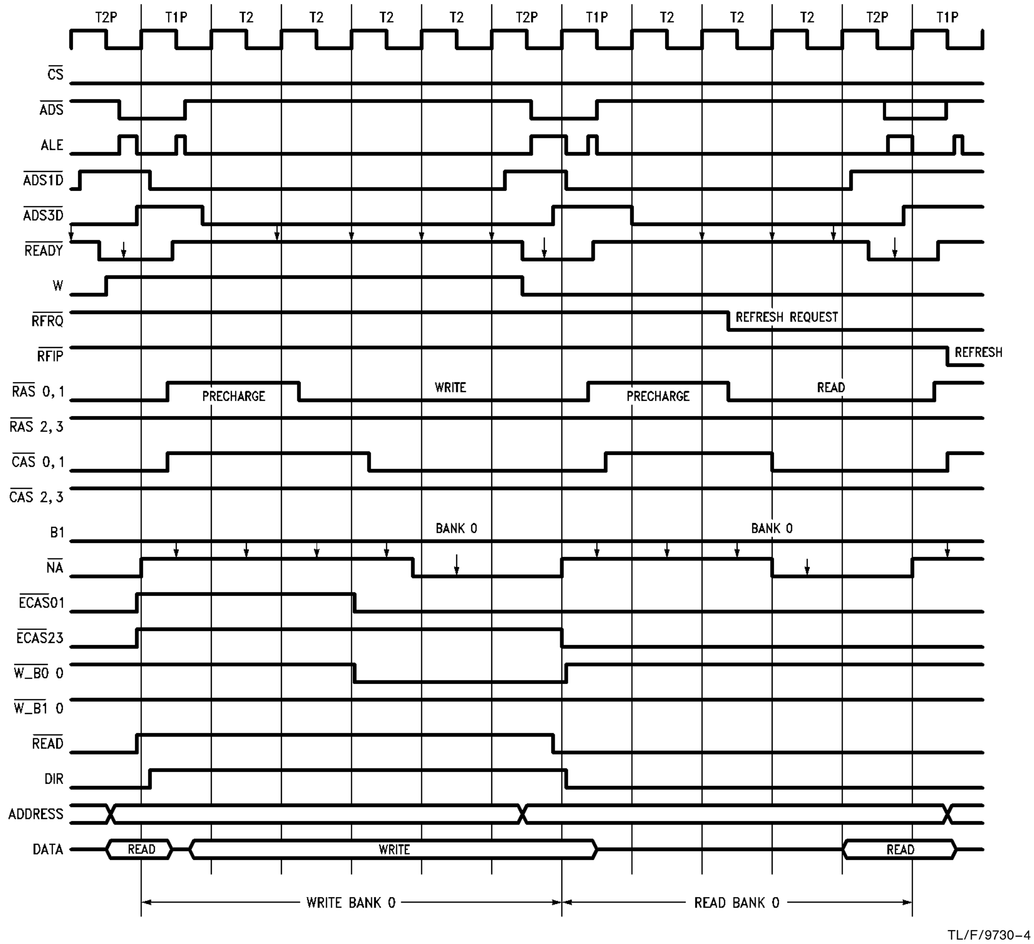

FIGURE 4. 80386 Design #1 Address Pipelined Timing

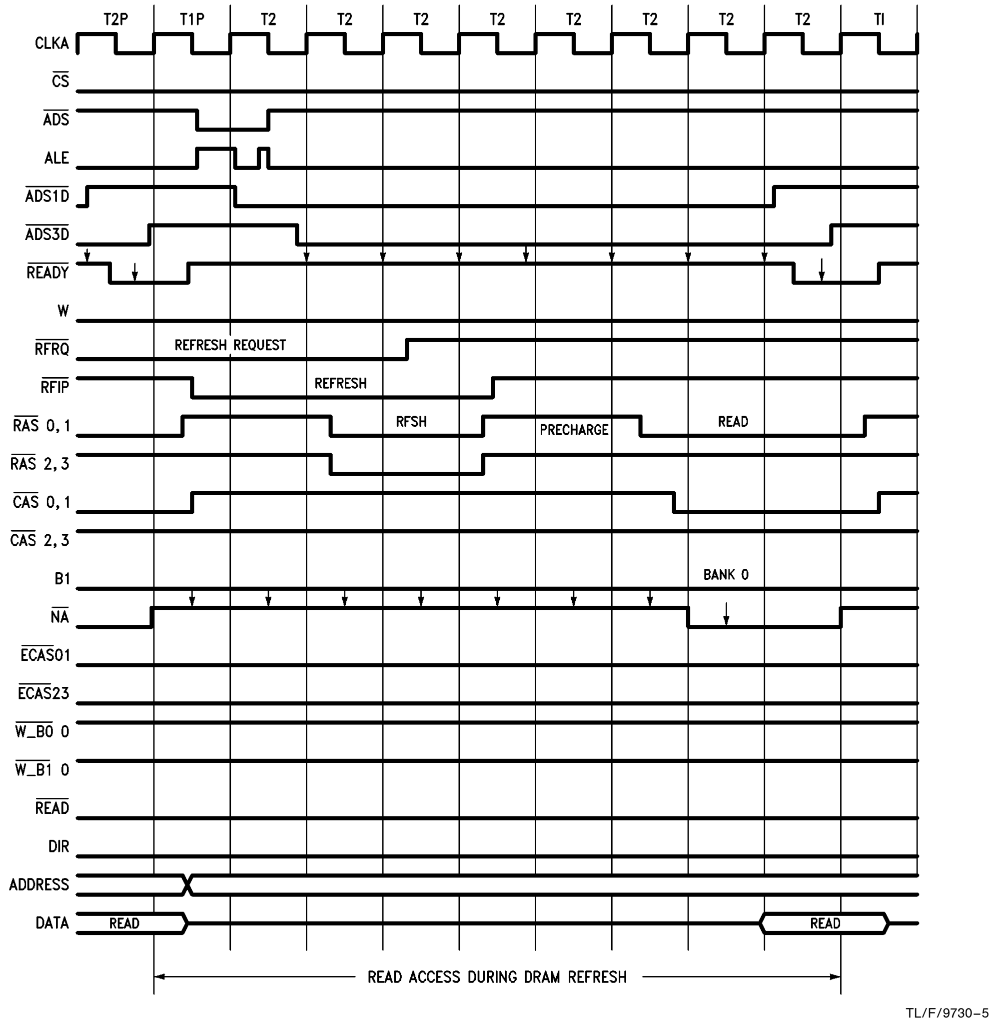

FIGURE 5. 80386 Design #1 Address Pipelined Timing

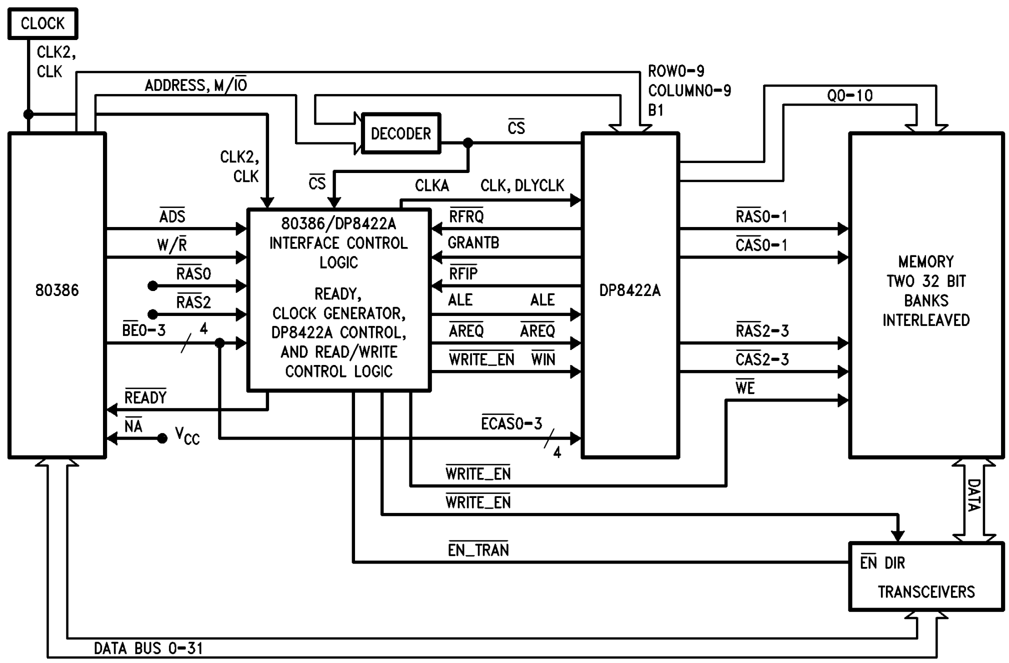

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FIGURE 6. 80386 Design #2(A, B, C) System Block Diagram for Non-Address Pipelined Mode Operation at up to 50 MHz (DP8422A Uses One Half Speed Clock)

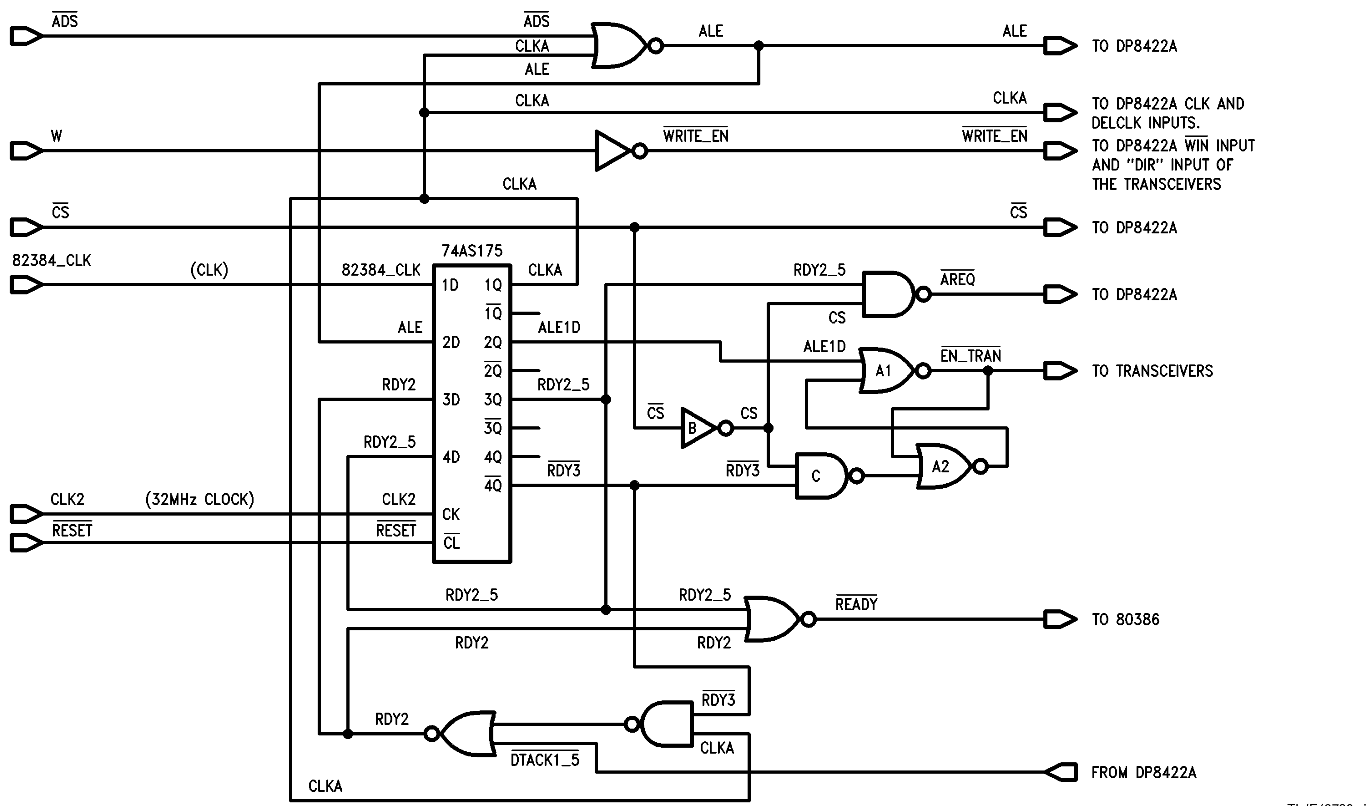

FIGURE 7a. 80386/DP8422 Interface Control Logic for Design #2A

```
PAL16R4D
CLK2 82384_CLK CS~ ADS~ W DTACK1~ NC1 NC2 NC3 GND
OE~ NC4 NC5 RDY_D~ READY~ AREQ~ CLKA ALE WRITE_EN~ VCC

IF (VCC) WRITE_EN~ = W * /AREQ~

IF (VCC) ALE = /ADS~ * /CLKA * AREQ~

CLKA := /82384_CLK

AREQ~ := /CS~ * ALE * /CLKA
        + /AREQ~ * /CS~ * READY~ * RDY_D~

READY~ := /CS~ * /AREQ~ * /DTACK1~ * RDY_D~ * /CLKA
         + /READY~ * /CS~ * /AREQ~ * RDY_D~

RDY_D~ := /CS~ * /AREQ~ * /DTACK1~ * /READY~
```

FIGURE 7B Design #2B: 80386 Non-Pipelined PAL (up to 20 MHz)

```
PAL16R4E
CLK2 82384_CLK CS~ ADS~ W DTACK2~ NC1 NC2 NC3 GND
OE~ NC4 READY~ RDY_D~ NC5 AREQ~ CLKA ALE WRITE_EN~ VCC

IF (VCC) WRITE_EN~ = W * /AREQ~

IF (VCC) ALE = /ADS~ * /CLKA * AREQ~

IF (VCC) READY~ = /CS~ * /AREQ~ * /DTACK2~ * RDY_D~ * CLKA
         +/READY~ * /CS~ * /AREQ~ * /CLKA

CLKA := /82384_CLK

AREQ~ := /CS~ * ALE * /CLKA
        + /AREQ~ * /CS~ * READY~ * RDY_D~

RDY_D~ := /CS~ * /AREQ~ * /DTACK2~ * CLKA
         +/RDY_D~ * /READY~ * /AREQ~
         +/RDY_D~ * /CLKA
```

If the PAL design is used, the timing diagrams of *FIGURES 8, 9, 10* will be the same with the exception of $\overline{\text{AREQ}}$ which will look like the $\overline{\text{EN\_\_TRAN}}$ waveform. The $\overline{\text{AREQ}}$ output will drive $\overline{\text{EN\_\_TRAN}}$. The meaning of AREQ~ is the same $\overline{\text{AREQ}}$.

FIGURE 7C. Design #2C: 80386 Non-pipelined PAL (up to 25 MHz. In this PAL design an external 74F74 Flip-Flop is used to capture 'DTACK1~' which has a setup time of [40 ns−7.5 ns (CLKA delay) − 28 ns (DTACK1~ delay) =] 4.5 ns. This 4.5 ns setup time is too small for any current PAL to capture. The captured 'DTACK1~' is called 'DTACK2~').

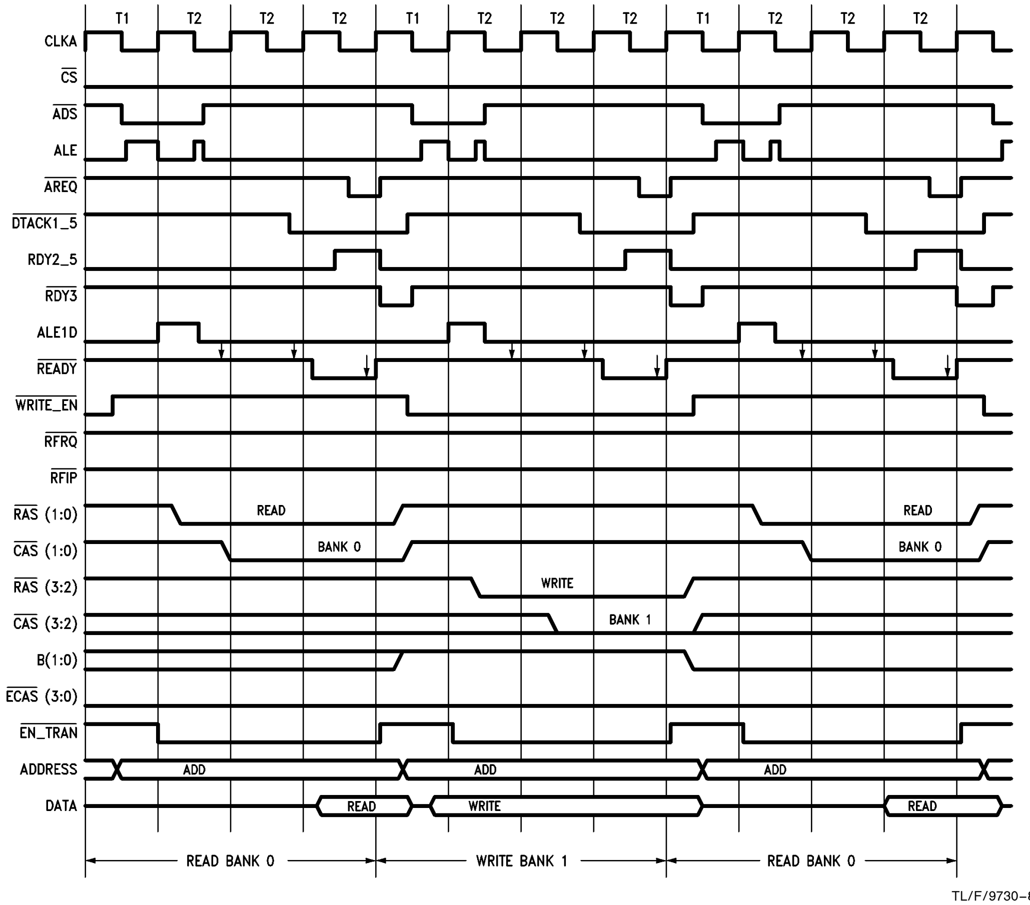

FIGURE 8. 80386 Design #2(A, B, C) Non-Address Pipelined Timing

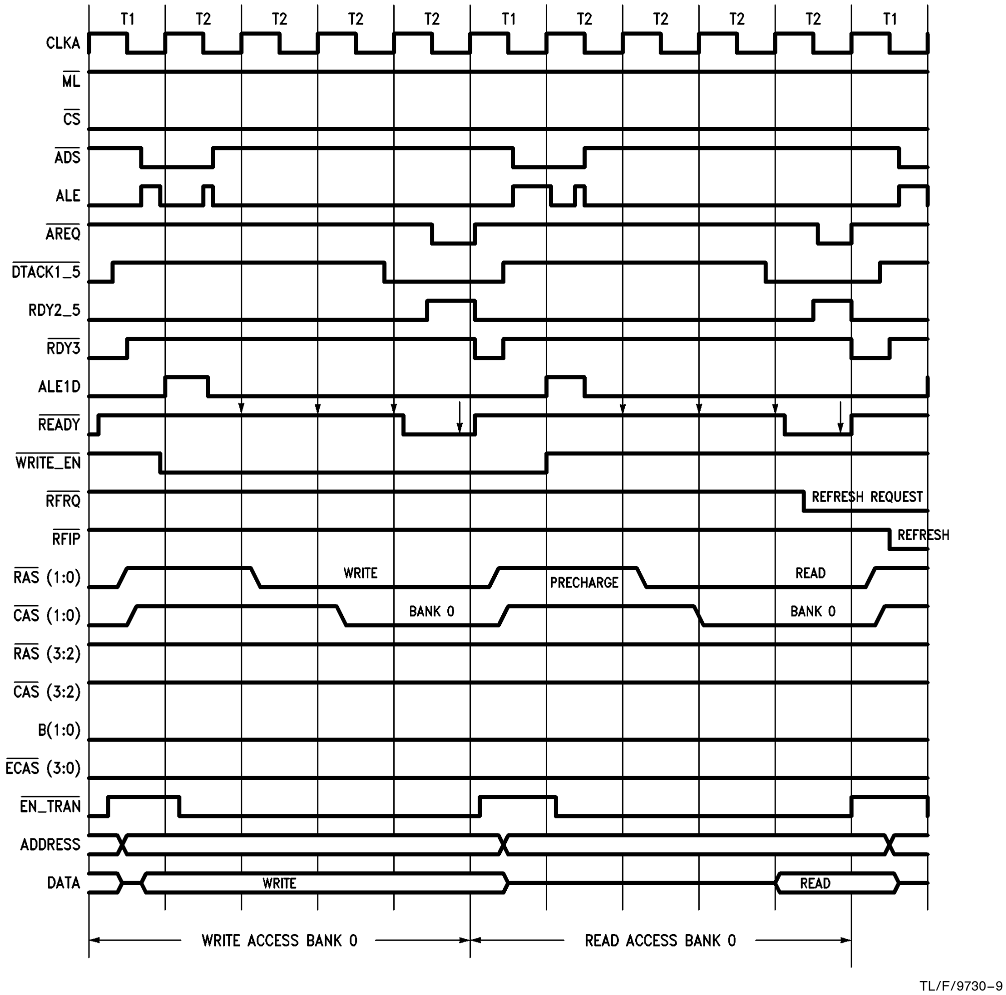

FIGURE 9. 80386 Design #2(A, B, C) Non-Address Pipelined Timing

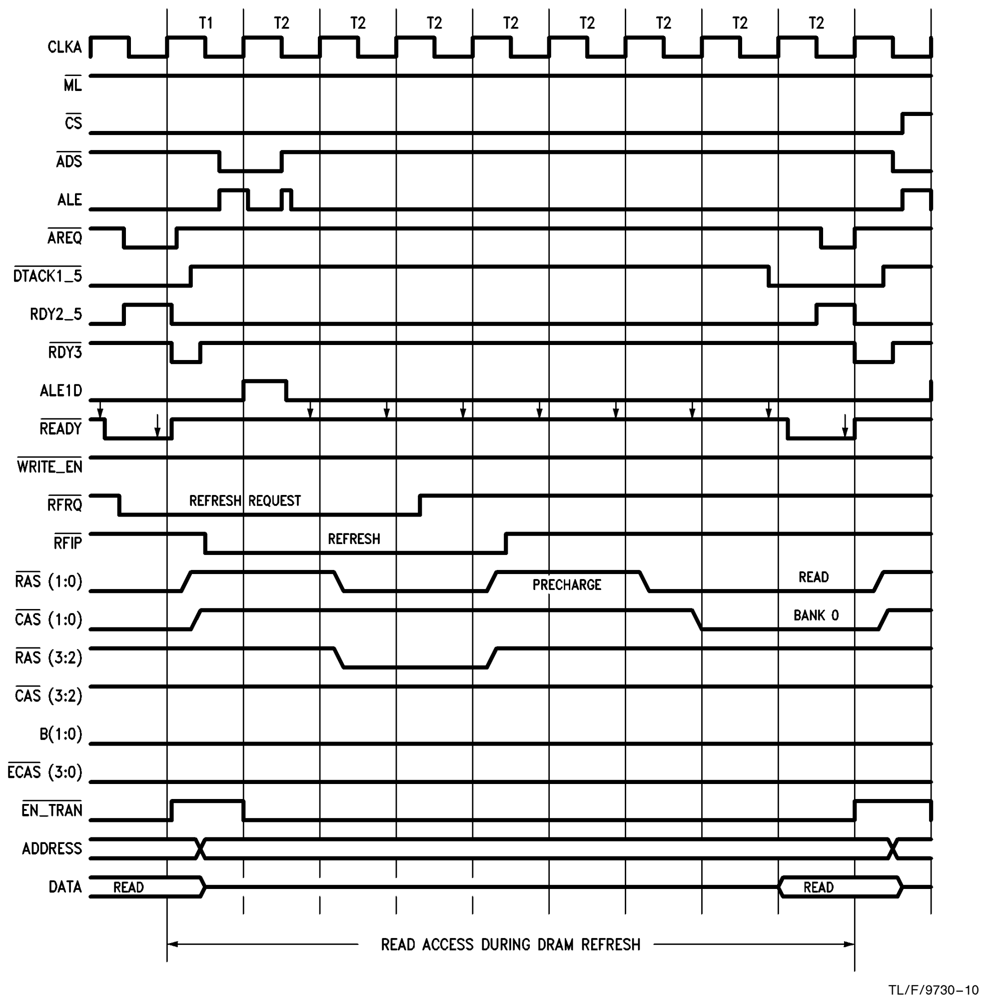

FIGURE 10. 80386 Design #2(A, B, C) Non-Address Pipelined Timing

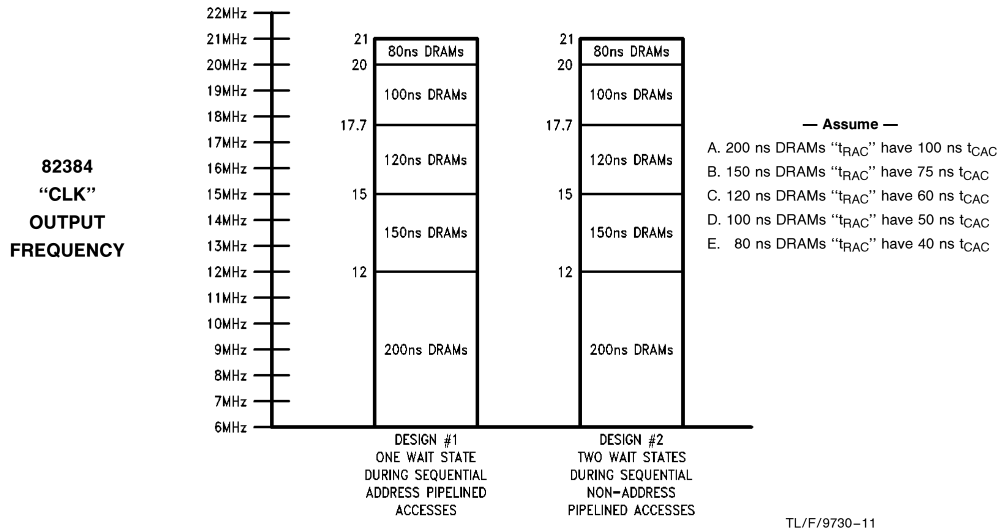

FIGURE 11. 80386 Design #1 and #2, DRAM Speed Verses Processor Speed (The Processor Speed is Referencing the 82384 "CLK" Output, The DRAM Speed is Referencing the $\overline{RAS}$ Access Time "t_{RAC}" of the DRAM)

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