Interfacing the DP8420A/21A/22A to the 68030 Microprocessor

National Semiconductor
Application Note 537
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I. INTRODUCTION

This application note describes how to interface the 68030 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). It is assumed that the reader is already familiar with 68030 and the DP8422A modes of operation.

II. DESCRIPTION OF DESIGN, ALLOWING UP TO 25 MHz OPERATION WITH 2, 3 OR 4 WAIT STATES IN NORMAL ACCESSES AND 1 OR 2 WAIT STATES DURING BURST ACCESSES

This design drives two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4 Mbit x 1 DRAMs). By choosing a different $\overline{RAS}$ and $\overline{CAS}$ configuration mode (See Programming Mode Bits Section of DP8422A Data Sheet) this application can support 4 banks of DRAM, giving a memory capacity of 64 Mbytes (using 4 Mbit x 1 DRAMs, NOTE that when driving 64 Mbytes the timing calculations will have to be adjusted to the greater capacitive load).

The memory banks are interleaved on every four word (32-bit word) boundry. This means that the address bit (A4) is tied to the bank select input of the DP8422A (B1). Address bits A3, 2 are tied to the highest row and column address inputs to support nibble mode burst accesses (using nibble mode DRAMs). Address bits A1, 0 are used to produce the four byte select data strobes, used in byte reads and writes. If the majority of accesses made by the 68030 are sequential, the 68030 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks, allowing one memory bank to be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed. This is a higher performance memory system then a non-interleaved memory system (bank select on the higher address bits). Each separate memory access to the same memory bank will generally require extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time.

This design supports the 68030 in its synchronous mode of operation. All DRAM accesses are terminated through the 68030 $\overline{STERM}$ input. The burst mode transfer operations are also supported using the synchronous mode of operation. To support these operations nibble mode DRAMs must be used. Nibble mode DRAMs are necessary to support wrap-around during a burst access.

This application allows 2, 3 or 4 wait states to be inserted in normal synchronous accesses and 1 or 2 wait states to be inserted during burst accesses of the 68030. The number of wait states can be adjusted through the $\overline{WAITIN}$ input of the DP8422A and the $\overline{ADDW}$ input of the PAL®, see the table below (the first two rows of the table can also be seen in the timing simulations that appear at the end of this application note):

$\overline{WAITIN}$	$\overline{ADDW}$	Number of Wait States In	
		Normal Access	Burst Access
0	0	4	2
0	1	3	1
1	0	3	2
1	1	2	1

The PAL has an input called "$\overline{EXST}$" that allows the user to setup the $\overline{STERM}$ for any other system peripheral to this PAL. This PAL will synchronize $\overline{EXST}$ to the system clock by gating it with a low logic level on the CLK input (for more information see the PAL equations in Section V). This allows one device to produce $\overline{STERM}$ to the 68030.

The logic shown in this application note forms a complete 68030 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

a. Arbitration between Port A, Port B, and refreshing the DRAM;

b. The insertion of wait states to the processor (Port A and Port B) when needed (i.e, if $\overline{RAS}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc.);

c. Performing byte writes and reads to the 32-bit words in memory;

d. Normal and burst access operations.

By making use of the enable input on the 74AS244 buffer, this application can easily be used in a dual access application. The addresses and chip select are tri-stated through this buffer, the write input ($\overline{WIN}$), lock input ($\overline{LOCK}$), and $\overline{ECAS}0-3$ inputs must also be able to be tri-stated (another 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. If this design is used in a dual access application at 25 MHz the t_{RAC} and t_{CAC} (require $\overline{RAS}$ and $\overline{CAS}$ access time required by the DRAM) will have to be recalculated since the time to $\overline{RAS}$ and $\overline{CAS}$ is longer for the dual access application (See TIMING Section of this application note).

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III. 68030 DESIGN, UP TO 25 MHz WITH 2, 3 OR 4 WAIT STATES DURING NORMAL ACCESSES AND 1 OR 2 WAIT STATES DURING BURST ACCESSES, PROGRAMMING MODE BITS

Programming

Bits	Description
R0 = 1	$\overline{RAS}$ low four clocks, $\overline{RAS}$ precharge of three clocks
R1 = 1	
R2 = 1	$\overline{DTACK}$1 is chosen. $\overline{DTACK}$ low first rising CLK edge after access $\overline{RAS}$ is low.
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. $\overline{WAITIN}$ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access.
R7 = 1	Select $\overline{DTACK}$
R8 = 1	Non-Interleaved Mode
R9 = X	
C0 = X C1 = X C2 = X	Select based upon the input "DELCLK" frequency. Example: if the input clock frequency is 20 MHz then choose C0, 1, 2 = 0, 0, 0 (divide by ten, this will give a frequency of 2 MHz). If using the DP8422A over 20 MHz do an initial divide by two externally and then run that output into the DELCLK input and choose the correct divider.
C3 = X	
C4 = 0 C5 = 0 C6 = 1	$\overline{RAS}$ groups selected by "B1". This mode allows two $\overline{RAS}$ outputs to go low during an access, and allows byte writing in 32-bit words.
C7 = 1	Column address setup time of 0 ns.
C8 = 1	Row address hold time of 15 ns.
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1	Fall-thru latches
B1 = 1	Access mode 1
$\overline{ECAS0}$ = 0	$\overline{CAS}$ not extended beyond $\overline{RAS}$

0 = Program with low voltage level

1 = Program with high voltage level

X = Program with either high or low voltage level (don't care condition)

IV. 68030 TIMING CALCULATIONS FOR DESIGN AT 25 MHz WITH 4 WAIT STATES DURING THE NORMAL ACCESSES AND 2 WAIT STATES DURING BURST ACCESSES

1. Minimum $\overline{ADS}$ low setup time to $\overline{CLOCK}$ high for $\overline{DTACK}$ logic to work correctly (DP8422A–25 needs 25 ns):

   40 ns (one clock period) − 10 ns (PAL16R4D combinational output max) = 30 ns

2A. Minimum address setup time to $\overline{ADS}$ low (DP8422A–25 needs 14 ns):

   40 ns (one clock period) − 20 ns (assumed 68030 max time to address valid from CLK high) − 6.2 ns (74AS244 buffer delay max) + 2.5 ns (minimum PAL16R4D combinational output delay) = 16.3 ns

2B. Minimum address setup time to CLK high (used in #3B calculation below):

   40 ns (one clock period) − 20 ns (assumed 68030 max time to address valid from CLK high) − 6.2 ns (74AS244 buffer delay max) = 13.8 ns

3A. Minimum $\overline{CS}$ setup time to $\overline{ADS}$ low (DP8422A–25 needs 5 ns):

   16.3 ns (#2A) − 9 ns (max 74AS138 decoder) = 7.3 ns

3B. Minimum $\overline{CS}$ setup time to CLK high (PAL equations need 0 ns):

   13.8 ns (#2B) − 9 ns (max 74AS138 decoder) = 4.8 ns

4. Determining t_{RAC} during a normal access ($\overline{RAS}$ access time needed by the DRAM):

   180 ns (four and one half clock periods to do the access) − 10 ns (PAL16R4D combinational output, $\overline{ADS}$) − 29 ns ($\overline{ADS}$ to $\overline{RAS}$ low) − 5 ns (68030 data setup time) − 7 ns (74F245) = 129 ns.

   Therefore the t_{RAC} of the DRAM must be 129 ns or less.

5. Determining t_{CAC} during a normal access ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   180 ns − 10 ns − 5 ns − 7 ns − 75 ns ($\overline{ADS}$ to $\overline{CAS}$ low on DP8422A–25, 50 pF spec) −12 ns [74AS32, 6 ns plus 6 ns extra, taken from lab data on the 74AS32, for driving a 22Ω damping resister and 150 pF of capacitance associated with driving 16 DRAM $\overline{CAS}$ inputs (per $\overline{CAS}$ output)] = 71 ns.

   Therefore the t_{CAC} of the DRAM must be 71 ns or less.

6. Determining the nibble mode access time needed during a burst access:

   120 ns (three clock periods to do the burst) − 20 ns (one half clock period during which $\overline{CAS}$ is high from the previous access) − 20 ns (the data is sampled on a faling clock edge) − 10 ns (PAL16R4D combinational output from CLK input falling edge, $\overline{ENCAS}$) − 12 ns (74AS32 delay to produce $\overline{CAS}$ from the $\overline{ENCAS}$ input, see discription from #5) − 5 ns (68030 data setup time) − 7 ns (74F245) = 46 ns.

   Therefore the nibble mode access time of the DRAM must be 46 ns or less.

7. Maximum time to $\overline{DTACK}$2 low (PAL16RD needs 10 ns setup to CLK):

   40 ns (One clock) − 28 ns ($\overline{DTACK}$2 low from CLK high on DP8422A–25) = 12 ns

8. Minimum $\overline{STERM}$ setup time to CLK (0 ns to CLK rising edge is needed by the 68030):

   20 ns (one half clock period) − 10 ns (PAL16R4D combinational output maximum) = 10 ns

** Note: That calculations can be performed for different frequencies and/or different combinations of wait states by substituting the appropriate values into the above equations.

V. 68030 Design, PAL Equations Written in National Semiconductor PLAN™ Format

```
PAL16R4D
BCLK /CS /AS NC1 /DTACK /EXST /ADDW CLK NC2 GND
/OE  /STERM /DC NC3 /DB /DA NC4 /ENCAS /AREQ VCC

IF (VCC) /AREQ = /AS * /CS * CLK
               + /AREQ * /CS * /CLK

IF (VCC) /ENCAS = /AREQ * /CS * DC
                + /AREQ * /CS * /CLK

IF (VCC) /DC =   /AS * /CS * /DB * /CLK
                 + /AS * /CS * /DC * CLK

IF (VCC) /STERM = /AS * /CS * /DA * DB * /CLK * /ADDW
                  + /AS * /CS * /DTACK * DB * /CLK * ADDW
                  + /EXST * /CLK
                  + /STERM * CLK

*** ''IF (/CS) /STERM'' could be used if the user desires to wire ''OR''
          /STERM outputs together from other peripherals.
/DA: = /AREQ * /CS * /DTACK * DB * /ADDW
/DB: = /AREQ * /CS * /DTACK * /DA * DB * /ADDW
       + /AREQ * /CS * /DTACK * DB * ADDW
```

KEY: READING PAL EQUATIONS WRITTEN IN PLAN

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EXAMPLE EQUATIONS: IF (VCC) /DC = /AS * /CS * /DB * /CLK
                                  + /AS * /CS * /DC * CLK
```

This example reads: the output "/DC" will transition low given that one of the following conditions are valid:

1. The input "/AS" low AND the input "/CS" is low AND the output "/DB" is low and the input "CLK" is low, OR
2. The input "/AS" is low AND the input "/CS" is low AND the output "/DC" is low and the input "CLK" is high.

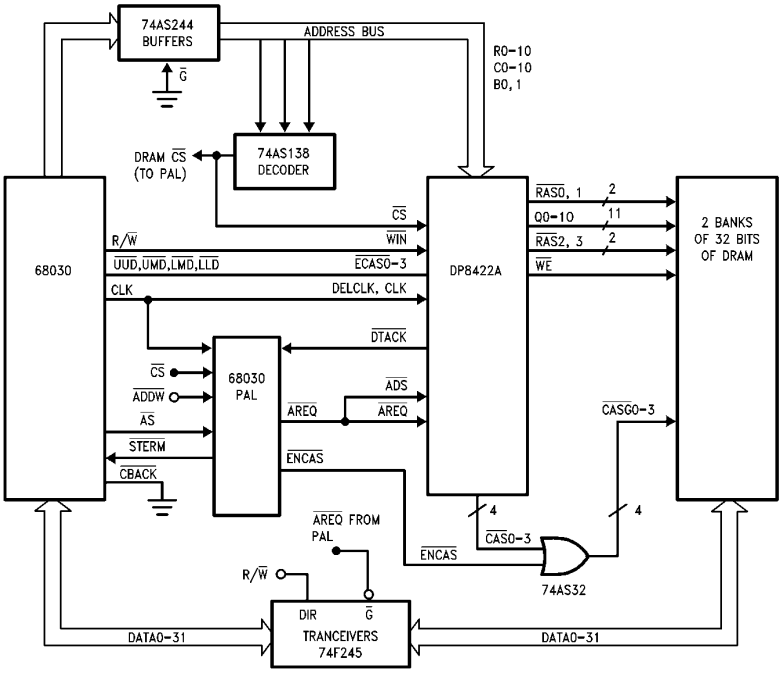

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FIGURE 1. 68030 Design, up to 25 MHz, with 2, 3 or 4 Wait States in Normal Accesses and 1 or 2 Wait State in Burst Accesses

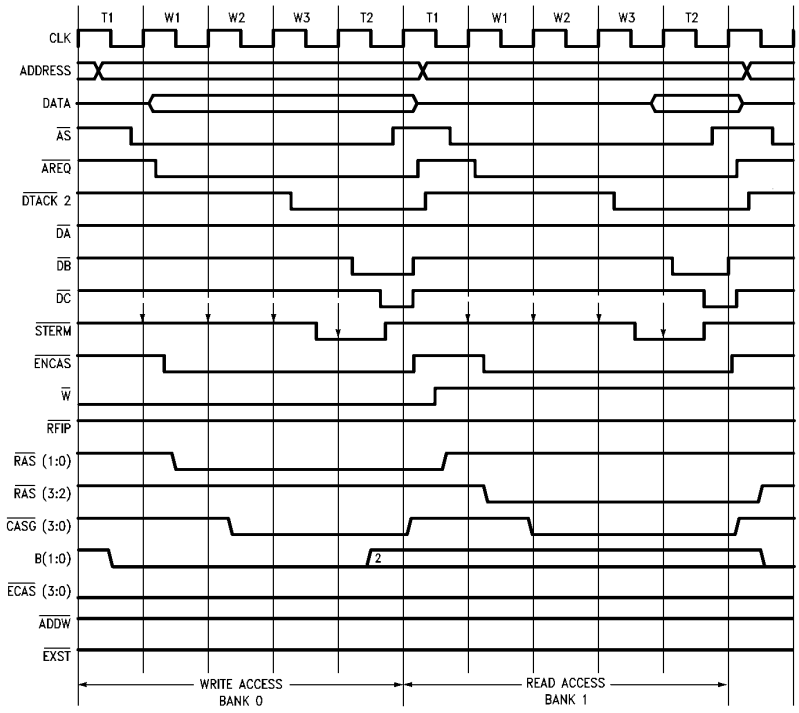

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FIGURE 2. 68030 Timing, 3 Wait States during Synchronous Accesses ($\overline{\text{ADDW}}$ = High)

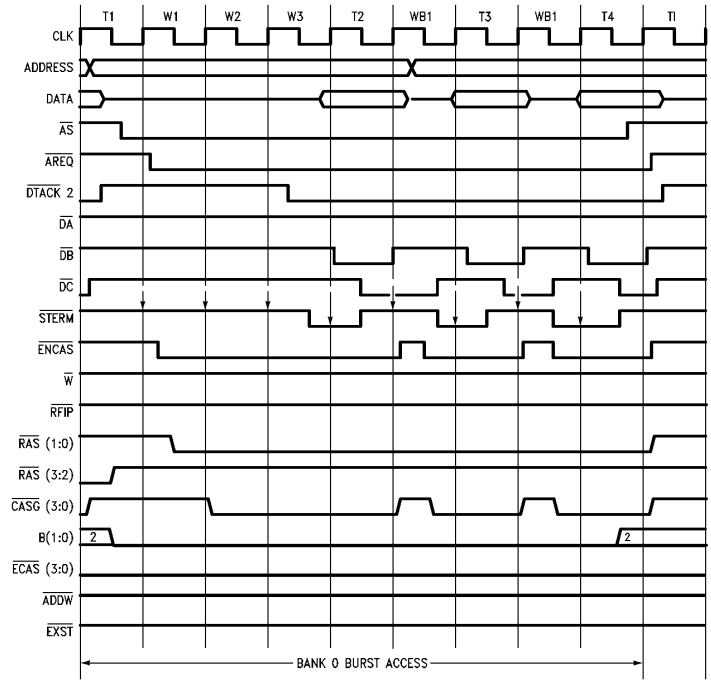

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FIGURE 3. 68030 Timing, 3 Wait States during Synchronous Accesses and 1 Wait State during Burst Accesses ($\overline{\text{ADDW}}$ = High)

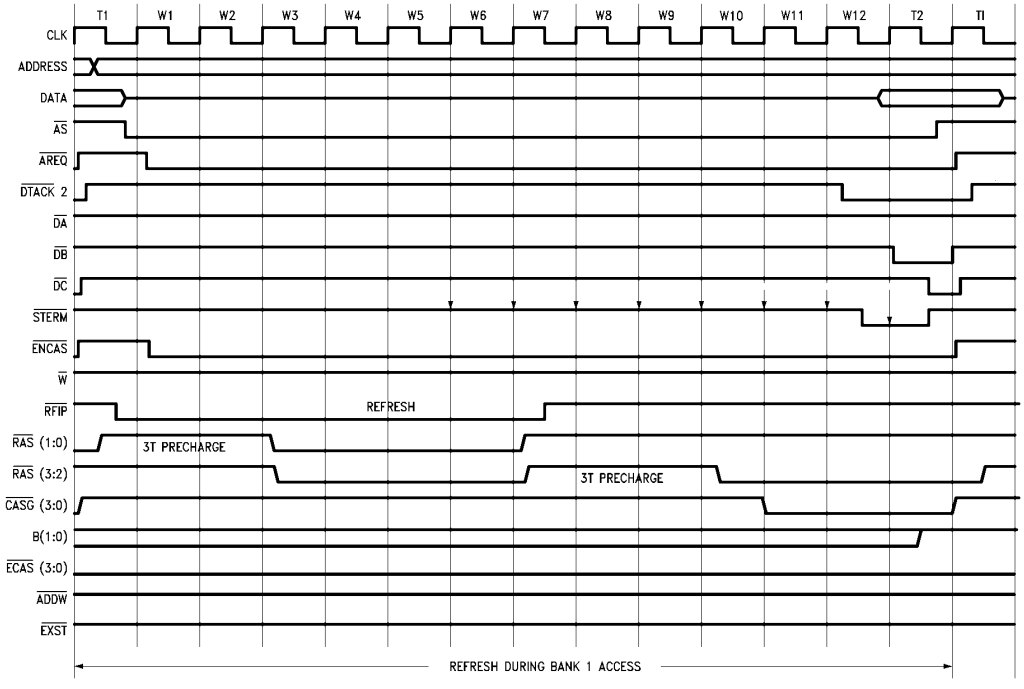

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FIGURE 4. 68030 Timing, 3 Wait States during Synchronous Accesses ($\overline{\text{ADDW}}$ = High)

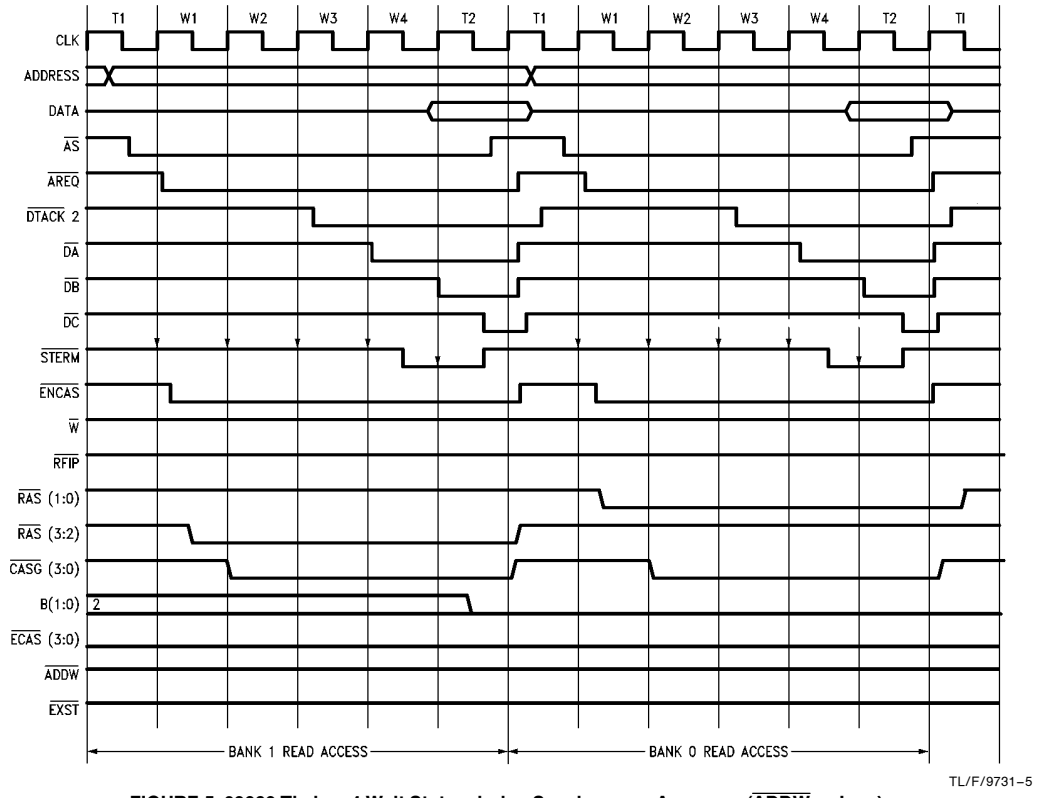

FIGURE 5. 68030 Timing, 4 Wait States during Synchronous Accesses ($\overline{ADDW}$ = Low)

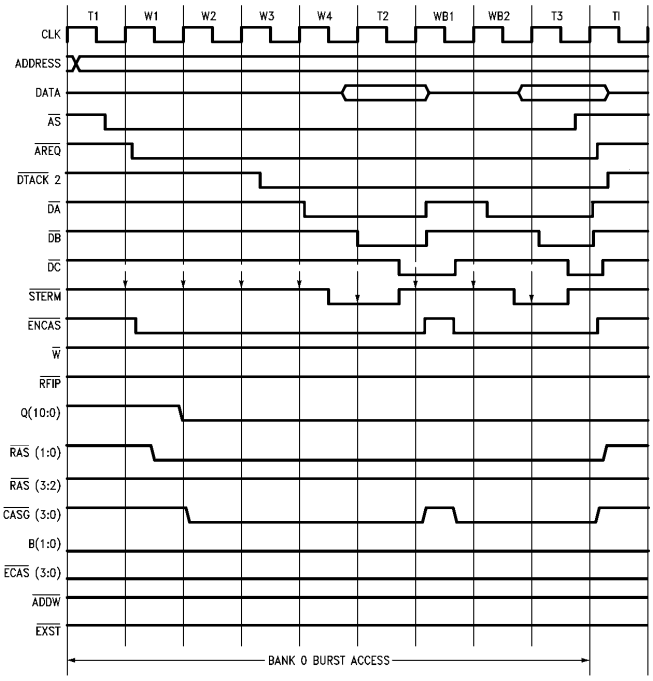

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FIGURE 6. 68030 Timing, 4 Wait States during Synchronous Accesses and 2 Wait States during Burst Accesses ($\overline{ADDW}$ = Low)

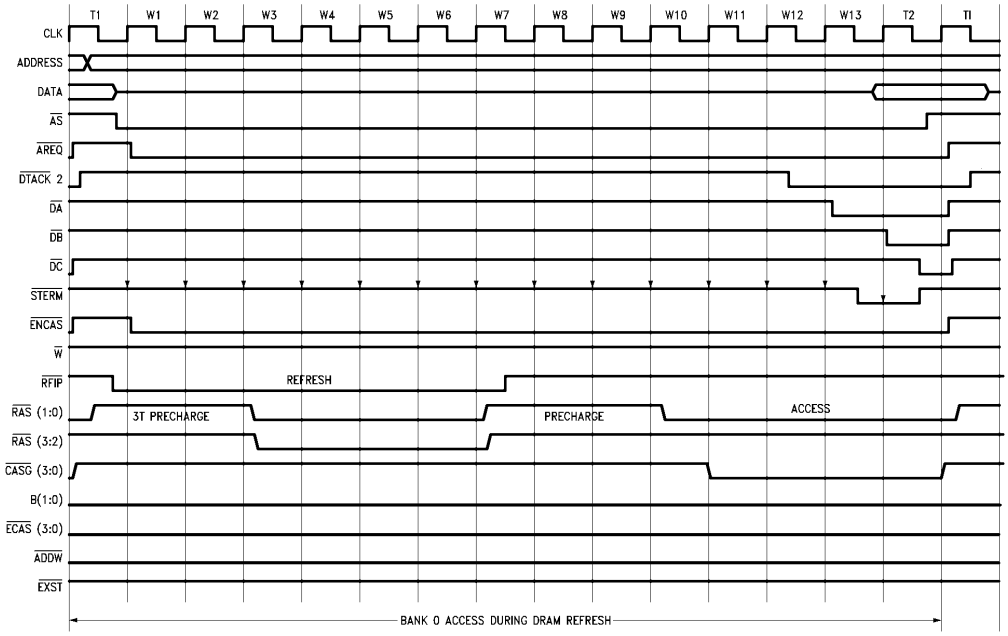

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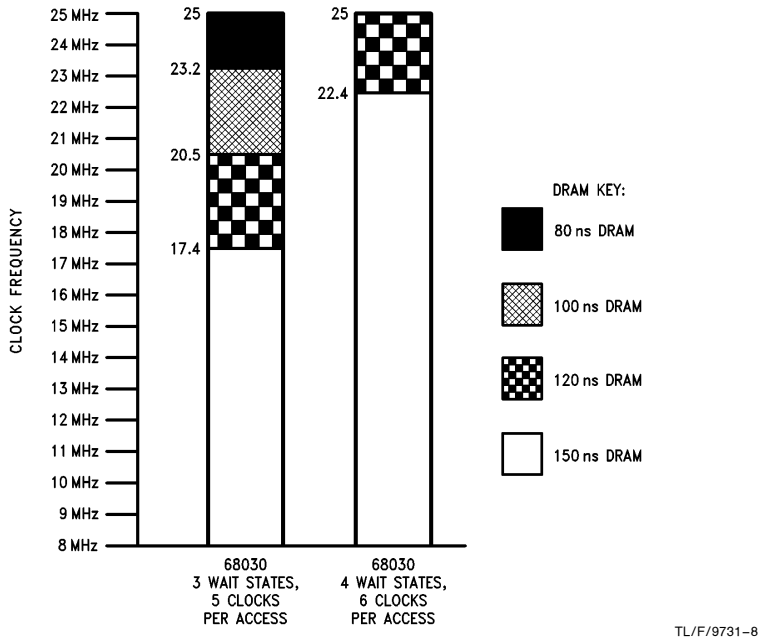
FIGURE 7. 68030 Timing, 4 Wait States during Synchronous Accesses ($\overline{ADDW}$ = Low)

DRAM Speed Versus Processor Speed (DRAM Speed References the RAS Access Time, tRAC, of the DRAM Using DP8422A-25 Timing Specifications)



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