Interfacing the DP8420A/21A/22A to the 68000/008/010

National Semiconductor
Application Note 538
Joe Tate and Rusty Meier
May 1989

INTRODUCTION

This application note explains interfacing the DP8420A/21A/22A DRAM controller to the 68000. Three different designs are shown and explained. It is assumed that the reader is familiar with the 68000 access cycles and the DP8420A/21A/22A modes of operation. This application note also applies to the 68010.

DESIGN #1 DESCRIPTION

Design #1 is a simple circuit to interface the 68000 to the DP8420A/21A/22A and up to 32 Mbytes of DRAM. The DP8420A/21A/22A is operated in Mode 1. An access cycle begins when the 68000 places a valid address on the address bus and asserts the address strobe ($\overline{AS}$). Chip select ($\overline{CS}$) is generated by a 74AS138 decoder. If a refresh or Port B access (DP8422A only) is not in progress, the DP8420A/21A/22A will assert the proper $\overline{RAS}$ depending on the bank select inputs (B0, B1). After guaranteeing the programmed value of row address hold time the DP8420A/21A/22A will switch the DRAM address (Q0–8, 9, 10) to the column address and assert $\overline{CAS}$. By this time, the 74AS245's have been enabled and the DRAMs place their data on the data bus. The DP8420A/21A/22A also asserts $\overline{DTACK}$ which is used to generate $\overline{DTACK}$ to the 68000 to complete the access.

If a refresh or Port B access had been in progress, the DP8420A/21A/22A would have delayed the 68000's access by inserting wait states into the access cycle until the refresh or Port B access was complete and the programmed amount of precharge time was met. This circuit can run up to 10 MHz with 0 wait states, with two or more banks. For 10 MHz, zero wait states with one bank, see design #2.

Timing parameters are referenced to the numbers shown in the DP8420A/21A/22A data sheet timing parameters. Numbered times starting with a "$" refer to the DP8420A/21A/22A timing parameters. Numbered times starting with "#" refer to the 68000 data sheet. Equations have been given to allow the user to calculate timing based on his frequency and application. The clock is at 10 MHz, a multiple of 2 MHz, allowing it to be tied directly to DELCLK. If DELCLK is not a multiple of 2 MHz, $\overline{ADS}$ to $\overline{CAS}$ must be recalculated.

DESIGN #1 TIMING AT 10 MHz AND 8 MHz

Clock Period = Tcp10 = 100 ns @ 10 MHz
= Tcp8 = 125 ns @ 8 ns

$400b: $\overline{ADS}$ Asserted Setup to CLK High
= Clock Period − CLK High to $\overline{AS}$ Asserted
= Tcp10 − #9
= 100 ns − 55 ns
= **45 ns @ 10 MHz**
= Tcp8 − #9
= 125 ns − 60 ns
= **65 ns @ 8 MHz**

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted
= 68000 Address to $\overline{AS}$ Max
− 74AS138 Decoder
= #11 − TphI Max
= 20 ns − 9 ns
= **11 ns @ 10 MHz**
= #11 − TphI
= 30 ns − 9 ns
= **21 ns @ 8 MHz**

$407 & $404: Address Valid Setup to $\overline{ADS}$ Asserted
= 68000 Address to $\overline{AS}$ Max
= #11 Max
= **20 ns @ 10 MHz**
= #11 Max
= **30 ns @ 8 MHz**

$405: $\overline{ADS}$ Negated Held from CLK High
= 68000 CLK High to $\overline{AS}$ Asserted Min
= #10 Min
= **0 ns @ 10 MHz**
= #10 Min
= **0 ns @ 8 MHz**

#47: DTACK Setup Time
= ½ Clock Period
− Clock to $\overline{DTACK}$ Asserted
= ½ Tcp10 − $18
= 50 ns − 28 ns
= **22 ns @ 10 MHz** **Using 8420-25
= ½ Tcp8 − $18
= 62.5 ns − 33 ns
= **29.5 ns @ 8 MHz** **Using 8420-25

$\overline{RAS}$ LOW DURING REFRESH

tRAS = Programmed Clock
− [(CLK High to Refresh $\overline{RAS}$ Asserted)
− (CLK High to Refresh $\overline{RAS}$ Negated)]
= Tcp10 + Tcp10 − $55
= 100 ns + 100 ns − 6 ns
= **194 ns @ 10 MHz**
= Tcp8 + Tcp8 − $55
= 125 ns + 125 ns − 6 ns
= **244 ns @ 8 MHz**

 TL/F/9732

RRD-B30M115/Printed in U. S. A.

$\overline{RAS}$ PRECHARGE PARAMETERS**

tRP = (Programmed Clocks − 1)
− [($\overline{AREQ}$ to $\overline{RAS}$ Negated)
− (CLK to $\overline{RAS}$ Asserted)]
= Tcp10 − $50
= 100 ns − 16 ns
= **84 ns @ 10 MHz**
= Tcp8 − $50
= 125 ns − 16 ns
= **109 ns @ 8 MHz**

**To gain more precharge program 3t or use design #2.

tRAC AND tCAC FOR DRAMs

Timing is supplied for the system shown in *Figure 1*. *(see Figures 2, 3* and *4)*. Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 0 or 1 wait state. If DELCLK is not a multiple of 2 MHz, the timing for tRAH and tASC will increase or decrease according to the equations given in the data sheet. The $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also have to be changed depending on the capacitance of the DRAM array.

0 Wait States

tRAC = s2 + s3 + s4 + s5 + s6 − CLK to $\overline{AS}$ Asserted Max − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted − 74AS245 Delay Max − 68000 Data Setup Min
= 2½ Tcp10 − #9 − $402 − Tphl Max − #27
= 250 ns − 55 ns − 35 ns − 7 ns − 10 ns
= **143 ns @ 10 MHz** Using 8420-20 w/Heavy Load
= 2½ Tcp8 − #9 − $402 − Tphl Max − #27
= 312.5 ns − 60 ns − 35 ns − 7 ns − 15 ns
= **195 ns @ 8 MHz** Using 8420-20 w/Heavy Load

1 Wait State

tRAC = s2 + s3 + s4 + sw + sw + s5 + s6 − CLK to $\overline{AS}$ Asserted Max − $\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted − 74AS245 Delay Max − 68000 Data Setup Min
= 3½ Tcp10 − #9 − $402 − Tphl Max − #27
= 350 ns − 55 ns − 35 ns − 7 ns − 10 ns
= **243 ns @ 10 MHz** Using 8420-20 w/Heavy Load
= 3½ Tcp8 − #9 − $402 − Tphl Max − #27
= 437.5 ns − 60 ns − 35 ns − 7 ns − 15 ns
= **320 ns @ 8 MHz** Using 8420-20 w/Heavy Load

0 Wait States

tCAC = s2 + s3 + s4 + s5 + s6 − CLK to $\overline{AS}$ Asserted Max − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted − 74AS245 Delay Max − 68000 Data Setup Min
= 2½ Tcp10 − #9 − $403a − Tphl Max − #27
= 250 ns − 55 ns − 94 ns − 7 ns − 10 ns
= **84 ns @ 10 MHz** Using 8420-20 w/Heavy Load
= 2½ Tcp8 − #9 − $403a − Tphl Max − #27
= 312.5 ns − 60 ns − 94 ns − 7 ns − 15 ns
= **136 ns @ 8 MHz** Using 8420-20 w/Heavy Load

1 Wait State

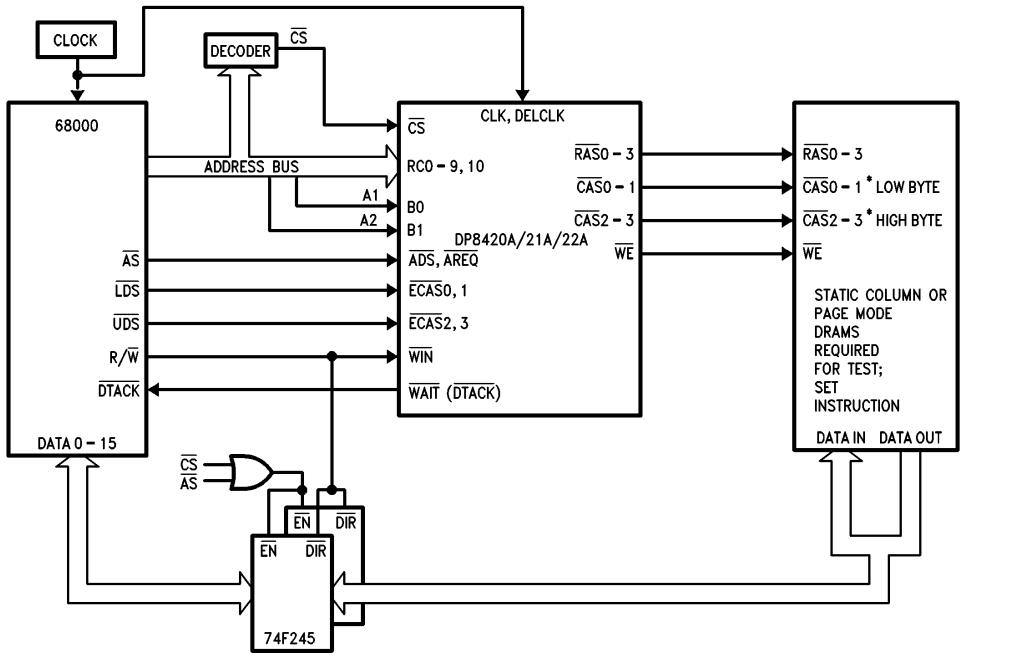
tCAC = s2 + s3 + s4 + sw + sw + s6 − CLK to $\overline{AS}$ Asserted Max − $\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted − 74AS245 Delay Max − 68000 Data Setup Min
= 3½ Tcp10 − #9 − $403a − Tphl Max − #27
= 350 ns − 55 ns − 94 ns − 7 ns − 10 ns
= **184 ns @ 10 MHz** Using 8420-20 w/Heavy Load
= 3½ Tcp8 − #9 − $403a − Tphl Max − #27
= 437.5 ns − 60 ns − 94 ns − 7 ns − 15 ns
= **261 ns @ 8 MHz** Using 8420-20 w/Heavy Load

Design #1 Programming Bits

Bits	Description	Value
R0, R1	$\overline{RAS}$ Low Time During REFRESH = 2T $\overline{RAS}$ Precharge Time = 2T	R0 = 0 R1 = 1
R2, R3	$\overline{DTACK}$ Generation Modes for Non-Burst Accesses	R2 = s R3 = s
R4, R5	$\overline{DTACK}$ Generation Modes for Burst Accesses	R4 = s R5 = s
R6	Add Wait States with $\overline{WAITIN}$	R6 = s
R7	$\overline{DTACK}$ Mode Select	R7 = 1
R8	Non Interleaved Mode	R8 = 1
R9	Staggered or All RAS REFRESH	R9 = u
C0, C1, C2	Divisor for DELCLK	C0 = s C1 = s C2 = s
C3	+30 REFRESH	C3 = 0
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode *Choose All $\overline{CAS}$ Mode	C4 = u C5 = u C6 = u
C7	Select 0 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Setup	C8 = 1
C9	CAS is Delayed to the Next Rising CLK Edge During Writes	C9 = 1
B0	The Row/Column Bank Latches Are Fall Through Mode	B0 = 1
B1	Access Mode 1	B1 = 1
$\overline{ECAS0}$	$\overline{CAS}$ Not Extended Beyond $\overline{RAS}$	$\overline{ECAS0}$ = 0

u = user defined **s = system dependent**

R2 = 1	R3 = 0		for 0 WAIT STATES
R2 = 1	R3 = 0	R6 = 0	for 1 WAIT STATE
C0 = 1	C1 = 0	C2 = 1	for 10 MHz
C0 = 0	C1 = 0	C2 = 1	for 8 MHz
R4 = 0	R5 = 0		for 0 WAIT STATES during write portion of test and set
R4 = 1	R5 = 1		for 1 WAIT STATE during write portion of test and set



TL/F/9732–1

FIGURE 1. 68000 Design # 1

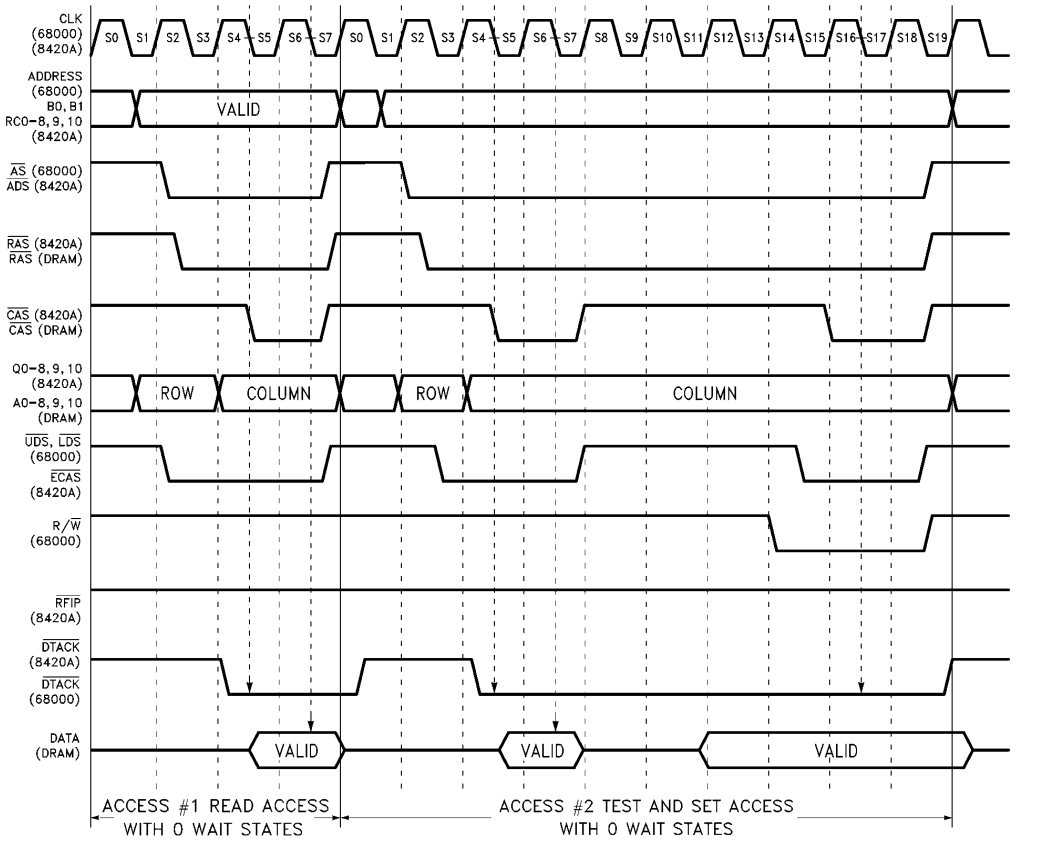
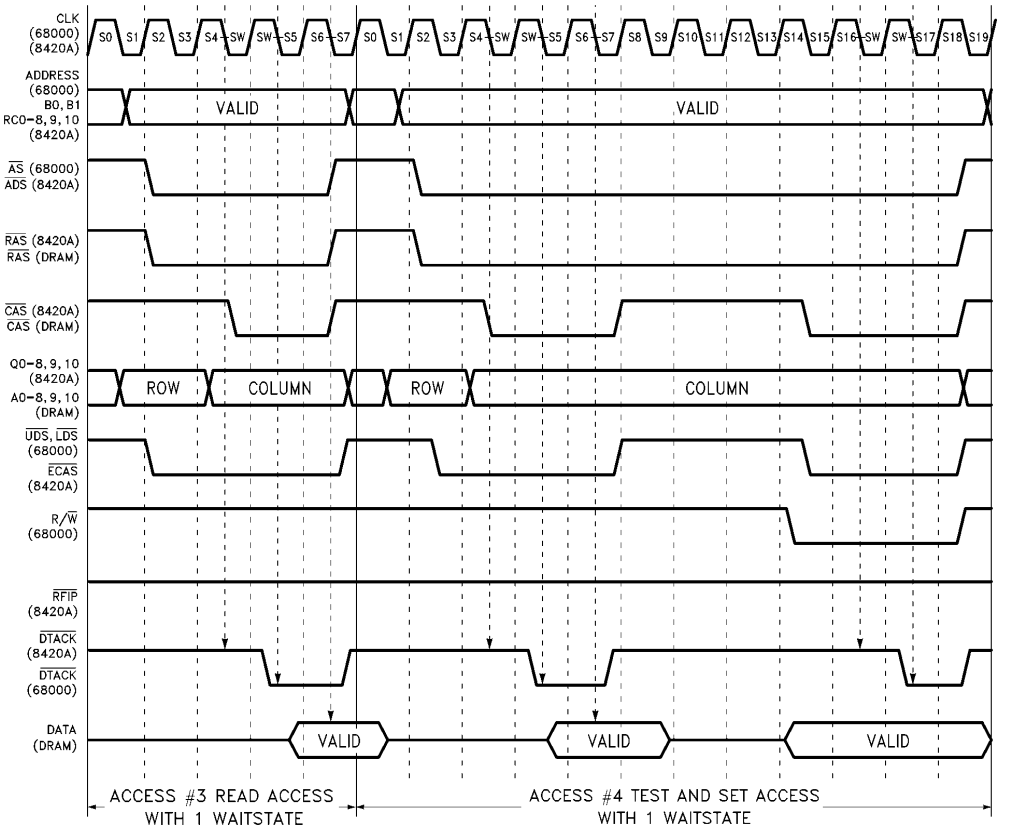
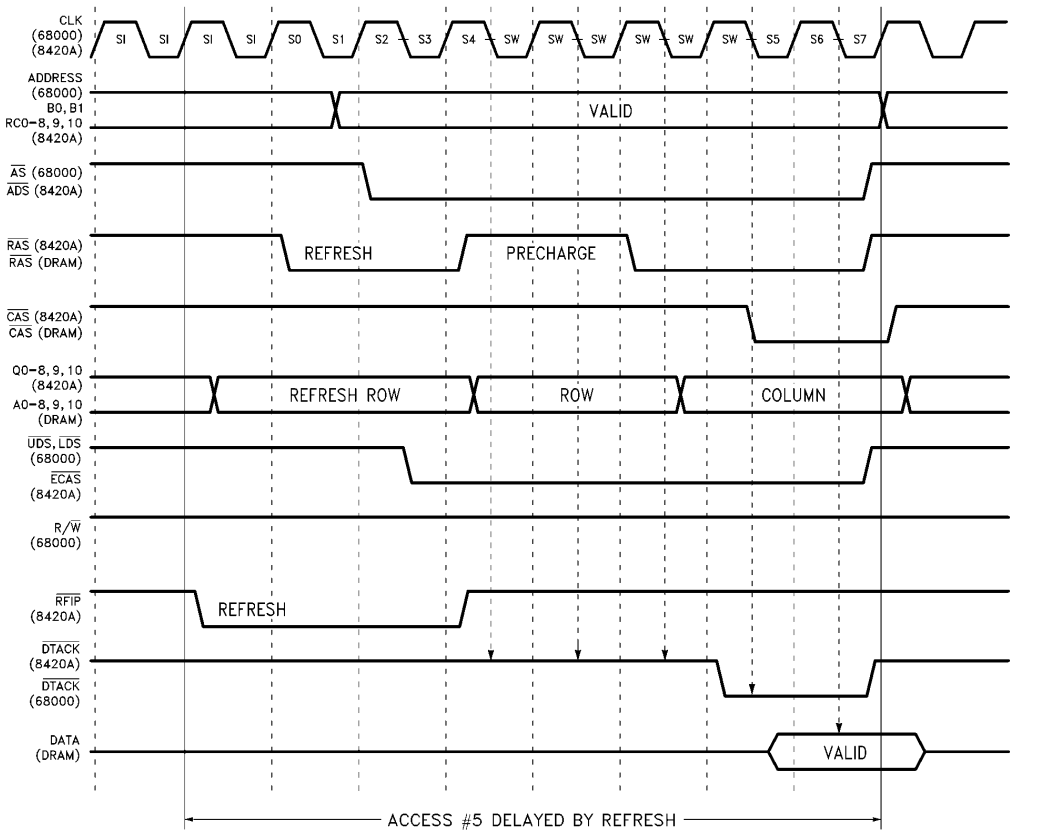


FIGURE 2. 68000 Design # 1 Timing



TL/F/9732–3

FIGURE 3. 68000 Design #1 Timing



TL/F/9732–4

FIGURE 4. 68000 Design # 1 Timing

DESIGN #2 DESCRIPTION

Design #2 differs from Design #1 in that the 68000 can be run up to 12.5 MHz. This design can also run with no wait states at 10 MHz if only one bank of DRAM is being used. A latch must be used with the 68000 address strobe to guarantee the address setup to $\overline{ADS}$ asserted requirement of the DP8420A/21A/22A. Again, the DP8420A/21A/22A is operated in Mode 1.

An access cycle begins when the 68000 places a valid address on the address bus at the beginning of processor state s1. At processor state s2, the 68000 asserts the address strobe, $\overline{AS}$. This signal is qualified with CLK low to set a latch. The output of this latch produces the signal $\overline{ADS}$ to the DP8420A/21A/22A. When the signal $\overline{ADS}$ is asserted on the DP8420A/21A/22A, the chip will assert $\overline{RAS}$. After guaranteeing the row address hold time, the 8420A/21A/22A will place the column address to the DRAM address bus. After guaranteeing the column address setup time, the DP8420A/21A/22A will assert $\overline{CAS}$. After time tCAC has passed, the DRAM will place its data on the data bus. The 8420A/21A/22A will assert the $\overline{DTACK}$ output allowing the bus cycle to end.

If a refresh of a Port B access had been in progress, the access would have been delayed by inserting wait states in the Port A access cycle.

DESIGN #2 TIMING AT 12.5 MHz

Clock Period = Tcp12 80 ns @ 12.5 MHz

$400b: $\overline{ADS}$ Asserted Setup to CLK High

= Clock Period + ½ Clock Period + 74AS04 Delay Min + 74AS04 Delay Min − Clock to AS Asserted Max − 74AS04 Delay Min − 74AS02 Delay Max − 74AS02 Delay Max

= Tcp12 + ½ Tcp12 + Tphl Min + Tphl Min − #9 − Tphl Min − Tphl Max − Tphl Max

= 80 ns + 40 ns + 1 ns + 1 ns − 55 ns − 1 ns − 4.5 ns − 4.5 ns

= 57 ns @ 12.5 MHz

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted

= Clock Period + 74AS04 Delay Min + 74AS04 Delay Min + 74AS02 Delay Min + 74AS02 Delay Min − 74AS04 Delay Min − Clock to ADR Max − 74AS138 Delay Max

= Tcp12 + Tphl Min + Tphl Min + Tphl Min + Tphl Min − Tphl Min − #6 − Tphl Max

= 80 ns + 1 ns + 1 ns + 1 ns + 1 ns − 1 ns − 55 ns − 9 ns

= 19 ns @ 12.5 MHz

$407 & $404: Address Valid to $\overline{ADS}$ Asserted

= Clock Period + 74AS04 Delay Min + 74AS04 Delay Min + 74AS02 Delay Min + 74AS02 Delay Min − Clock to ADR Max − 74AS04 Min

= Tcp12 + Tphl + Tphl + Tphl + Tphl − #6 − Tphl

= 80 ns + 1 ns + 1 ns + 1 ns + 1 ns − 55 ns − 1 ns

= 28 ns @ 12.5 MHz

$405: $\overline{ADS}$ Negated Held from CLK High

= Min 74AS04 + Min 74AS02 + Min 74AS02 + Min 74AS04 − Min 74AS04

= Tphl + Tphl + Tphl + Tphl − Tphl

= 1 ns + 1 ns + 1 ns + 1 ns − 1 ns

= 3 ns @ 12.5 MHz

#47: DTACK Setup Time

= 1 Clock Period − CLOCK skew (74AS04) − Max Clock to DTACK

= Tcp12 − Tphl Max − $18

= 80 ns − 5 ns − 28 ns

= 47 ns @ 12.5 MHz

$\overline{RAS}$ LOW DURING REFRESH

tRAS = Programmed Clock − [(CLK High to Refresh $\overline{RAS}$ Asserted) − (CLK High to Refresh $\overline{RAS}$ Negated)]

= Tcp12 + Tcp12 − $55

= 80 ns + 80 ns − 6 ns

= 154 ns @ 12.5 MHz

$\overline{RAS}$ PRECHARGE PARAMETERS

tRP = Programmed Clocks − Clock to $\overline{AS}$ Negated − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]

= Tcp12 + Tcp12 − $50

= 80 ns + 80 ns − 16 ns

= 144 ns @ 12.5 MHz

$29b: $\overline{AREQ}$ Negated Setup to CLK

= Clock Period + Min CLOCK Skew 74AS04 − Max 74AS02 − Max 74AS02

= Tcp12 + Tphl + Tphl − Tphl

= 80 ns + 1 ns − 4.5 ns − 4.5 ns

= 72 ns @ 12.5 MHz

tRAC AND tCAC FOR DRAMs

Timing is supplied for the system shown in *Figure 5*. (See *Figures 6*). Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system. Timing has been suppiled for systems with 0 wait states and 1 bank of DRAM and 1 wait state and 4 banks of DRAM. If DELCLK is not a multiple of 2 MHz, the times of tRAH and tASC will increase or decrease according to the equations given in the data sheet. The $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also have to be changed depending on the capacitance of the DRAM array.

tRAC

0 wait states * does not use transceivers *

tRAC = s2 + s3 + s4 + s5 + s6 − 74AS02 Max − 74AS02 Max − Clock to AS Max − $\overline{ADS}$ to $\overline{RAS}$ − Data Setup

= 2½ Tcp12 − Tphl − Tphl − #9 − $402 − #27

= 200 − 4.5 ns − 4.5 ns − 55 ns − 25 ns − 10 ns

= 101 ns @ 12.5 MHz **Using 8420-25 w/Light Load

1 wait state * uses transceivers *

tRAC = s2 + s3 + s4 + sw + sw + s5 + s6 − 74AS02 Max − 7AS02 Max − Clock to $\overline{AS}$ Max − $\overline{ADS}$ to $\overline{RAS}$ − 74AS245 Delay − Data Setup

= 3½ Tcp12 − Tphl − Tphl − #9 − $402 − Tphl − #27

= 280 ns − 4.5 ns − 4.5 ns − 55 ns − 29 ns − 7 ns − 10 ns

= 170 ns @ 12.5 MHz

tCAC

0 wait states * does not use transceivers *

tCAC = s2 + s3 + s4 + s5 + s6 − 74AS02 Max − 74AS02 Max − Clock to $\overline{AS}$ Max − $\overline{ADS}$ Asserted to $\overline{CAS}$ − Data Setup

= 2½ Tcp12 − Tphl − Tphl − #9 − $403a − #27

= 200 ns − 4.5 ns − 4.5 ns − 55 ns − 75 ns − 10 ns

= 51 ns @ 12.5 MHz *Using 8420-25 w/Light Load

1 wait state * uses transceivers *

tCAC = s2 + s3 + s4 + sw + sw + s5 + s6 − 74AS02 Max Delay − 74AS02 Max Delay − Clock to $\overline{AS}$ Max − $\overline{ADS}$ Asserted to $\overline{CAS}$ − 74AS245 Data Setup

= 3½ Tcp12 − Tphl − Tphl − #9 − $403a − Tphl − #27

= 280 ns − 4.5 ns − 4.5 ns − 55 ns − 75 ns − 7 ns − 10 ns

= 124 ns @ 12.5 MHz

DESIGN #2, 0 WAIT STATES DURING WRITE ACCESS

Design #2 can be modified to allow 0 wait states during writes. To accomplish this, the chip must be programmed with the same value except that bits R2, R3 and R6 are changed to:

R2 = 0 DTACK of 0T from RAS
R3 = 0
R6 = 0 Hold off DTACK 1 extra clock period

The hardware must be modifed. The signal R/W from the 68000 is inverted and tied to the 8420 signal $\overline{WAITIN}$. This ensures that a wait state will only be asserted during read accesses (see *Figure 6*).

0 waits during write access timing

$\overline{RAS}$ Low Time

tRP = Max $\overline{AS}$ Low − ½ Clock Period − 74AS02 Delay − 74AS02 Delay + 74AS02 Delay + 74AS02 Delay − [($\overline{ADS}$ Asserted to $\overline{RAS}$) − ($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated)]

= #14 − ½ Tcp12 − Tphl − Tphl + Tphl + Tphl − $52

= 160 ns − 40 ns − 0 ns

= 120 ns @ 12.5 MHz

$\overline{CAS}$ Low Time

tCP = s2 + s3 + s4 + s5 + s6 − Max CLK to $\overline{AS}$ − 74AS02 − 74AS02 − Max $\overline{AS}$ to $\overline{CAS}$ + Min CLK to $\overline{DS}$ + Min ECAS to CAS

= 2½ Tcp12 − #9 − Tphl − Tphl − $403a + #12 + $14

= 200 ns − 55 ns − 4.5 ns − 4.5 ns − 82 ns + 0 ns + 0 ns

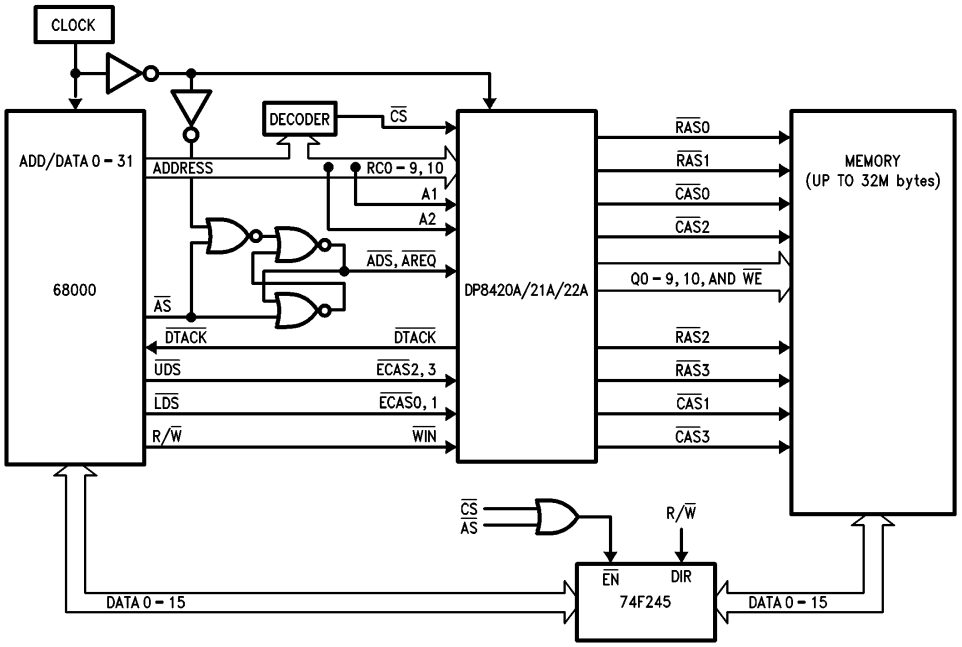
= 54 ns @ 12.5 MHz

Design #2 Programming Bits

Bits	Description	Value
R0, R1	$\overline{RAS}$ Low Time = 2T $\overline{RAS}$ Precharge Time = 2T	R0 = 0 R1 = 1
R2, R3	$\overline{DTACK}$ Generation Modes for Non-Burst Accesses	R2 = 0 R3 = 1
R4, R5	$\overline{DTACK}$ Generation Modes for Burst Accesses	R4 = 0 R5 = 1
R6	Add Wait States with $\overline{WAITIN}$	R6 = 0
R7	$\overline{DTACK}$ Mode Select	R7 = 1
R8	Non Interleaved Mode	R8 = 1
R9	Staggered or All RAS REFRESH	R9 = u
C0, C1, C2	Divisor for DELCLK	C0 = u C1 = u C2 = u
C3	+30 REFRESH	C3 = 0
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode *Choose All $\overline{CAS}$ Mode	C4 = u C5 = u C6 = u
C7	Select 15 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Setup	C8 = 1
C9	CAS is Delayed to the Next Rising CLK Edge During Writes	C9 = 1
B0	The Row/Column Bank Latches Are Fall Through Mode	B0 = 1
B1	Access Mode 1	B1 = 1
$\overline{ECAS0}$	$\overline{CAS}$ Not Extended Beyond $\overline{RAS}$	$\overline{ECAS0}$ = 0

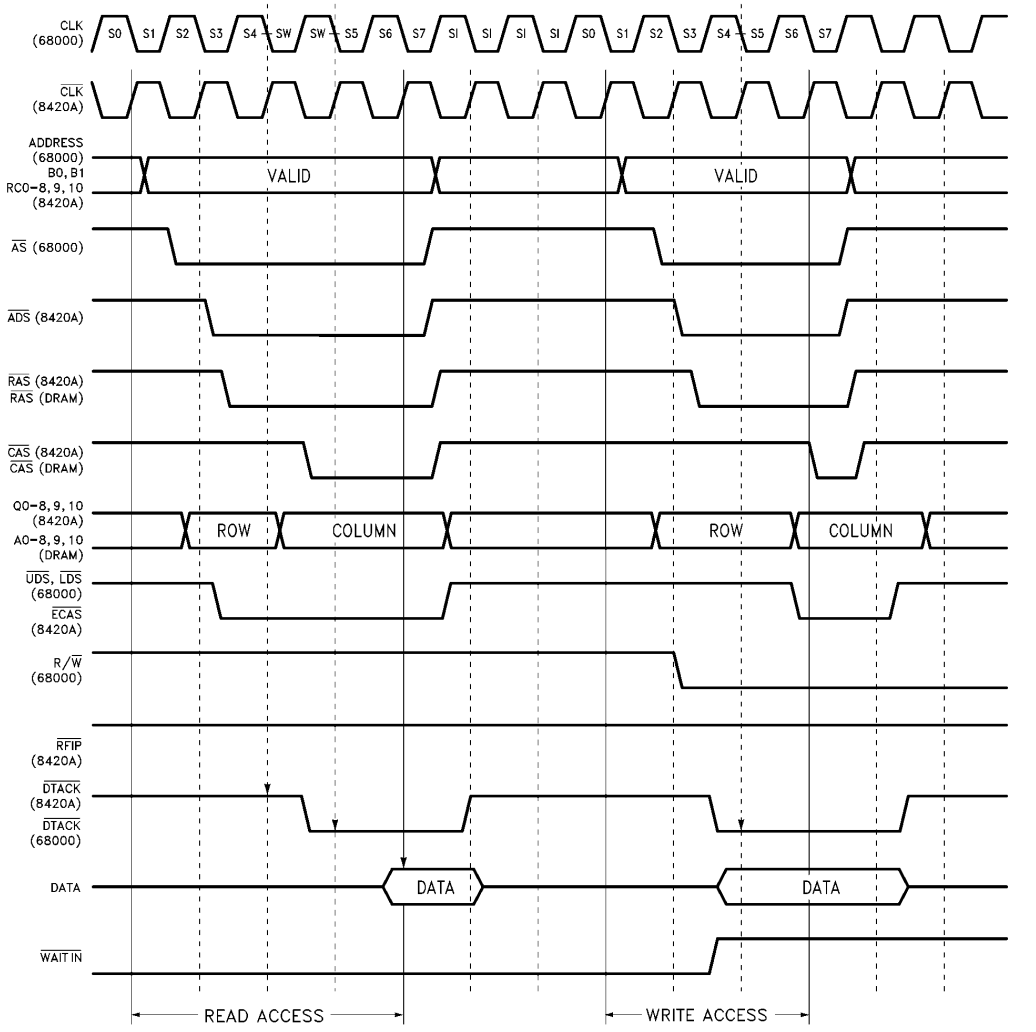
u = user defined

*see previous page for 0 WAIT STATES during writes



TL/F/9732–5

FIGURE 5. 68000 Design #2 up to 12.5 MHz



TL/F/9732–6

FIGURE 6. Design #2 Timing with Zero Wait States during Writes

DESIGN #3 DESCRIPTION

Design #3 is a simple circuit to interface the 68000 running @ 16 MHz to the DP8420A/21A/22A and up to 32 Mbytes of DRAM. The DP8420A/21A/22A is operated in Mode 1. An access cycle begins when the 68000 places a valid address on the address bus and asserts $\overline{AS}$. $\overline{AS}$ is then clocked with a 74AS74 flip-flop. The output of the flip-flop is used to produce $\overline{ADS}$ to the DP8420A/21A/22A.

Chip Select ($\overline{CS}$) is generated by a 74AS138 decoder. If a refresh or Port B access had been in progress, the 8420A/21A/22A would hold off the access by inserting wait states in the access cycle. The DP8420A/21A/22A will place the row address on the DRAM's address bus and assert $\overline{RAS}$. After guaranteeing the row address hold time, tRAH, the DP8420A/21A/22A will place the column address on the DRAM's address bus and assert $\overline{CAS}$.

DESIGN #3 TIMING AT 16.667 MHz

Clock Period = Tcp16 = 60 ns @ 16.667 MHz

$400b: $\overline{ADS}$ Asserted Setup to CLK High
= Clock Period − 74AS74 Delay Max
= Tcp16 − Tphl
= 60 ns − 9 ns
= **51 ns @ 16.667 MHz**

$401: $\overline{CS}$ Asserted Setup to $\overline{ADS}$ Asserted
= 1½ Clock Periods + Min 74AS74 Delay − Max Clock to Address − 74AS138 Delay
= 1½ Tcp16 + Tphl − #6 − Tphl
= 90 ns + 4.5 ns + 50 ns − 9 ns
= **35.5 ns @ 16.667 MHz**

$407 & $404: Address Valid Setup to $\overline{ADS}$ Asserted
= 1½ Clock Periods + Min 74AS74 Delay − Max Clock to Address
= 1½ Tcp16 + Tphl − #6
= 90 ns + 4.5 ns − 50 ns
= **44.5 ns @ 16.667 MHz**

$405: $\overline{ADS}$ Negated Held from CLK High
= Min 74AS74 Delay
= **4.5 ns @ 16.667 MHz**

#47: DTACK Setup Time
= Clock Period − 74AS74 Delay Max
= Tcp16 − Tphl
= 60 ns − 9 ns
= **51 ns @ 16.667 MHz**

$\overline{RAS}$ LOW DURING REFRESH

tRAS = Programmed Clocks − [(CLK High to Refresh $\overline{RAS}$ Asserted) − (CLK High to Refresh $\overline{RAS}$ Negated)]
= Tcp16 + Tcp16 + Tcp16 + Tcp16 − $55
= 240 ns − 6 ns
= **234 ns @ 16.667 MHz**

tRP = (Programmed Clocks − 1) − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]
= Tcp16 + Tcp16 − $50
= 120 ns − 16 ns
= **104 ns @ 16.667 MHz**

$\overline{RAS}$ PRECHARGE PARAMETERS

tRP = Programmed Clocks − Clock to $\overline{AS}$ Negated − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]

tRAC AND tCAC FOR DRAMs

Timing is supplied for the system shown in *Figure 7*. Since system and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 2 wait states. If DELCLK is not a multiple of 2 MHz, the timing for tRAH and tASC will increase or decrease according to the times given in the data sheet. The $\overline{ADS}$ to $\overline{RAS}$ and $\overline{ADS}$ to $\overline{CAS}$ will also have to be changed depending on the capacitance of the DRAM array.

1 wait state * using 1 BANK with no transceivers

tRAC = s4 + sw + sw + s5 + s6 − 74AS74 Delay − $\overline{ADS}$ to $\overline{RAS}$ − Data Setup
= 2½ Tcp16 − Tphl − $402 − #27
= 150 ns − 9 ns − 25 ns − 10 ns
= **106 ns @ 16.667 MHz** Using 8420-25 w/Light Load

2 wait states * uses 4 banks with tranceivers *

tRAC = s4 + sw + sw + sw + sw + s5 + s6 − 74AS74 Delay − $\overline{ADS}$ to $\overline{RAS}$ − Data Setup − Transceivers
= 3½ Tcp16 − Tphl − $402 − #27 − Tphl
= 210 ns − 9 ns − 29 ns − 10 ns − 7 ns
= **155 ns @ 16.667 MHz**

1 wait state * using 1 BANK with no transceivers

tCAC = s4 + sw + sw + s5 + s6
− 74AS74 Delay − $\overline{ADS}$ to $\overline{CAS}$
− Data Setup
= 2½ Tcp16 − Tphl − $403a − #27
= 150 ns − 9 ns − 75 ns − 10 ns

= 56 ns @ 16 MHz

2 wait states * using 4 banks with transceivers *

tCAC = s4 + sw + sw + sw + sw + s5 + s6
− 74AS74 Delay − $\overline{ADS}$ to $\overline{CAS}$
− Data Setup − Transceiver
= 3½ Tcp16 − Tphl − $403a
− #27 − Tphl
= 210 ns − 9 ns − 82 ns
− 10 ns − 7 ns

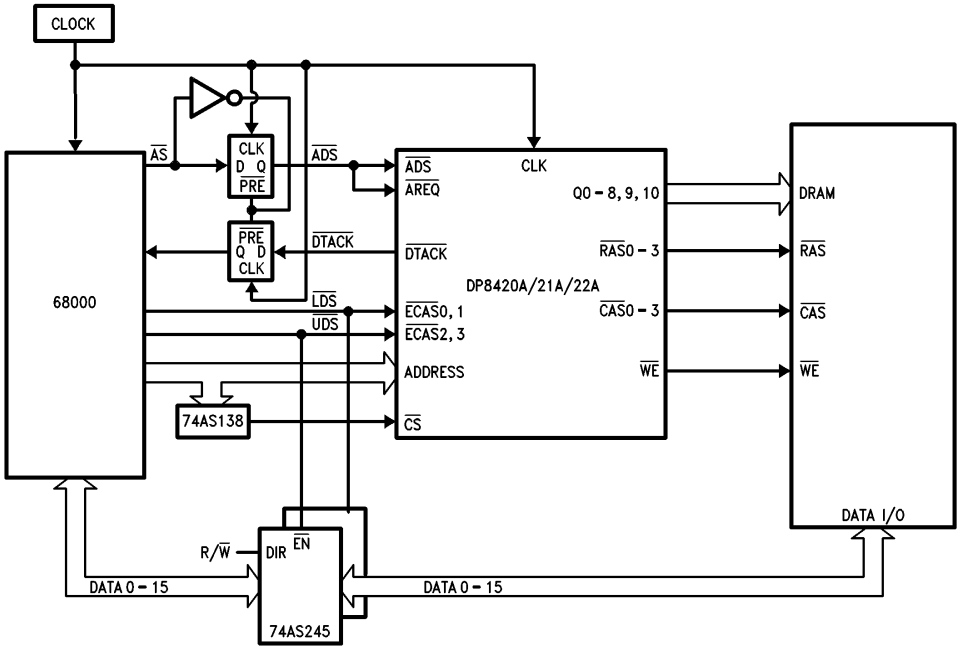
= 102 ns @ 16 MHz

Design #3 Programming Bits

Bits	Description	Value
R0, R1	$\overline{RAS}$ Low Time = 2T $\overline{RAS}$ Precharge Time = 2T	R0 = 0 R1 = 1
R2, R3	$\overline{DTACK}$ Generation Modes for Non-Burst Accesses	R2 = 1 R3 = 0
R4, R5	$\overline{DTACK}$ Generation Modes for Burst Accesses	R4 = u R5 = u
R6	Add Wait States with $\overline{WAITIN}$	R6 = u
R7	$\overline{DTACK}$ Mode Select	R7 = 1
R8	Non Interleaved Mode	R8 = 1
R9	Staggered or All RAS REFRESH	R9 = u
C0, C1, C2	Divisor for DELCLK (+8 for 16 MHz)	C0 = 0 C1 = 1 C2 = 0
C3	+30 REFRESH	C3 = 0
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode *Choose All $\overline{CAS}$ Mode	C4 = u C5 = u C6 = u
C7	Select 15 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Setup	C8 = 1
C9	CAS is Delayed to the Next Rising CLK Edge During Writes	C9 = 1
B0	The Row/Column Bank Latches Are Fall Through Mode	B0 = 1
B1	Access Mode 1	B1 = 1
$\overline{ECAS0}$	$\overline{CAS}$ Not Extended Beyond $\overline{RAS}$	$\overline{ECAS0}$ = 0

u = user defined

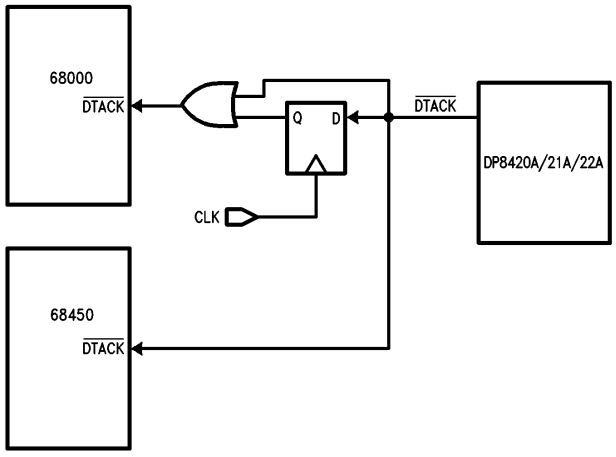
*see previous page for 0 WAIT STATES during writes



TL/F/9732–7

FIGURE 7. 68000 Design #3, Works up to 16 MHz

Additional Circuitry for Design #1
Using the 68450 DMA Controller



TL/F/9732–8

Because the 68450 samples $\overline{DTACK}$ on a positive edge of CLK and the 68000 samples $\overline{DTACK}$ on the negative edge, additional circuitry must be added to produce the two $\overline{DTACK}$ signals. The $\overline{DTACK}$s must be produced different to ensure $\overline{RAS}$ low time after an access delayed by a refresh. The programming bits must also be changed as follows:

```
For 0 WAITSTATES
R2 = 0 R3 = 1 FOR /DTACK OF 1/2

For 1 WAITSTATE
R2 = 0 R3 = 1 R6 = 0 FOR /DTACK OF 1 1/2
```

Tie the DP8420 signal $\overline{WAITIN}$ low for 1 waitstate and high for 0 waitstates. All timing except for the following should still apply. Times with a "#" refer to the 68000 data sheet. Times with a "!" refer to the 68450 data sheet and times with a "$" refer to the DP8420A/21A/22A data sheet.

$47: $\overline{DTACK}$ Setup Time

= ½ CLOCK Period − 74AS74 CLOCK to Q − 74AS32

= ½ Tcp10 − Tphl − Tphl

= 50 ns − 9 ns − 6 ns

= **35 ns @ 10 MHz**

= ½ Tcp8 − Tphl − Tphl

= 62.5 ns − 9 ns − 6 ns

= **47 ns @ 8 MHz**

!6: $\overline{DTACK}$ Setup Time (68450)

= ½ CLOCK Period − CLOCK to $\overline{DTACK}$

= ½ Tcp10 − $18

= 50 ns − 28 ns

= **22 ns @ 10 MHz**

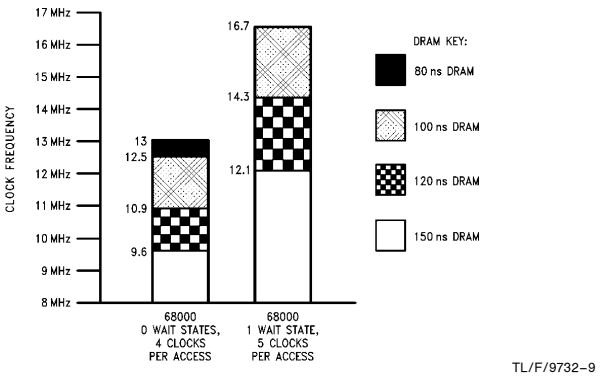
= ½ Tcp8 − $18

= 62.5 ns − 33 ns

= **29 ns @ 8 MHz**

All other 68450 times are the same as the 68000.

DRAM Speed Versus Processor Speed,
(DRAM Speed References the RAS Access Time, tRAC, of the DRAM.
Using DP8422A-25 Timing Specifications)



TL/F/9732–9

Lit. # 100538

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408