Interfacing the DP8420A/21A/22A to the NS32008/016/C016/032/132

National Semiconductor
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INTRODUCTION

This application note explains interfacing the DP8420A/21A/22A to the National Semiconductor 32C016. Two different designs are shown and explained. It is assumed the reader is familiar with the NS32C016 access cycles and the DP8420A/21A/22A modes of operation. This application note is written for the NS32C016, but is also valid for the NS32008/016/032/132.

DESIGN DESCRIPTION

This design is a simple circuit to interface the DP8420A/21A/22A to the NS32C016 and up to 32 Mbytes of DRAM. The DP8420A/21A/22A is operated in mode 0. An access cycle begins when the 32C016 asserts the $\overline{ADS}$ signal and places a valid address on the bus. The $\overline{ADS}$ signal places a group of 74AS373 fall-through latches in fall-through mode and $\overline{ADS}$ negated latches the address to guarantee the address is valid throughout the entire access. The $\overline{ADS}$ signal is inverted to produce the signal ALE to the DP8420A/21A/22A. On the next rising clock edge, after the ALE signal is asserted, the DP8420A/21A/22A will assert $\overline{RAS}$. After guaranteeing the row address hold time, tRAH, the DP8420A/21A/22A will place the column address on the DRAM address bus, guarantee the column address setup time and assert $\overline{CAS}$. The transceivers are enabled by $\overline{CS}$ and $\overline{AS}$. After tCAC, the DRAM will place the data on the bus. The DP8420A/21A/22A will also take care of refresh access arbitration and will hold off the access by asserting the $\overline{CWAIT}$ signal to the NS32C201 TCU.

Timing parameters are referenced to the numbers shown in the DP8420A/21A/22A data sheet. Times beginning with a "$" refer to the DP8420A/21A/22A data sheet. Times beginning with a "#" refer to the NS32C016 data sheet. Times beginning with a "!" refer to the NS32C201 data sheet in the 1986 Series 32000® data book. Equations given allow the user the calculation timing based on his frequency and application. The clock to the DELCLK has been chosen to be a multiple of 2MHz. If you do not have a clock, which is a multiple of 2 MHz, the $\overline{ADS}$ to $\overline{CAS}$ time must be recalculated.

DESIGN TIMING PARAMETERS

Clock Period = Tcp10 = 100 ns @ 10 MHz
= Tcp15 = 66 ns @ 15 MHz

$300: $\overline{CS}$ asserted to CLK High
= T1 − (PHI1 to address + AS373 in to Out + AS138 Decoder + CTTL to PHI1 Max + Inverter)
= Tcp − #tALV − tphl − tphl − !tPCr
= 100 ns − 50 ns − 6 ns − 9 ns − 2 ns
= 33 ns @ 10 MHz
= 66 ns − 35 ns − 6 ns − 9 ns − 2 ns
= 14 ns @ 15 MHz

$301b: ALE Setup to CLK High
= T1 − Inverter Max − PHI1 to $\overline{ADS}$ − CTTL to PHI1
= Tcp − tplh − #tADSa − !tPCr
= 100 ns − 5 ns − 35 ns − 2 ns
= 55 ns @ 10 MHz
= 66 ns − 5 ns − 26 ns − 2 ns
= 33 ns @ 15 MHz

$302: ALE Pulse Width
= T1 − Inverter Max − PHI1 to $\overline{ADS}$ − CTTL to PHI1
= #tADSw
= 30 ns @ 10 MHz
= 25 ns @ 15 MHz

$303 & $304: Address Setup to CLK
= T1 − PHI1 to Address + AS373 in to out + CTTL to PHI1 Max)
= Tcp − #tADSa − tphl − !tPCr
= 100 ns − 50 ns − 6 ns − 2 ns
= 42 ns @ 10 MHz
= 66 ns − 35 ns − 6 ns − 2 ns
= 23 ns @ 15 MHz

$309: ALE Negated Held from CLK High
= Min CLK to $\overline{ADS}$ + Min Inverter − CTTL to PHI1 Max
= Min CLK to $\overline{ADS}$ + 1 ns − 2 ns
= Min CLK to $\overline{ADS}$ − 1 ns @ 10 MHz
= Min CLK to $\overline{ADS}$ − 1 ns @ 15 MHz

* no time is specified for CLK to $\overline{ADS}$ min.*

$310: $\overline{WIN}$ Setup to CLK High to Guarantee $\overline{CAS}$ is Delayed
= T1 + T2 − PHI1 to CTTL R.E. − DDIN Signal Valid − 74AS04
= 2Tcp − !tPCr − #tDDINv − tphl
= 200 ns − 2 ns − 45 ns − 5 ns
= 148 @ 10 MHz
= 66 ns + 66 ns − 2 ns − 38 ns − 5 ns
= 87 ns @ 15 MHz

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$315: $\overline{AREA}$ Negated to CLK High that Starts Access $\overline{RAS}$

= T4 + T1 − PHI1 to CTTL R.E. − PHI1 to TSO High

= 2Tcp − !tPCr − !tTr

= 200 ns − 2 ns − 18 ns

= 180 ns @ 10 MHz

= 66 ns + 66 ns − 2 ns − 10 ns

= 120 ns @ 15 MHz

$\overline{CWAIT}$ TIMING

!tCWs(W): $\overline{CWAIT}$ Setup for WAIT STATES

= Min PHI1 Pulse Width + Min Clock Overlap − PHI1 to TSO − 74AS32

= !Tclw(1) + !tnOVL − !tTf − tphl

= 40 ns + 0 ns − 12 ns − 5 ns

= 23 ns @ 10 MHz

= 27 ns + 0 ns − 6 ns − 5 ns

= 16 ns @ 15 MHz

*parameters $311 & 312 & 314 ensure $\overline{WAIT}$ will already be asserted

!tCWs(W): $\overline{CWAIT}$ Setup for Termination of Access

= Clock Period − Max to PHI to CTTL − CLK to Wait High − 74AS32

= !TCP − !tTCr − $17 − tphl

= 100 ns − 6 ns − 31 ns − 5 ns

= 58 ns @ 10 MHz

= 66 ns − 2 ns − 31 ns − 5 ns

= 28 ns

tRAC AND tCAC TIMING FOR DRAMs

Timing diagrams are supplied on page 8. Since systems and DRAM times vary, the user is encouraged to change the following equations to match his system requirements. Timing has been supplied for systems with 0 or 1 wait states. If DELCLK is not a multiple of 2 MHz the CLK to $\overline{CAS}$ delay must be recalculated.

0 Wait States

tRAC = T2 + T3 − Max Clock Skew − CLK to $\overline{RAS}$ − Transceiver Delay − Data Setup

= 2TCP − !tPCr − $307 − tphl − #tDIs

= 200 ns − 6 ns − 26 ns − 7 ns − 15 ns

= 146 ns @ 10 MHz

= 2Tcp − !tPCr − $307 − tphl − #tDIs

= 132 ns − 2 ns − 26 ns − 7 ns − 10 ns

= 87 ns @ 15 MHz

1 Wait State

tRAC = T2 + TW + T3 − Max Clock Skew − CLK to RAS − Transceiver Delay − Data Setup

= 3Tcp − !tPCr − $307 − tphl − #tDIs

= 300 ns − 6 ns − 26 ns − 7 ns − 15 ns

= 246 ns @ 10 MHz

= 198 ns − 2 ns − 26 ns − 7 ns − 10 ns

= 153 ns @ 15 MHz

0 Wait States

tCAC = T2 + T3 − Max Clock Skew − CLK to RAS − Transceiver Delay − Data Setup

= 2Tcp − !tPCr − $308a − tphl − #tDIs

= 200 ns − 6 ns − 79 ns − 7 ns − 15 ns

= 93 ns @ 10 MHz

= 132 ns − 2 ns − 79 ns − 7 ns − 10 ns

= 34 ns @ 15 MHz

1 Wait States

tCAC = T2 + T3 − Max Clock Skew − CLK to $\overline{CAS}$ − Transceiver Delay − Data Setup

= 3Tcp − !tPCr − $308a − tphl − #tDIs

= 300 ns − 6 ns − 79 ns − 7 ns − 15 ns

= 193 ns @ 10 MHz

= 198 ns − 2 ns − 79 ns − 7 ns − 10 ns

= 100 ns @ 15 MHz

$\overline{RAS}$ Precharge Parameters

$29b: $\overline{AREQ}$ Negated Setup to CLK

= Clock Period − Clock Skew PHI1 to CTTL − PHI1 to TSO

= TCP − !tPCr − !tTr

= 100 ns − 2 ns − 18 ns

= 80 ns @ 10 MHz

= 66 ns − 2 ns − 10 ns

= 54 ns @ 15 MHz

tRP = Programmed Clocks − Clock Skew PHI1 to CTTL − PHI1 to TSO − [($\overline{AREQ}$ to $\overline{RAS}$ Negated) − (CLK to $\overline{RAS}$ Asserted)]

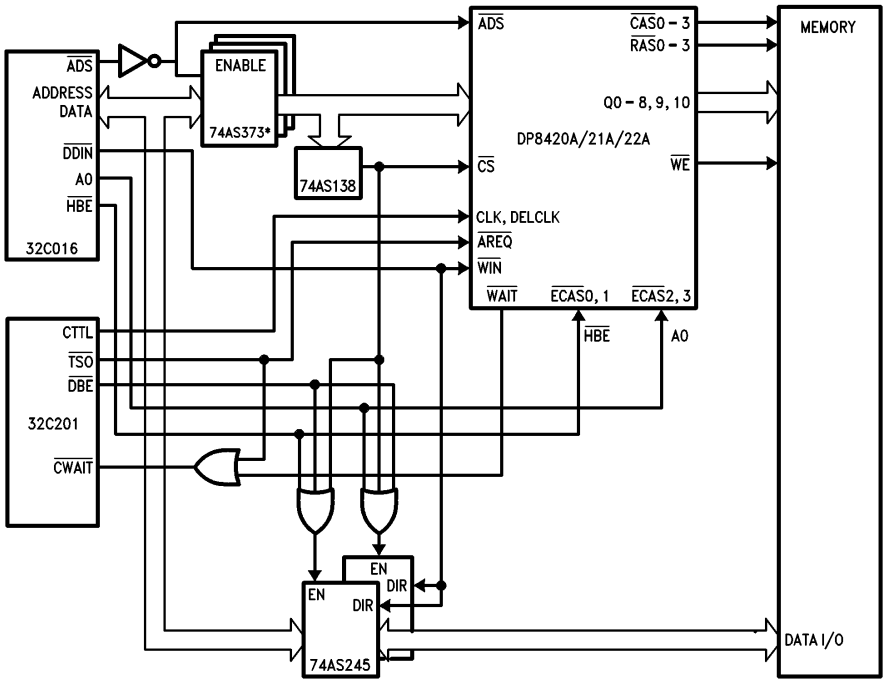
= 2TCP − !tPCr − !tTr − $50

= 200 ns − 2 ns − 18 ns − 16 ns

= 164 ns @ 10 MHz

RAS Low During Refresh

tRAS = Programmed Clocks − [(CLK High to Refresh $\overline{RAS}$ Asserted) − (CLK High to Refresh $\overline{RAS}$ Negated)]
= 2TCP − $55
= 200 ns − 6 ns
= **194 ns @ 10 MHz**
= 132 ns − 6 ns
= **126 ns @ 15 MHz**



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*Latches are not needed if DP8420A/21A/22A internal latches are used.

32C016 up to 15 MHz

Design Programming Bits

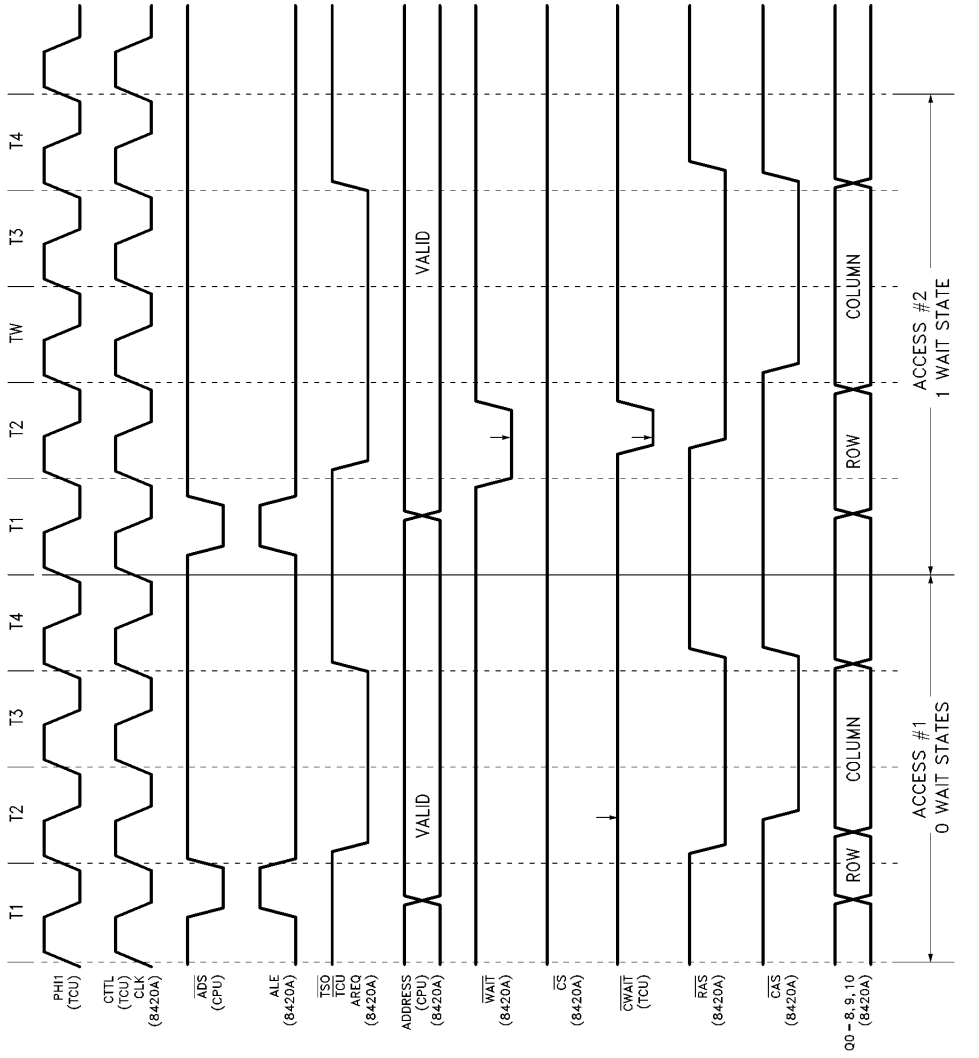
Bits	Description	Value
R0, R1	$\overline{RAS}$ Low During Refresh = 2T $\overline{RAS}$ Precharge Time = 2T	R0 = 0 R1 = 1
R2, R3	$\overline{WAIT}$ Generation Mode during Non-Burst Access	R2 = u R3 = u
R4, R5	$\overline{WAIT}$ During Burst	R4 = 0 R5 = 0
R6	ADD Wait States with $\overline{WAITIN}$	R6 = x
R7	$\overline{WAIT}$ Mode Selected	R7 = 0
R8	Non-Interleaved Mode	R8 = 1
R9	Staggered or all $\overline{RAS}$ Refresh	R9 = u
C0, C1, C2	Divisior for DELCLK *Use a Multiple of 2 MHz External Clock	C0 = * C1 = * C2 = *
C3	+30 REFRESH	C3 = *
C4, C5, C6	$\overline{RAS}$, $\overline{CAS}$ Configuration Mode **Choose an all $\overline{CAS}$ Mode, Tie a $\overline{CAS}$ to Each Nibble	C4 = ** C5 = ** C6 = **
C7	Select 0 ns Column Address Setup	C7 = 1
C8	Select 15 ns Row Address Hold	C8 = 1
C9	$\overline{CAS}$ is Delayed During Writes	C9 = 1
B0	Latches are Fall-Through	B0 = 1
B1	Access Mode 0	B1 = 0
$\overline{ECAS}$0	Non-Extend $\overline{CAS}$ Mode	$\overline{ECAS}$0 = 0

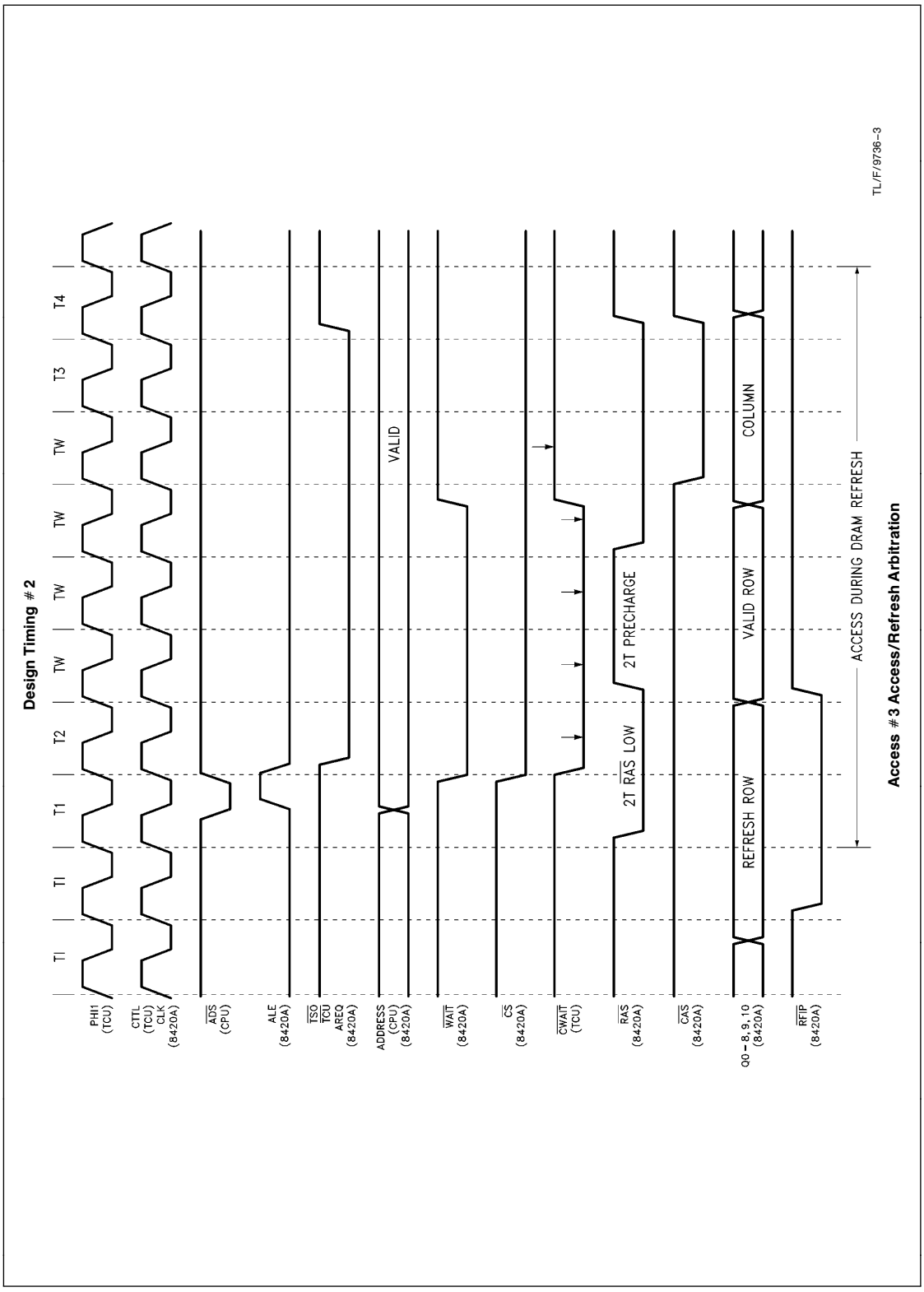
x = don't care

u = user defined

R2 = 0	R3 = 1	for 0 WAIT STATES
R2 = 1	R3 = 0	for 1 WAIT STATE
R9 = 0		all $\overline{RAS}$ refresh
R9 = 1		staggered refresh

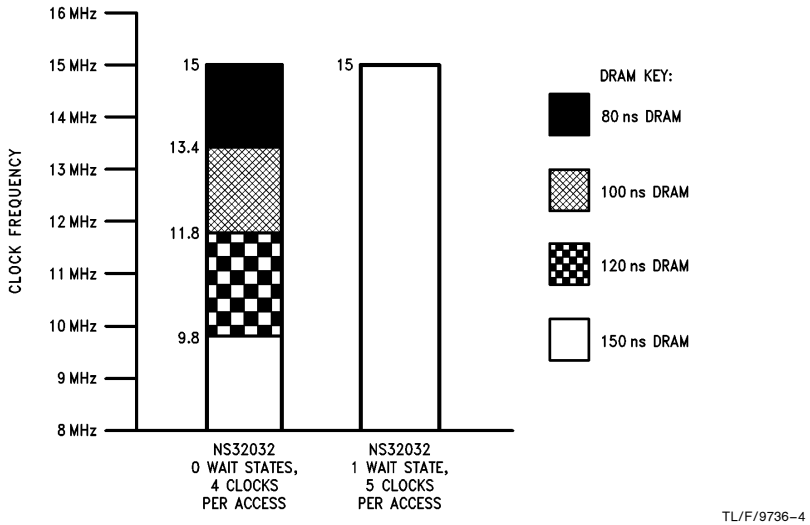
Design Timing # 1





Access #3 Access/Refresh Arbitration

DRAM Speed Versus Processor Speed (DRAM Speed References the RAS Access Time, t_{RAC}, of the DRAM Using DP8422A-25 Timing Specifications)



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