Interfacing the DP8420A/21A/22A to the National Semiconductor NS32332

National Semiconductor
Application Note 543
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I INTRODUCTION

This application note describes how to interface the National Semiconductor NS32332 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). There are four designs shown in this application note. The differences between these designs are as follows:

1. Design #1 can be used up to 14 MHz, has no wait states in normal accesses and no wait states in burst accesses, does not contain an MMU unit, is programmed with $\overline{\text{DTACK}}$0 out of the DP8422A, and has the $\overline{\text{1W}}$ input of the PAL tied high,
2. Design #2 can be used up to 15 MHz, has one wait state in normal accesses and no wait states in burst accesses, does not contain an MMU unit, is programmed with $\overline{\text{DTACK}}$1 out of the DP8422A, and has the $\overline{\text{1W}}$ input of the PAL tied high,
3. Design #3 can be used up to 14 MHz, has one wait state in normal accesses and no wait states in burst accesses, does contain an MMU unit, is programmed with $\overline{\text{DTACK}}$0 out of the DP8422A, and has the $\overline{\text{1W}}$ input of the PAL tied high,
4. Design #4 can be used up to 15 MHz, has two wait states in normal accesses and no wait states in burst accesses, does contain an MMU unit, is programmed with $\overline{\text{DTACK}}$1 out of the DP8422A, and has the $\overline{\text{1W}}$ input of the PAL tied high,

An extra wait state can also be added to any of the four above designs by tying the $\overline{\text{1W}}$ input low. It is assumed that the reader is already familiar with NS32332 and the DP8422A modes of operation.

II DESCRIPTION OF FOUR DESIGNS, ALLOWING UP TO 15 MHz OPERATION WITH 0, 1, OR 2 WAIT STATES IN NORMAL ACCESSES, NO WAIT STATES IN BURST ACCESSES AND AN OPTIONAL MMU (MEMORY MANAGEMENT UNIT, NS32382)

These four designs are all similar. Taken together they allow the user to design a 32332 DRAM system with 0, 1, or 2 wait states during an access. This system can be designed with or without the NS32382 MMU. These designs are shown driving two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4 Mbit x 1 DRAMs). By choosing a different $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ configuration mode (see programming mode bits section of DP8422A data sheet), this application could support 4 banks of DRAM, giving a memory capacity of 64 Mbytes (using 4 Mbit x 1 DRAMs).

Note: When driving 64 Mbytes, the timing calculations will have to be adjusted to the greater capacitive load.

The memory banks are interleaved on every four word (32-bit word) boundary. This means that the address bit (A4) is tied to the bank select input of the DP8422A (B1). If the majority of accesses made by the NS32332 are sequential, the NS32332 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks, allowing one memory bank to be precharging ($\overline{\text{RAS}}$ precharge) while the other bank is being accessed. This is a higher performance memory system than a non-interleaved memory system (bank select on the higher address bits). Each back to back memory access to the same memory bank will generally require extra wait states to be inserted into the CPU access cycles to guarantee the $\overline{\text{RAS}}$ precharge time.

The logic shown in this application note forms a complete NS32332 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, Port B, and refreshing the DRAM;
B. the isertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{\text{RAS}}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc.);
C. performing byte writes and reads to the 32-bit words in memory.

By making use of the enable input on the 74AS373 latch, this application can easily be used in a dual access application. The addresses and chip select are TRI-STATE® through this latch, the write input ($\overline{\text{WIN}}$), lock input ($\overline{\text{LOCK}}$), and $\overline{\text{ECAS}}$0–3 inputs must also be able to be TRI-STATE (a 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B), the DP8422A can be used in a dual access applications. All the timing (see TIMING section of this application note) will remain the same whether single or dual accessing is implemented.

If an MMU (NS32382) is used the signal "$\overline{\text{PAV}}$" should be input to the PAL "$\overline{\text{ADS}}$" input instead of the NS32332 $\overline{\text{ADS}}$ input. If wanted the user could input the $\overline{\text{MADS}}$ signal to the PAL (using the "NC1" input), allowing the access cycle to be started one clock earlier. When the PAL senses the $\overline{\text{MADS}}$ input transitioning low it can insert one less wait state into that particular access.

The PAL output term $\overline{\text{D1}}$ and the input term $\overline{\text{1W}}$ can be deleted from the PAL if the user is not interested in adding an extra wait state to any of the four designs.

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III NS32332 DESIGN, UP TO 15 MHz WITH 0, 1, OR 2 WAIT STATES IN NORMAL ACCESSES AND NO WAIT STATES IN BURST ACCESSES, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 0	$\overline{RAS}$ Low Two Clocks, $\overline{RAS}$
R1 = 1	Precharge of Two Clocks
R2 = X	Choose depending on whether design
R3 = X	1–4 is chosen. Choose R2,3 = 0,0 if $\overline{DTACK}$0 is wanted. Choose R2,3 = 1,0 if $\overline{DTACK}$1 is wanted ($\overline{DTACK}$ low first rising CLK edge after access $\overline{RAS}$ is low).
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. Since we are not using the $\overline{WAITIN}$ input it should be tied high on the DP8422A.
R7 = 1	Select $\overline{DTACK}$
R8 = 1	Non-interleaved mode
R9 = X	
C0 = X	Select based upon the input
C1 = X	''DELCLK'' frequency. Example: if the
C2 = X	input clock frequency is 14 MHz then
C3 = X	choose C0,1,2, = 1,1,0 (divide by seven, this will give a frequency of 2 MHz).
C4 = 0	$\overline{RAS}$ groups selected by ''B1''. This
C5 = 0	mode allows two $\overline{RAS}$ outputs to go
C6 = 1	low during an access, and allows byte writing 32-bit words.
C7 = 1	Column address setup time of 0 ns
C8 = 1	Row address hold time of 15 ns
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1	Fall-thru latches
B1 = 0	Access mode 0
$\overline{ECAS}$0 = 0	$\overline{CAS}$ not extended beyond $\overline{RAS}$

0 = program with low voltage level

1 = program with high voltage level

X = program with either high or low voltage level (don't care condition)

IV NS32332, DESIGN #2 (NO MMU UNIT) AT 15 MHz WITH ONE WAIT STATE IN NORMAL ACCESSES, DESIGN #4 (HAS MMU UNIT) AT 15 MHz WITH TWO WAIT STATES IN NORMAL ACCESSES. DESIGNS #2 AND #4 HAVE A TOTAL OF THREE CLOCK PERIODS TO ACCESS THE DRAM IN NORMAL ACCESSES AND HAVE ZERO WAIT STATES DURING BURST ACCESSES.

1. Maximum time to latch enable valid:

   $\overline{ADS}$ makes the 74AS373 fall-thru at 17 ns (max) from PHI1 CLOCK low + 5 ns (74AS04) + 2 ns (PHI1 to CTTL clock skew) = 24 ns

*Note: $\overline{MADS}$ and $\overline{PAV}$ are valid 17 ns maximum from PHI1 rising clock edge if NS32382 is used

2. Maximum time to address valid from CTTL CLOCK (NS32332 spec) = 20 ns (address valid from PHI1 clock) + 2 ns (PHI1 to CTTL clock skew) = 22 ns
3. Maximum time to latched address valid from CTTL CLOCK:

   11.5 ns (74AS373 enable time maximum) + 24 ns (#1) = 35.5 ns
4. Minimum ALE high setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 15 ns):

   66.6 ns (one clock period) − 17 ns (NS32332 max time to $\overline{ADS}$ low from PHI1) − 2 ns (PHI1 to CTTL clock skew) − 15 ns (PAL16R6B combinational output) − 5 ns (74AS04) = 27.6 ns
5. Minimum address setup time to CLOCK high (DP8422A–25 needs 18 ns):

   66.6 ns (one clock period) − 35.5 ns (#3) = 31.1 ns
6. Minimum $\overline{CS}$ setup time to CLOCK high (DP8422A-25 needs 13 ns):

   66.6 ns (one clock period) − 35.5 ns (#3) − 9 ns (Max 74AS138 decoder) = 22.1 ns
7. Determining t_{RAC} ($\overline{RAS}$ access time required by the DRAM):

   199.8 ns (three clock periods to do access) − 2 ns (NS32C201 PHI1 to CTTL clock skew) − 7 ns (data set-up time) − 7 ns (74F245) − 26 ns (CLK to $\overline{RAS}$ low on DP8422A-25) = 157.8 ns. Therefore the t_{RAC} of the DRAM must be 157.8 ns or less.
8. Determining t_{CAC} ($\overline{CAS}$ access time) and column address access time required by the DRAM:

   199.8 ns − 2 ns − 7 ns − 7 ns − 12 ns (74AS32, 6 ns, plus 6 ns extra, taken from lab data on the 74AS32, requried to drive a 22Ω damping resistor and an equivalent load capacitance of 150 pF, approximately 16 DRAM $\overline{CAS}$ inputs per $\overline{CASG}$n output) − 72 ns (CLK to $\overline{CAS}$ low on DP8422A-25) = 99.8 ns. Therefore the t_{CAC} of the DRAM must be 99.8 ns or less.
9. Determining the nibble mode access time required by the DRAM:

   66.6 ns (T3 clock) − 2 ns (clock skew) − 12 ns (PAL16R6B, $\overline{CASEN}$ clocked output) − 12 ns (74AS32, see #8 description) − 7 ns (74F245) − 7 ns (data setup) = 26.6 ns

   Therefore the nibble mode access time needed by the DRAM must be 26.6 ns or less.
10. Maximum time to $\overline{DTACK}$0 low (PAL16R6B needs 15 ns setup to CTTL):

    66.6 ns (one clock) − 33 ns ($\overline{DTACK}$0 low from CLK high on DP8422A-25) = 33.6 ns

    **Note that $\overline{DTACK}$1 may be used from some of the designs, it occurs at 28 ns maximum from the CLK input.
11. Minimum RDY setup time to RDY being sampled (12 ns to the PHI1 falling edge is needed by the NS32332):

    27.3 ns (minimum PHI1 high pulse width) − 2 ns (NS32C201 PHI1 to CTTL clock skew) − 12 ns (PAL16R6B clocked output maximum) = 13.3 ns

*Note: Calculations can be performed for different frequencies and the other designs (#1 and #3) by substituting the appropriate values into the above equations. Design numbers 1 and 3 have only two clock periods to perform an access, therefore the t_{RAC} and t_{CAC} calculations would be affected by having one less clock period during an access.

V NS32332 DESIGN, PAL EQUATIONS WRITTEN IN NATIONAL SEMICONDUCTOR PLAN FORMAT

```
PAL16R6B
CTTL /CS /ADS /BOUT /DTACK EXRDY /1W RESET
NC1 GND
/OE /EN_TRAN NC2 /AREQ /CASEN /D2 /D1 RDY
/ADSL VCC
IF (VCC) /ADSL = /ADS
                 +/ADSL*AREQ*/RESET
                 +/ADSL*/BOUT*/CS
                 +/ADSL*/CASEN*/CS

IF (VCC) /EN=_TRAN = /AREQ*/CS*/CASEN
                     +/EN_TRAN*/BOUT

RDY := /CS*/ADSL*D1*/1W
       +/CS*/ADSL*DTACK*D2*1W

/D1 := /DTACK*D1*/1W*/CS*/RESET
       +*/EXRDY*CS*/1W

/D2 := /CS*/D1*/1W*/RESET
       +/CS*/DTACK*D2*1W*/RESET
       +CS*/EXRDY*1W*/RESET

/CASEN := /ADSL*D2*/RESET
          +AREQ*/RESET

/AREQ := /ADSL*/RESET
```

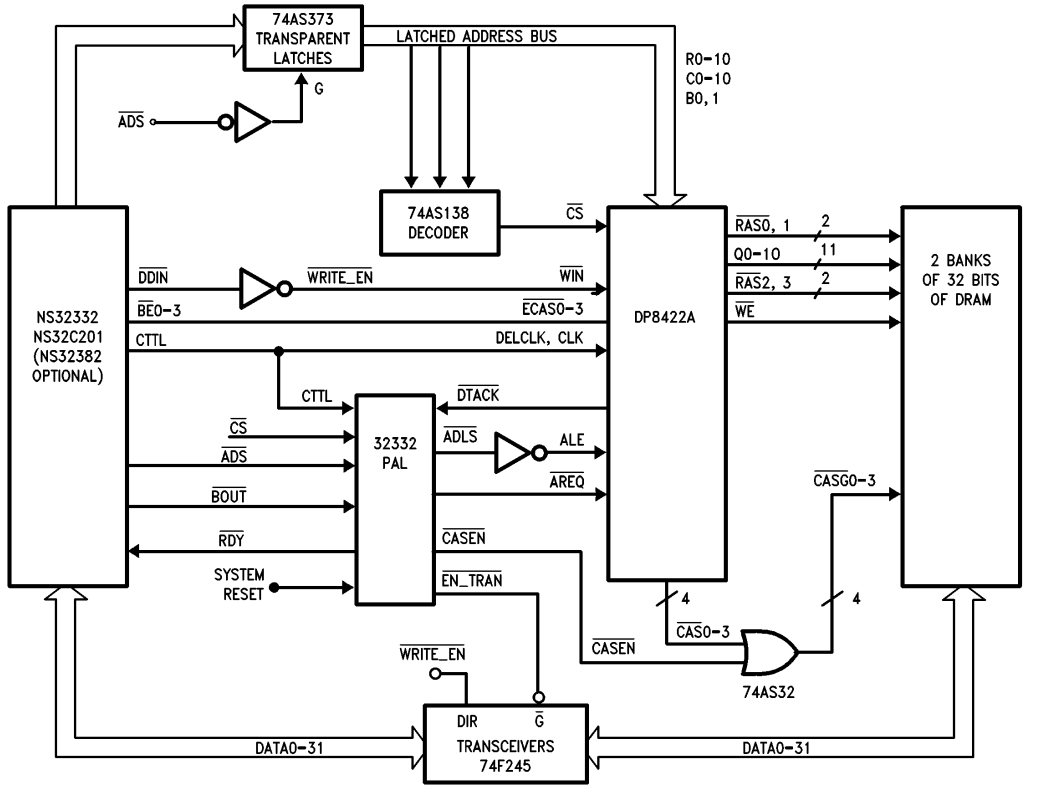
Key: Reading PAL® Equations Written in PLAN™

```
EXAMPLE EQUATIONS: /CASEN := /ADSL*D2*/RESET
                             +AREQ*/RESET
```

This example reads: the output ''/CASEN'' will transition low on the next rising ''CTTL'' clock edge (given that one of the following conditions are valid a setup time before ''CTTL'' transitions high);

1. the output ''/ADSL'' is low AND the output ''/D2'' is high AND the input ''RESET'' is low, OR
2. the output ''/AREQ'' is high AND the input ''RESET'' is low

NS32332 Design, up to 15 MHz, May Include MMU; 0, 1, or 2 Wait States per Normal Access, No Wait States in Burst Accesses (74AS373 latches are not needed if address and bank inputs meet setup and hold times of ALE and DP8422A is programmed to latch the addresses)



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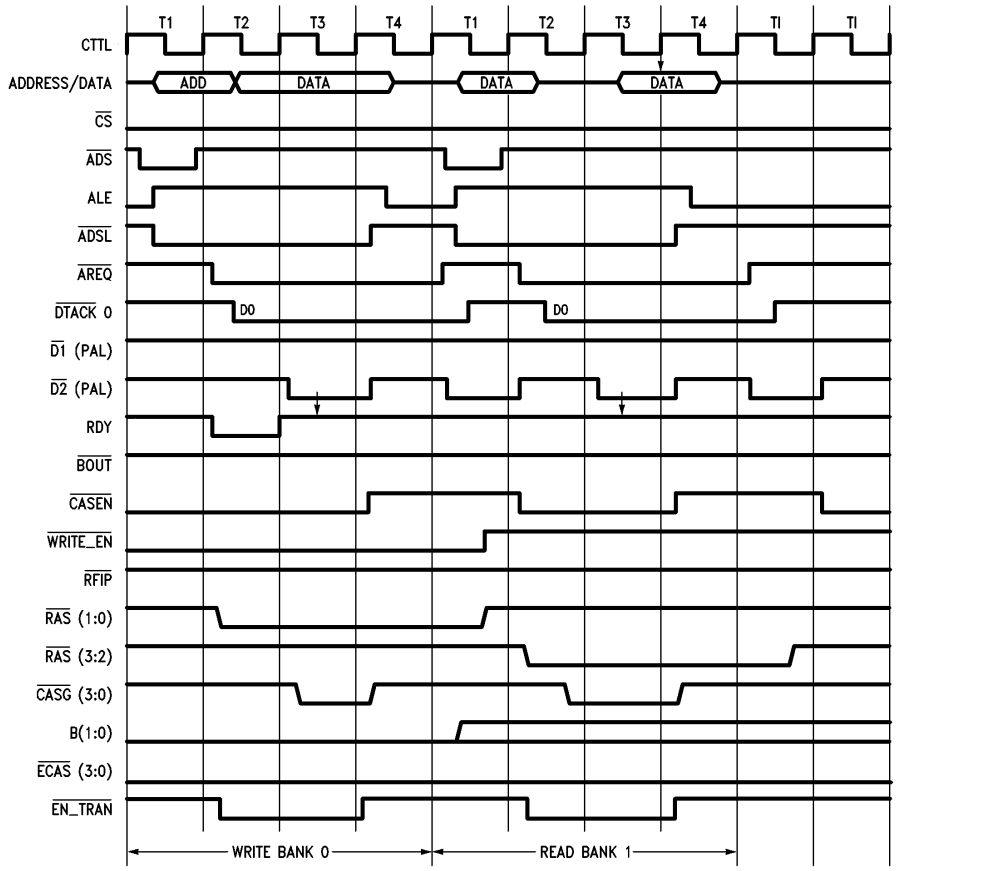

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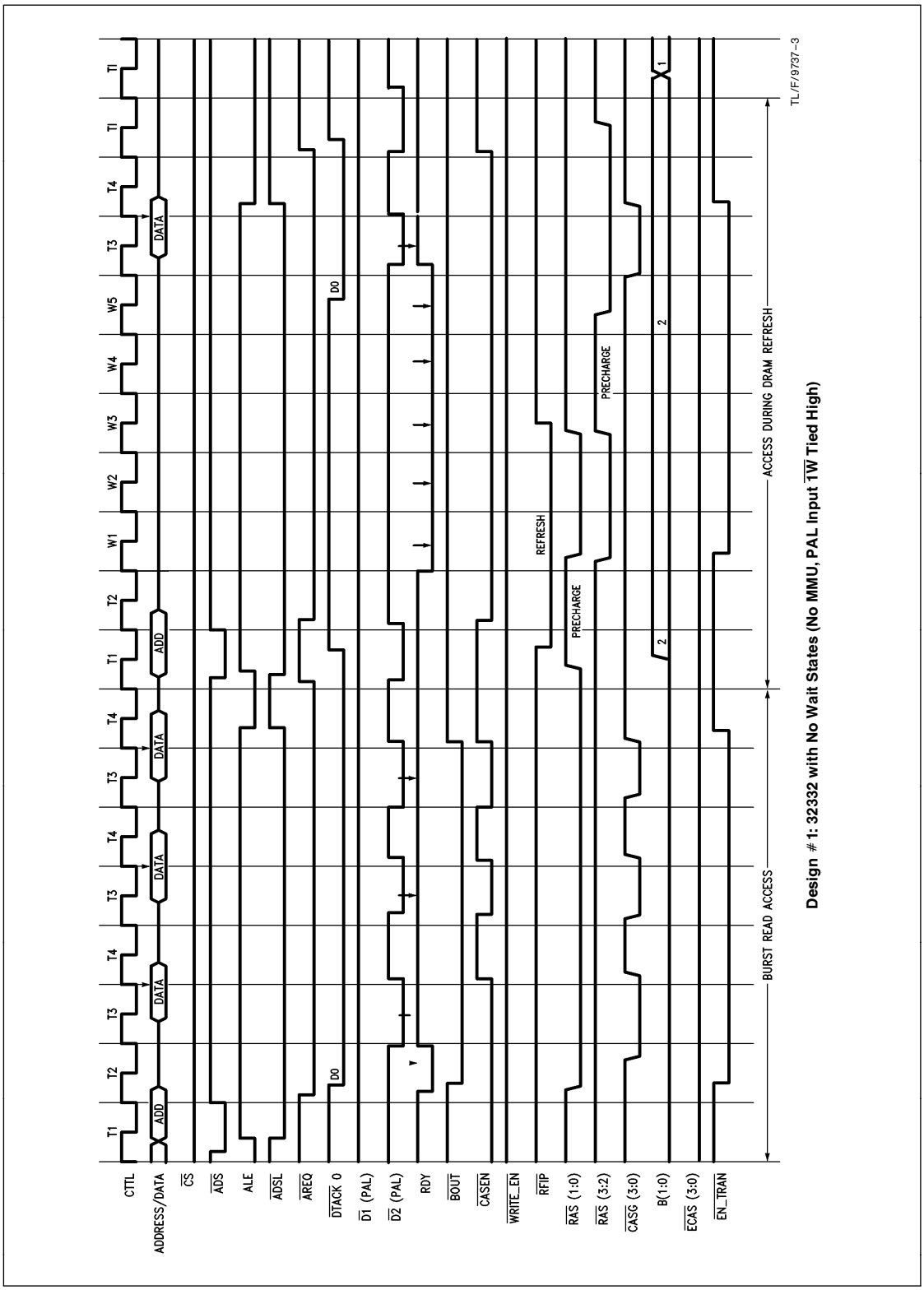
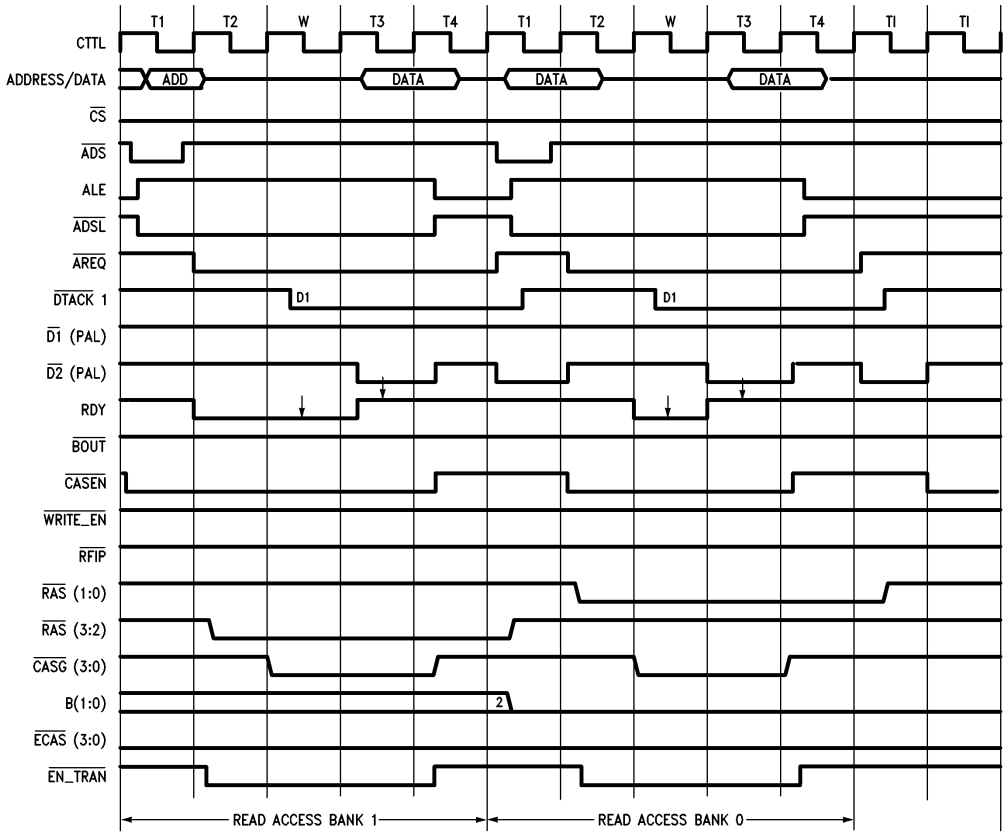
Design # 1: 32332 with No Wait States (No MMU, PAL Input $\overline{1W}$ Tied High)



Design #1: 32332 with No Wait States (No MMU, PAL Input $\overline{1W}$ Tied High)

Design #2: 32332 with One Wait State per Access (Non-Burst, $\overline{\text{DTACK}}$1 Programmed)
No MMU, PAL Input $\overline{\text{1W}}$ Tied High



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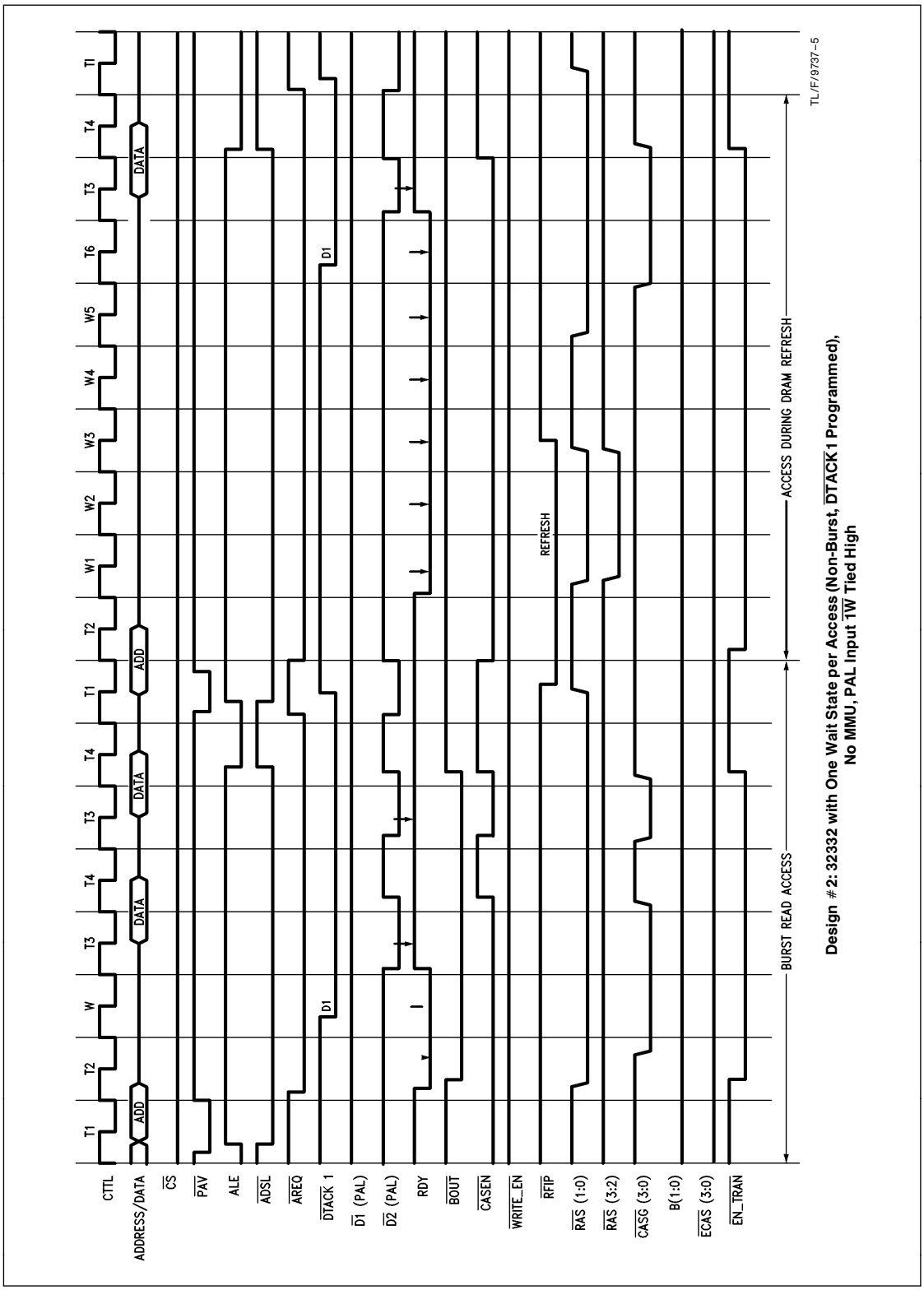
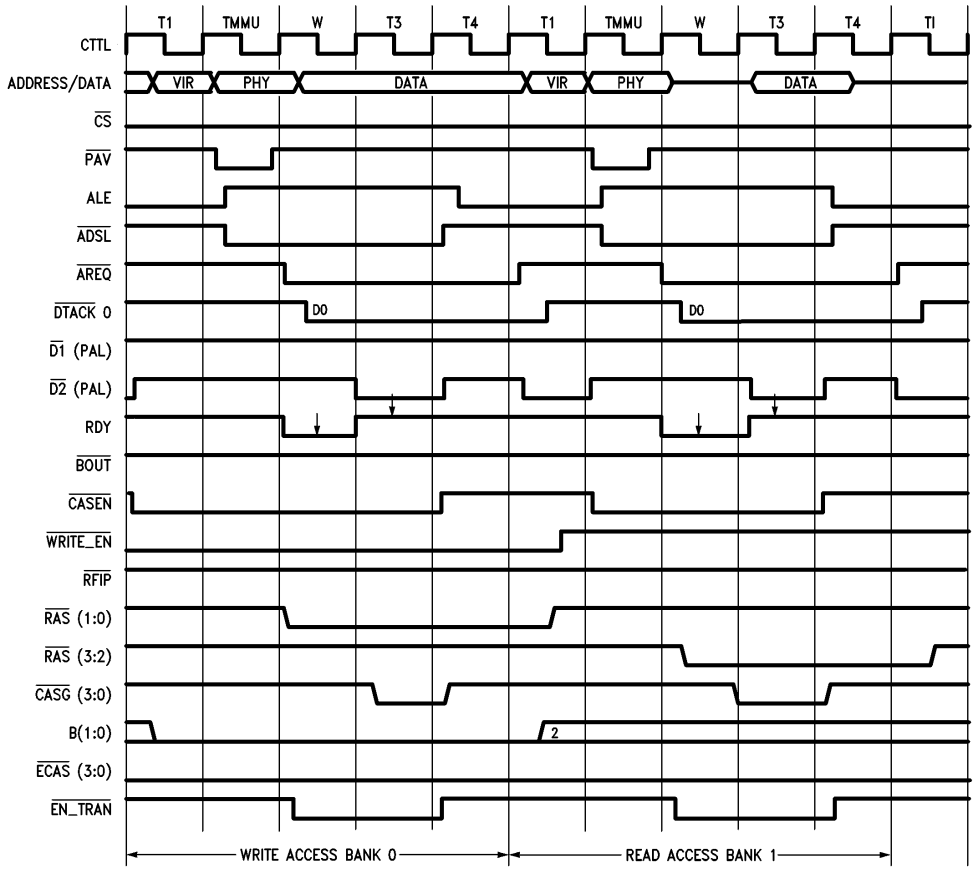


Design #2: 32332 with One Wait State per Access (Non-Burst, $\overline{\text{DTACK}}$1 Programmed), No MMU, PAL Input 1W Tied High



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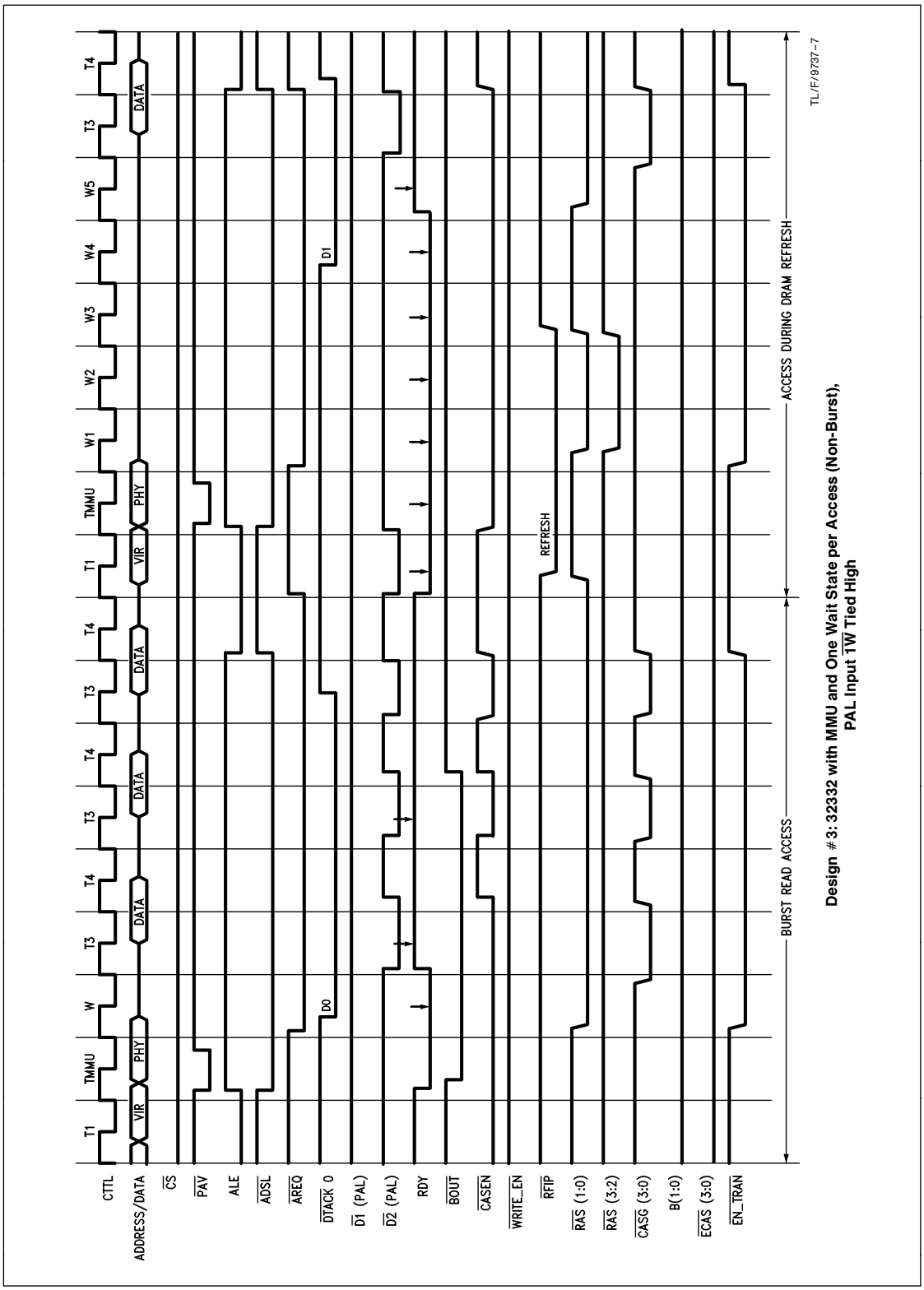
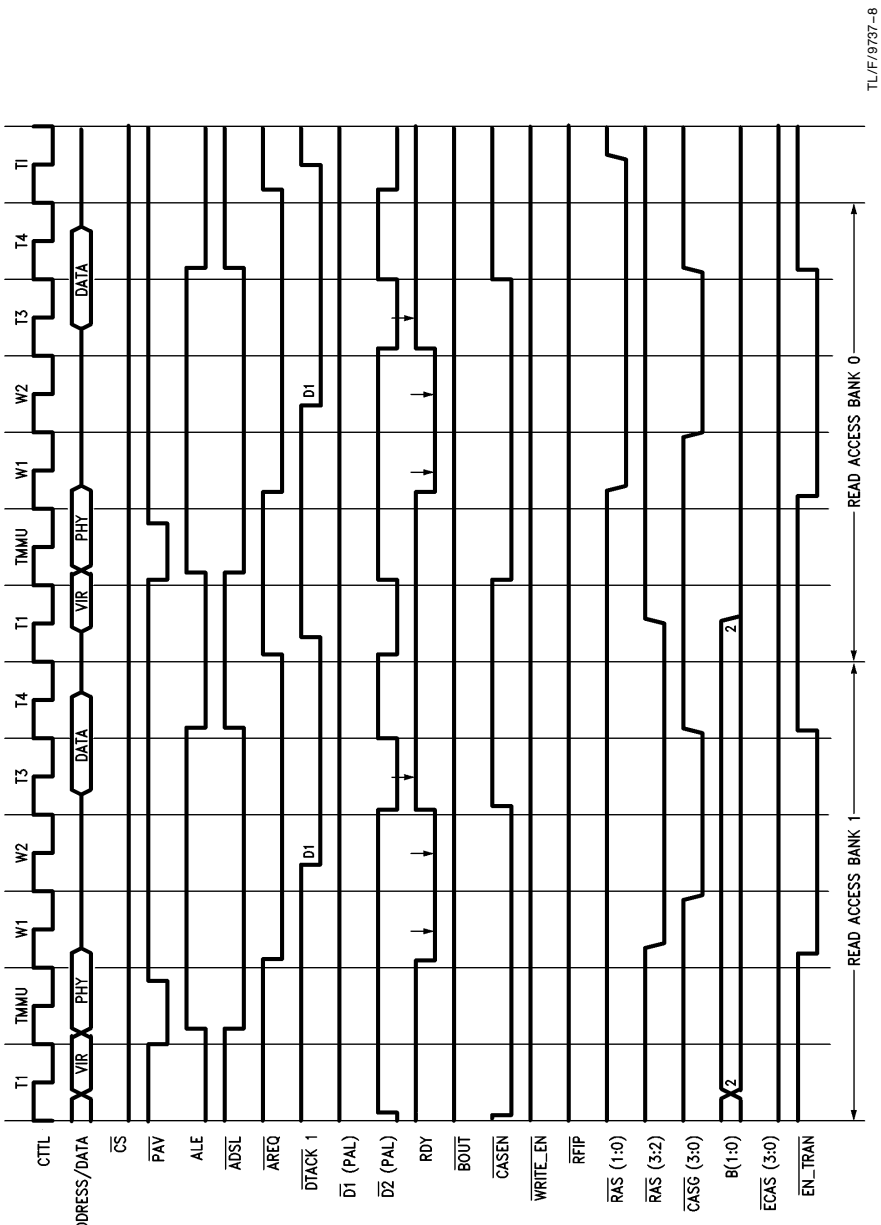
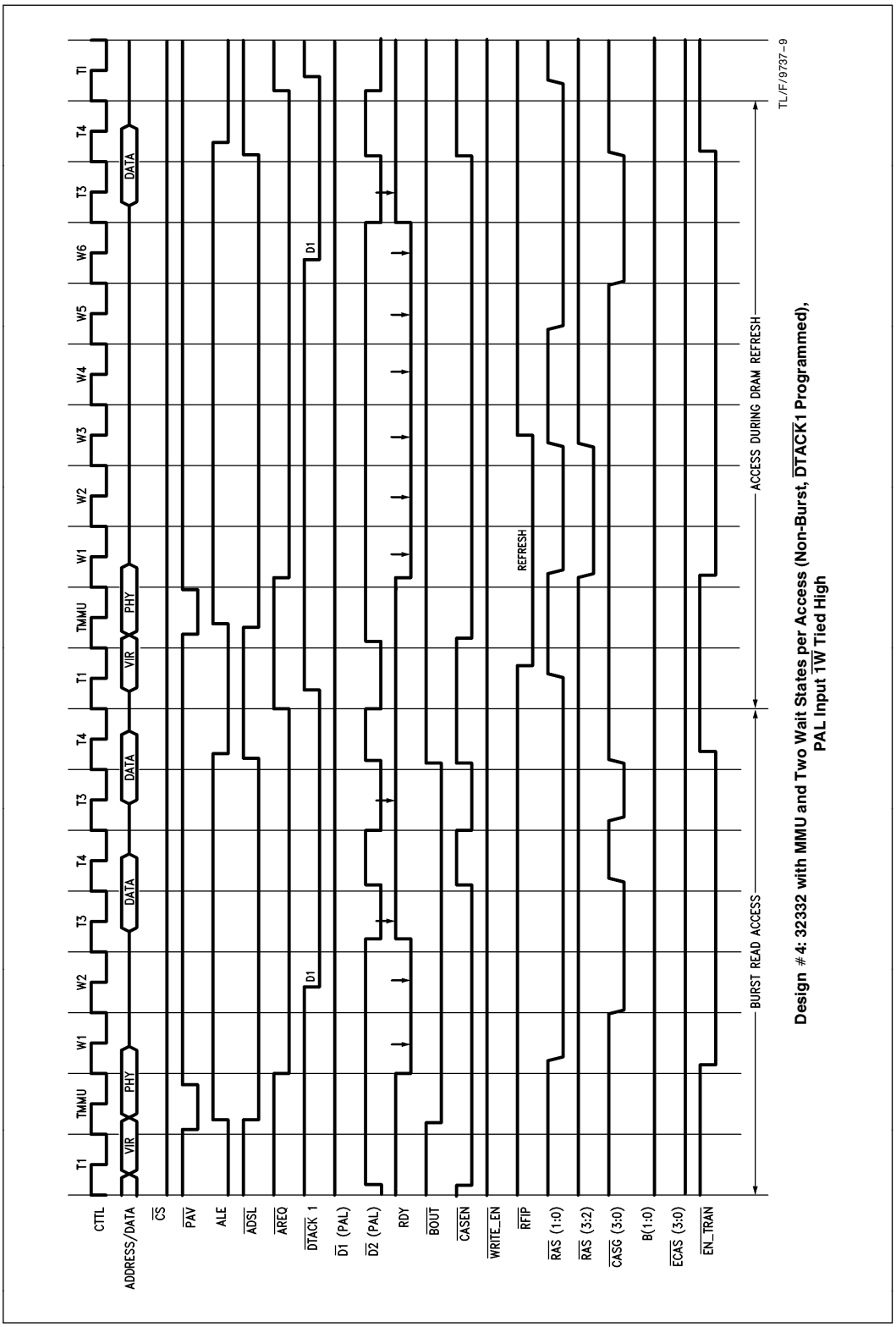
Design #3: 32332 with MMU and One Wait State per Access (Non-Burst), PAL Input $\overline{1W}$ Tied High



Design #3: 32332 with MMU and One Wait State per Access (Non-Burst), PAL Input 1W Tied High

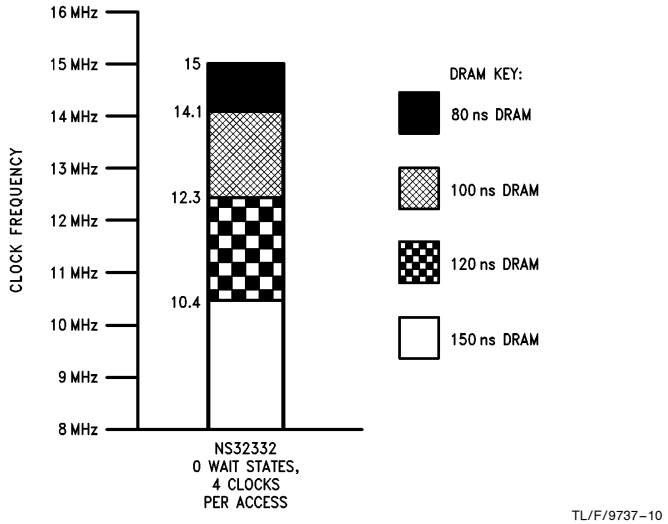


Design # 4: 32332 with MMU and Two Wait States per Access (Non-Burst, $\overline{\text{DTACK}}$1 Programmed), PAL Input $\overline{\text{1W}}$ Tied High



Design # 4: 32332 with MMU and Two Wait States per Access (Non-Burst, $\overline{\text{DTACK}}$1 Programmed), PAL Input 1W Tied High

Dram Speed Vs. Processor Speed, (Dram Speed References the RAS Access Time, tRAC, of the Dram, using DP8422A-25 Timing Specifications)



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