Interfacing the DP8420A/21A/22A to the 8086/186/88/188 Microprocessor

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I INTRODUCTION

This application note describes how to interface the 80186 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). It is assumed that the reader is already familiar with 80186 and the DP8422A modes of operation. This application note will also allow the 8086/88/188 to interface to the DP8420A/21A/22A.

II DESCRIPTION OF DESIGN, 8086/88/186/188 OPERATING AT UP TO 16 MHz (UP TO 12.5 MHz WITH 0 WAIT STATES)

The block diagram of this design is shown driving four banks of DRAM, each bank being 16 bits in width, giving a maximum memory capacity of up to 32 Mbytes (using 4 M-bit × 1 DRAMs).

The memory banks are interleaved on word (16-bit word) boundries. This means that the address bits (A1,2) is tied to the bank select inputs of the DP8422A (B0,1).

Address bit A0 is used, along with Bus High Enable ($\overline{BHE}$), to produce the two byte select data strobes. These byte selects (A0, $\overline{BHE}$) are used in byte reads and writes as well as selects for the transceivers.

This application allows 0 or more wait states to be inserted in normal accesses of the 8086/186/88/188. The number of wait states can be adjusted through the $\overline{WAITIN}$ input of the DP8422A.

The logic shown in this application note forms a complete 8086/186/88/188 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, Port B and refreshing the DRAM;

B. the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{RAS}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc);

C. performing byte writes and reads to the 16-bit words in memory.

If the system uses the 8086/88 the ''ALE'' output can be directly input to the DP8420A/21A/22A, the 74AS08 ''AND'' gate and the two 74AS04 inverters on the ''ALE'' output are not needed.

By using the ''output control'' pins of some external latches (74AS373's), this application can easily be used in a dual access application. The addresses could be tri-stated through these latches, the write input ($\overline{WIN}$), lock input ($\overline{LOCK}$), and $\overline{ECAS0\text{-}3}$ inputs must also be able to be tri-stated (a 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. If this design is used in a dual access application the t_{RAC} and t_{CAC} (required $\overline{RAS}$ and $\overline{CAS}$ access time required by the DRAM) will have to be recalculated since the time to $\overline{RAS}$ and $\overline{CAS}$ is longer for the dual access application (see TIMING section of this application note).

III 8086/186/88/188 DESIGN, 10 MHz WITH 0 WAIT STATES DURING NORMAL ACCESSES, PROGRAM MODE BITS

Programming Bits	Description
R0 = 0	$\overline{RAS}$ low two clocks, $\overline{RAS}$ precharge
R1 = 1	of two clocks. If more $\overline{RAS}$ precharge is desired the user should program three periods of $\overline{RAS}$ precharge.
R2 = 0	$\overline{WAIT}$ zero is chosen. $\overline{WAIT}$ follows
R3 = 0	the access $\overline{RAS}$ low.
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAIT}$ = 0, add one clock to $\overline{WAIT}$. $\overline{WAITIN}$ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access
R7 = 0	Select $\overline{WAIT}$
R8 = 1	Non-interleaved Mode
R9 = X	
C0 = X	Select based upon the input
C1 = X	''DELCLK'' frequency. Example: if the
C2 = X	input clock frequency is 10 MHz then choose C0,1,2 = 1,0,1 (divide by five, this will give a frequency of 2 MHz).
C3 = X	
C4 = 0	$\overline{RAS}$ banks selected by ''B0,1''. This
C5 = 1	mode allows one $\overline{RAS}$
C6 = 1	output to go low during an access, and allows byte writing in 16-bit words.
C7 = 1	Column address setup time of 0 ns.
C8 = 1	Row address hold time of 15 ns
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1	Fall through latches.
B1 = 0	Access mode 0
$\overline{ECAS}$0 = 0	$\overline{CAS}$ not extended beyond $\overline{RAS}$

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either high or low voltage level (don't care condition)

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IV 8086/186/88/188 TIMING CALCULATIONS FOR DESIGN AT 10 MHz WITH NO WAIT STATES DURING NORMAL ACCESSES

1. Minimum ALE high setup time to CLOCK high (DP8422A-20 needs 16 ns, #301a):

   100 ns (one clock period) − 9 ns (maximum delay through two 74AS04S) − 6 ns (74AS08 max delay) = 85 ns

2. Minimum address setup time to CLK high (DP8422A-20 needs 20 ns, #303):

   100 ns (one clock period) − 50 ns (min address valid delay, TCLAV parameter in 80C186 data sheet) − 6 ns (74AS373 max delay) + 1 ns (74ALS04B min delay) = 45 ns

3. Minimum $\overline{CS}$ setup time to clock high (DP8422-20 needs 14 ns, #300):

   45 ns (#2 above) − 10 ns (max 74ALS138 decoder) = 35 ns

4. Determining t_{RAC} during a normal access ($\overline{RAS}$ access time needed by the DRAM):

   200 ns (two clock periods to do the access) − 32 ns (CLK to $\overline{RAS}$ low max, DP8422-20 #307) − 15 ns (8086/186/88/188 data setup time, TDVCL) − 8 ns (74AS245A max delay) − 5 ns (74AS04 max delay, clock skew) = 140 ns

   Therefore the t_{RAC} of the DRAM must be 140 ns or less.

5. Determining t_{CAC} during a normal access ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   200 ns − 89 ns (CLK to $\overline{CAS}$ low on DP8422A-20, #308a) − 15 ns − 8 ns − 5 ns = 83 ns

   Therefore the t_{CAC} of the DRAM must be 83 ns or less.

6. Minimum SRDY (Synchronous ReaDY) setup time to SYSCLK low (CLK to DP8422A is inverted from SYSCLK), 8086/186/88/188 SRDY input needs 15 ns, TSRYCL:

   100 ns (one clock period) − 39 ns (DP8422A-20 max delay to $\overline{WAIT}$ 0 high after arbitration, parameter #17) = 61 ns

Note: Calculations can be performed for different frequencies, different logic (ALS or CMOS . . . etc), or the DP8422A-25, and/or different combinations of wait states by substatuting the appropriate values into the above equations.

V 8086/186/88/188 TIMING CALCULATIONS FOR DESIGN AT 16 MHz WITH ONE WAIT STATE DURING NORMAL ACCESSES (THE $\overline{WAITIN}$ INPUT OF THE DP8422A SHOULD BE TIED LOW)

1. Minimum ALE high setup time to CLOCK high (DP8422A-20 needs 16 ns, #301a):

   62.5 ns (one clock period) − 9 ns (maximum delay through two 74AS04s) − 6 ns (74AS08 max delay) = 47.5 ns

2. Minimum address setup time to CLK high (DP8422A-20 needs 20 ns, #303):

   62.5 ns (one clock period) − 33 ns (min address valid delay, TCLAV parameter in 80C186 data sheet) − 6 ns (74AS373 max delay) + 1 ns (74ALS04B min delay) = 24.5 ns

3. Minimum $\overline{CS}$ setup time to clock high (DP8422A-20 needs 14 ns, #300):

   24.5 ns (#2 above) − 10 ns (max 74ALS138 decoder) = 14.5 ns

4. Determining t_{RAC} during a normal access ($\overline{RAS}$ access time needed by the DRAM):

   182.5 ns (three clock periods to do the access) − 32 ns (CLK to $\overline{RAS}$ low max, DP8422A-20 #307) − 15 ns (8086/186/88/188 data setup time, TDVCL) − 8 ns (74S245A max delay) − 5 ns (74AS04 max delay, clock skew) = 122.5 ns

   Therefore the t_{RAC} of the DRAM must be 122.5 ns or less.

5. Determining t_{CAC} during a normal access ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

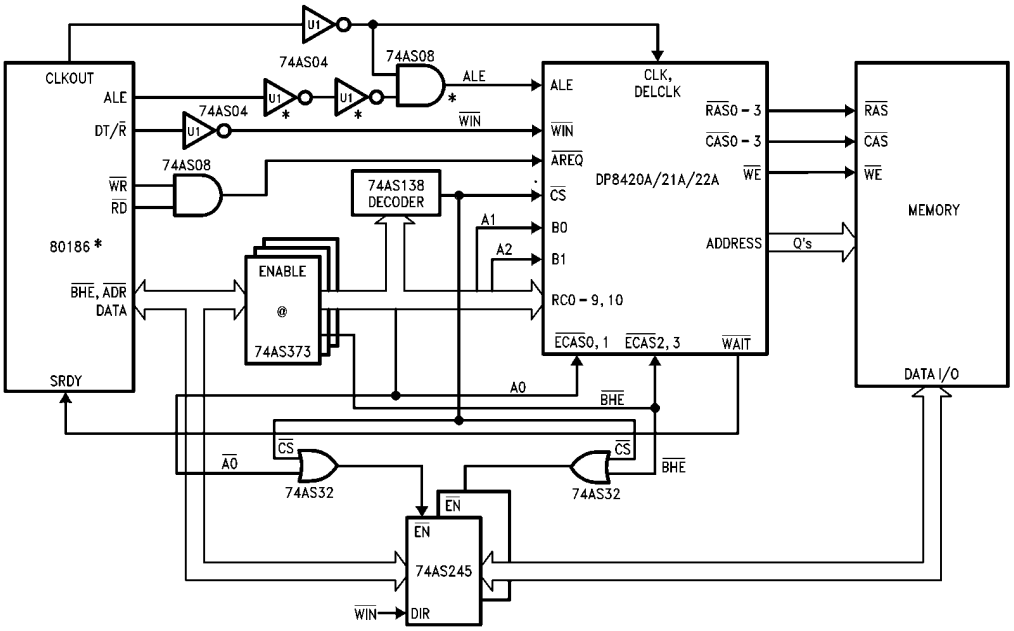
   182.5 ns − 89 ns (CLK to $\overline{CAS}$ low on DP8422A-20, #308a) − 15 ns − 8 ns − 5 ns = 65.6 ns

   Therefore the t_{CAC} of the DRAM must be 65.5 ns or less.

6. Minimum SRDY (Synchronous ReaDY) setup time to SYSCLK low (CLK to DP8422A is inverted from SYSCLK), 8086/186/88/188 SRDY input needs 15 ns, TSRYCL:

   62.5 ns (one clock period) − 39 ns (DP8422A-20 max delay to $\overline{WAIT}$ 1 high, parameter #17) = 23.5 ns

Note: Calculations can be performed for different frequencies, different logic (ALS or CMOS . . . etc), the DP8422A-25 and/or different combinations of wait states by substatuting the appropriate values into the above equations.



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@May not be needed in all memory applications

*If using the 8086/88 the two inverters (74AS04) and the ''AND'' gate (74AS08) are not needed, ALE from the 8086/88 can be directly connected to the DP8420A/21A/22A ALE input.

FIGURE 1. 80186 Block Diagram

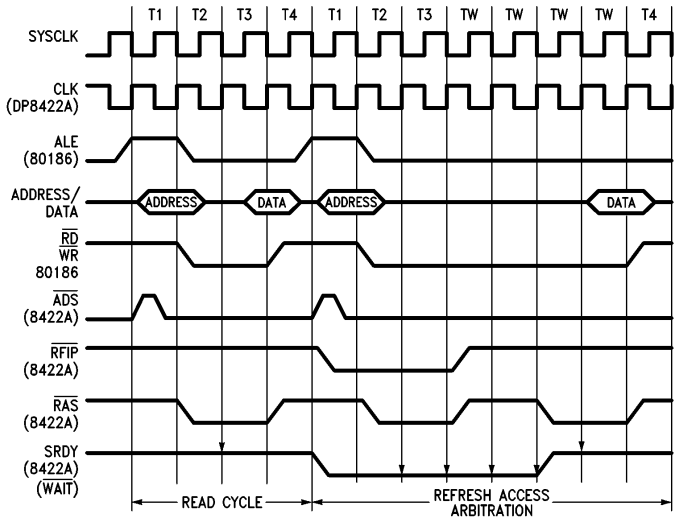

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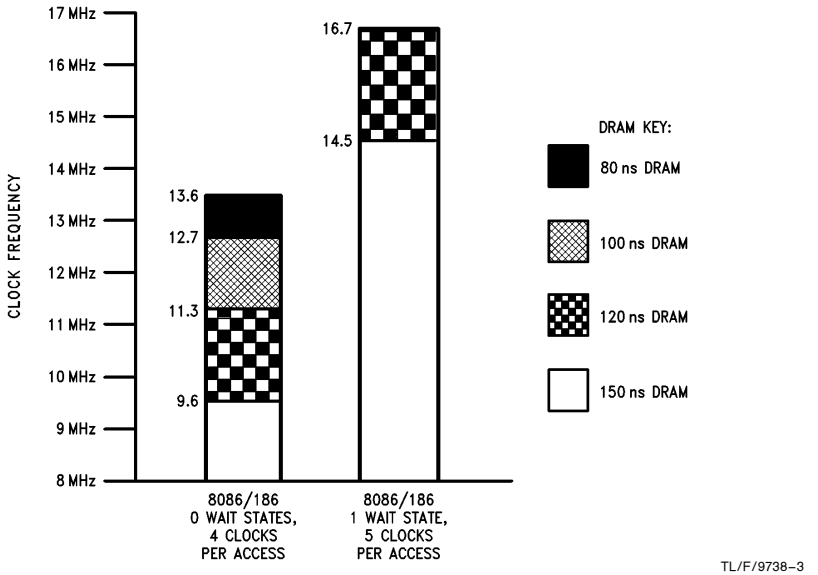
FIGURE 2. 80186 Timing

DRAM Speed Vs. Processor Speed, (DRAM Speed References the $\overline{RAS}$ Access Time, t_{RAC}, of the DRAM, using DP8422A-25 Timing Specifications)



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