Interfacing the DP8420A/21A/22A to the 80286

National Semiconductor
Application Note 545
Webster (Rusty) Meier Jr. and Joe Tate
November 1987

INTRODUCTION

This application note describes how to interface the 80286 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). There are three designs contained within this application note. The designs differ in terms of the maximum allowable frequency of operation. Design #1 can be used up to 16 MHz (80286-8) with one wait state. Design #2 can be used up to 20 MHz (80286-10) with one wait state. Design #3 can be used up to 25 MHz (80286-12) with one wait state. It is assumed that the reader is already familiar with 80286 access cycles and the DP8422A modes of operation.

DESCRIPTION OF DESIGN #1, ALLOWS UP TO 16 MHz OPERATION (CLOCK OUTPUT OF THE 82284) WITH NO WAIT STATES USING THE 80286-8

Design #1 (see *Figures 1 and 2*) consists of the DP8422A DRAM controller and several logic gates. These parts interface to the 80286 as shown in the block diagram. It accommodates two banks of DRAM, each bank being 16 bits in width, giving a maximum memory capacity of 16 Mbytes (using 4M-bit X 1 DRAMs). By choosing a different $\overline{RAS}$ and $\overline{CAS}$ configuration mode (see programming mode bits section of 8422A data sheet) this application could support 4 banks of DRAM, giving a memory capacity of 32 Mbytes (using 4M-bit X 1 DRAMs).

The memory banks are interleaved. This means that the least significant address bit (A1) is tied to the bank select input of the DP8422A (B1). Because the majority of accesses made by the 80286 will be sequential in nature, one memory bank can be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed. The interleaved memory system has higher system performance than a non-interleaved memory system. In a non-interleaved memory system, each sequential access will generally be to the same memory bank thereby requiring extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time.

The user can choose non-address pipelined mode for this design as long as the parameter ''$\overline{AREQ}$ negated to CLK high minimum to guarantee tASR = 0 ns'' is guaranteed (45 ns minimum for the 8422A-20, 39 ns for the 8422A-25). At 16 MHz, the user must choose address pipelined mode since it is not possible to meet the above parameter (62.5 ns one clock − 25 ns $\overline{MRDC}$,$\overline{MWRC}$ max valid − 5.5 ns 74AS08 max delay + 1 ns min 74AS00 $\overline{CLOCK}$ delay = 33.5 ns which is less than the 39 ns the DP8422A-25 needs). When using the DP8422A in address pipelined mode, the DRAMs chosen should need a minimum column address hold time of 32 ns or less.

The logic shown in this application note forms a complete 80286 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. Arbitration between Port A, Port B, and refreshing the DRAM;
B. The insertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{RAS}$ precharge is needed, refresh is occurring during a memory access, the other Port is currently doing an access . . . etc.);
C. Performing byte writes and reads to the 16-bit words in memory.

Since the $\overline{WE}$ output of the DP8422A becomes refresh request ($\overline{RFRQ}$) if the chip is programmed in address pipelining mode, the $\overline{WIN}$ signal was buffered to provide $\overline{WE}$ to the DRAMs.

The gates labeled ''U1'' should both be in the same package (74AS00) so that their delays cancel, see the TIMING section for how these delays cancel.

The ready logic can be made faster by programming $\overline{DTACK0}$ into the DP8422A and running this through a fast bipolar flip-flop clocked by $\overline{CLOCK}$.

By making use of the enable input on the 74AS373 latch, this application can easily be used in a dual access application. The addresses and chip select are TRI-STATE® through this latch, the write input ($\overline{WIN}$), lock input ($\overline{LOCK}$), and $\overline{ECAS}$0–3 inputs must also be able to be TRI-STATE (a 74AS244 could be used for this purpose). By multiplexing the above inputs, (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. All the timing (see TIMING section of this application note) will remain the same whether single or dual accessing is implemented.

DESCRIPTION OF DESIGN #2, ALLOWS UP TO 20 MHz OPERATION (CLOCK OUTPUT OF THE 82284) WITH NO WAIT STATES USING THE 80286-10

Design #2 (see *Figures 3, 4, 5*) is basically the same as Design #1 except for the following changes:

A. The circuit that produces $\overline{SRDY}$, the gate signal for the 74AS373 transparent latches, and $\overline{AREQ}$ has been changed to using $\overline{DTACK0}$, several 74AS374 flip-flops, and some logic gates. This was needed for speed in producing the gating signal of the 74AS373 (so as to get adequate address and chip select setup time),
B. The output ''D1'' which is used to produce the $\overline{AREQ}$ input was gated with $\overline{CS}$. This was done to guarantee that the $\overline{DTACK2}$ output becomes defined after power up,
C. This design will work at 20 MHz,
D. This design has zero wait states inserted in normal sequential accesses, multiple wait states may be inserted on multiple accesses to the same memory bank, during DRAM refreshing, or during accesses from Port B if dual accessing is used (DP8422A only).

In the 80286 READY LOGIC, the 74AS374 flip-flop that produces the D2 output has some gating at its inputs. This gating is used to synchronize the D2 output to the 80286 PCLK so as to end the access at the correct time.

The user can choose non-address pipelined mode for this design as long as the parameter ''$\overline{AREQ}$ negated to CLK high minimum to guarantee tASR = 0 ns'' is guaranteed

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

RRD-B30M115/Printed in U. S. A.

(45 ns minimum for the 8422A-20, 39 ns for the 8422A-25). At 20 MHz, the user should choose address pipelined mode since it is not possible to meet the above parameter (50 ns one clock − 8 ns 74AS374 max delay − 4.5 ns 74AS00 max delay + 1 ns min 74AS00 $\overline{\text{CLOCK}}$ delay = 38.5 ns which is less than the 39 ns the DP8422A-25 needs). The user should also keep in mind that when using the DP8422A in address pipelined mode the DRAMs chosen need a minimum column address hold time of 32 ns.

DESCRIPTION OF DESIGN #3, ALLOWS UP TO 25 MHz OPERATION (CLOCK OUTPUT OF THE 82284) WITH ONE WAIT STATE USING THE 80286-12

Design #3 (see *Figures 6, 7, 8*) is very similar to Design #2 except for the following changes:

A. The circuit that produces $\overline{\text{SRDY}}$, the gate signal for the 74AS373 transparent latches, and $\overline{\text{AREQ}}$ has been changed to use $\overline{\text{DTACK}}$2, a 74AS175 flip-flop, and some logic gates. This was needed because the 84288-12 was not known to be available, and also for speed in producing the gating signal of the 74AS373,

B. The $\overline{\text{AREQ}}$ input was gated with $\overline{\text{CS}}$ using gate ''U2''. This was done to guarantee that the $\overline{\text{DTACK2}}$ output becomes defined after power up,

C. This design will work at 25 MHz and possibly beyond, if the 80286 is ever produced at faster speeds (see the TIMING section for Design #3),

D. This design has one wait state inserted in normal sequential accesses, multiple wait states may be inserted on multiple accesses to the same memory bank, during DRAM refreshing, or during accesses from Port B if dual accessing is used (DP8422A only).

The user can choose non-address pipelined mode for this design as long as the parameter ''$\overline{\text{AREQ}}$ negated to CLK high minimum to guarantee tASR = 0 ns'' is guaranteed (45 ns minimum for the 8422A-20, 39 ns for the 8422A-25). At 25 MHz, the user must choose address pipelined mode since it is not possible to meet the above parameter (40 ns one clock − 7.5 ns 74AS175 max delay − 1 ns min 74AS00 $\overline{\text{CLOCK}}$ delay = 33.5 ns which is less than the 39 ns the DP8422A-25 needs). The user should also keep in mind that when using the DP8422A in address pipelined mode the DRAMs chosen need a minimum column address hold time of 32 ns.

In the 80286 READY LOGIC, the 74AS175 flip-flop that produces the D4 output has some gating at its inputs. This gating is used to synchronize the D4 output to the 80286 PCLK so as to end the access at the correct time.

80286 DESIGN #1, UP TO 16 MHz WITH NO WAIT STATES, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 0	$\overline{\text{RAS}}$ low two clocks, $\overline{\text{RAS}}$ precharge of
R1 = 1	two clocks. It should be noted that the user should choose R0,1 = 11 when operating above 16 MHz to allow enough $\overline{\text{RAS}}$ precharge time
R2 = 1	$\overline{\text{DTACK}}$ low one clock from $\overline{\text{RAS}}$ low
R3 = 0	
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 1	If $\overline{\text{WAITIN}}$ = 0, add two clocks to $\overline{\text{DTACK}}$
R7 = 1	Select $\overline{\text{DTACK}}$
R8 = X	The user may choose address pipelined mode (R8 = 0) remember to choose DRAMs with column address hold times of 32 ns or less, or non-address pipelined mode (R8 = 1), at clock frequencies below 16 MHz.
R9 = X	
C0 = X	Select based upon the input clock
C1 = X	frequency. Example: if the input clock
C2 = X	frequency is 12 MHz then choose C0,1,2 = 0,0,1 (divide by six, this will give a frequency of 2 MHz).
C3 = X	
C4 = 1	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ groups selected by ''B1''.
C5 = 1	This mode allows two $\overline{\text{RAS}}$ and two
C6 = 1	$\overline{\text{CAS}}$ outputs to go low during an access, and allows byte writing in 16-bit words.
C7 = 1	Column address setup time of 0 ns.
C8 = 1	Row address hold time of 15 ns.
C9 = 1	Delay $\overline{\text{CAS}}$ during write accesses to one clock after $\overline{\text{RAS}}$ transitions low
B0 = 1	Fall-thru latches
B1 = 0	Access mode 0
$\overline{\text{ECAS}}$0 = 0	Non-extend $\overline{\text{CAS}}$ mode

0 = Program with low voltage level

1 = Program with high voltage level

X = Program with either high or low voltage level (don't care condition)

80286 DESIGN #2, UP TO 20 MHz WITH NO WAIT STATES, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 1	$\overline{RAS}$ low four clocks, $\overline{RAS}$ precharge of three clocks
R1 = 1	
R2 = 0	$\overline{DTACK}$ low from $\overline{RAS}$ low
R3 = 0	
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. Since we are not using the $\overline{WAITIN}$ input it should be tied high on the DP8422A.
R7 = 1	Select $\overline{DTACK}$
R8 = X	The user may choose address pipelined mode (R8 = 0), remember to choose DRAMs with column address hold times of 32 ns or less or non-address pipelined mode (R8 = 1), at clock frequencies below 20 MHz
R9 = X	
C0 = X	Select based upon the input clock
C1 = X	frequency. Example: if the input clock
C2 = X	frequency is 16 MHz then choose C0,1,2 = 0,1,0 (divide by eight, this will give a frequency of 2 MHz).
C3 = X	
C4 = 1	$\overline{RAS}$ and $\overline{CAS}$ groups selected by ''B1''.
C5 = 1	This mode allows two $\overline{RAS}$ and $\overline{CAS}$
C6 = 1	outputs to go low during an access, and allows byte writing in 16-bit words.
C7 = 1	Column address setup time of 0 ns.
C8 = 1	Row address hold time of 15 ns.
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1	Fall-thru latches
B1 = 0	Access mode 0
$\overline{ECAS}$0 = 0	Non-extend $\overline{CAS}$ mode

0 = Program with low voltage level

1 = Program with high voltage level

X = Program with either high or low voltage level (don't care condition)

80286 DESIGN #3, UP TO 25 MHz WITH ONE WAIT STATE, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 1	$\overline{RAS}$ low four clocks, $\overline{RAS}$ precharge of three clocks
R1 = 1	
R2 = 1	$\overline{DTACK}$ low one clock from $\overline{RAS}$ low
R3 = 0	
R4 = 0	No WAIT states during burst accesses
R5 = 0	
R6 = 0	If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. Since we are using $\overline{DTACK2}$ the $\overline{WAITIN}$ input should be tied low on the DP8422A.
R7 = 1	Select $\overline{DTACK}$
R8 = X	The user must choose address pipelined mode (R8 = 0), at clock frequencies above 20 MHz. Also remember to choose DRAMs with column address hold times of 32 ns or less or non-address pipelined mode (R8 = 1), at clock frequencies below 20 MHz
R9 = X	
C0 = X	Select based upon the input clock
C1 = X	frequency. Example: if the input clock
C2 = X	frequency is 12 MHz then choose C0,1,2 = 0,0,1 (divide by six, this will give a frequency of 2 MHz). For a CPU frequency of 24 MHz the clock could be divided by two initially to give a 12 MHz input to the DELCLK input of the DP8422A.
C3 = X	
C4 = 1	$\overline{RAS}$ and $\overline{CAS}$ groups selected by ''B1''.
C5 = 0	This mode allows two $\overline{RAS}$ and two
C6 = 1	$\overline{CAS}$ outputs to go low during an access, and allows byte writing in 16-bit words.
C7 = 1	Column address setup time of 0 ns.
C8 = 1	Row address hold time of 15 ns.
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low
B0 = 1	Fall-thru latches
B1 = 0	Access mode 0
$\overline{ECAS}$0 = 0	Non-extend $\overline{CAS}$ mode

0 = Program with low voltage level

1 = Program with high voltage level

X = Program with either high or low voltage level (don't care condition)

**80286, DESIGN #1, ACCESS MODE 0,
16 MHz TIMING (80286-8) WITH NO
WAIT STATES DURING SEQUENTIAL ACCESSES**

1. Maximum time to address valid:

   $\overline{MRDC}$, $\overline{MWTC}$ make 74AS373 fall-thru at 25 ns (max) from CLOCK low + 5.5 ns (74AS08) + 11.5 ns (74AS373 enable time) = 42 ns

2a. Maximum time to ALE high from CLOCK:

   40 ns (max status valid) + 4.5 ns (74AS00) = 44.5 ns

2b. Maximum time to ALE high from $\overline{CLOCK}$ (DP8422A CLK):

   40 ns (max status valid) + 0 ns (74AS00 delays of $\overline{CLOCK}$ and ALE cancel out) = 40 ns

3. Minimum ALE high setup time to $\overline{CLOCK}$ high (DP8422A-20 needs 16 ns):

   62.5 ns (one clock period) − 40 ns (#2b, the 74AS00 U1 delays in the $\overline{CLOCK}$ and the ALE path will cancel out) = 22.5 ns

4. Minimum address setup time to $\overline{CLOCK}$ high (DP8422A-20 needs 20 ns):

   62.5 ns (one clock period) + 1 ns (min 74AS00 delay, $\overline{CLOCK}$) − 42 ns (#1) = 21.5 ns

5a. Maximum $\overline{CS}$ valid time from $\overline{CLOCK}$ high:

   60 ns (maximum address valid from phase two of previous clock) + 22 ns (maximum prop delay of 74ALS138) − 1 ns (minimum 74AS00 $\overline{CLOCK}$ delay) = 81 ns,

   THIS IS EQUAL TO 18.5 NS FROM PHASE ONE OF THE CURRENT ''TS'' INVERTED CLOCK ($\overline{CLOCK}$, 81 ns − 62.5 ns = 18.5 ns).

5b. Maximum time to active high gating signal to 74AS373 transparent latch from $\overline{CLOCK}$:

   25 ns ($\overline{MRDC}$, $\overline{MWRC}$ maximum delay to inactive) + 5.5 ns (maximum 74AS08 delay) − 1 ns (minimum 74AS00 $\overline{CLOCK}$ delay) = 29.5 ns,

   AS CAN BE SEEN $\overline{CS}$ PRECEDES THIS ACTIVE HIGH GATING SIGNAL, THEREFORE THE MAXIMUM TIME TO THE GATING SIGNAL DETERMINES THE MAXIMUM TIME TO A VALID CHIP SELECT.

5c. Minimum $\overline{CS}$ setup time to $\overline{CLOCK}$ high (DP8422A-20 needs 14 ns):

   62.5 ns (one clock period) − 29.5 ns (#5b) − 11.5 ns (maximum enable time to valid output for 74AS373) = 21.5 ns

6. Determining tRAC ($\overline{RAS}$ access time needed by the DRAM):

   250 ns (TS + TC) − 62.5 ns (one clock) − 4.5 ns (74AS04 delay) − 10 ns (data setup time) − 7.5 ns (74AS245) − 32 ns (CLK to $\overline{RAS}$ low on DP8422A-25) = 133.5 ns

   Therefore the tRAC of the DRAM must be 133.5 ns or less.

7. Determining tCAC ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   250 ns − 62.5 − 4.5 − 10 ns − 7.5 ns − 89 ns (CLK to $\overline{CAS}$ low on DP8422A-25) = 76.5 ns

   Therefore the tCAC of the DRAM must be 76.5 ns or less.

8. Maximum time to $\overline{DTACK}$1 low:

   62.5 ns (One clock) + 4.5 ns (max 74AS04 $\overline{CLOCK}$ delay) +41 ns ($\overline{DTACK}$0 low from CLK high) = 108 ns

9. Minimum $\overline{DTACK}$1 setup time to $\overline{SRDY}$ being sampled (15 ns is needed by the 80286):

   125 ns (two clock periods) − 108 ns (#8) = 17 ns

*****IF FASTER SPEEDS ARE DESIRED THE USER CAN USE THE DP8422A-25.**

**80286, DESIGN #2, ACCESS MODE 0,
20 MHz TIMING (80286-10) WITH ZERO
WAIT STATES DURING SEQUENTIAL ACCESSES**

1. Maximum time to address valid:

   The ''G'' input makes the 74AS373 fall-thru at 8 ns (max) from $\overline{CLOCK}$ high (8 ns max delay of 74AS374 low to high) + 11.5 ns (74AS373 enable time) = 19.5 ns

2a. Maximum time to ALE high from CLOCK:

   28 ns (max status valid) + 4.5 ns (74AS00) = 32.5 ns

2b. Maximum time to ALE high from $\overline{CLOCK}$ (DP8422A CLK):

   28 ns (max status valid) + 0 ns (74AS00 delays of $\overline{CLOCK}$ and ALE cancel out) = 28 ns

3. Minimum ALE high setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 15 ns):

   50 ns (one clock period) − 28 ns (#2b, the 74AS00 U1 delays in the $\overline{CLOCK}$ and the ALE path will cancel out) = 22 ns

4. Minimum address setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 18 ns):

   50 ns (one clock period) − 19.5 ns (#1) = 30.5 ns

5a. Maximum $\overline{CS}$ valid time from $\overline{CLOCK}$ high:

   47 ns (maximum address valid from phase two of previous clock) + 22 ns (maximum prop delay of 74ALS138) − 1 ns (minimum 74AS00 $\overline{CLOCK}$ delay) = 68 ns,

   THIS IS EQUAL TO 18 NS FROM PHASE ONE OF THE CURRENT ''TS'' INVERTED CLOCK ($\overline{CLOCK}$).

5b. Maximum time to $\overline{AREQ}$ (active high gating signal to 74AS373 transparent latch from $\overline{CLOCK}$:

   8 ns (max delay of gate (D1) output of 74AS374 low to high from $\overline{CLOCK}$) + 4.5 ns (74AS00, $\overline{AREQ}$ is output) = 12.5 ns

   AS CAN BE SEEN $\overline{CS}$ SUCCEEDS THIS ACTIVE HIGH GATING SIGNAL, THEREFORE THE MAXIMUM TIME TO CHIP SELECT DETERMINES THE MAXIMUM TIME TO A VALID LATCHED CHIP SELECT.

5c. Minimum $\overline{CS}$ setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 13 ns):

   50 ns (one clock period) − 18 ns (#5a) − 11.5 ns (maximum enable time to valid output for 74AS373) = 20.5 ns

6. Determining tRAC ($\overline{RAS}$ access time needed by the DRAM):

   200 ns (TS + TC) − 50 ns (one clock) − 4.5 ns (74AS04 delay, $\overline{CLOCK}$) − 8 ns (data setup time) − 7.5 ns (74AS245) − 26 ns (CLK to $\overline{RAS}$ low on DP8422A-25) = 104 ns

   Therefore the tRAC of the DRAM must be 104 ns or less.

7. Determining tCAC ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   200 ns − 50 − 4.5 − 8 ns − 7.5 ns − 79 ns (CLK to $\overline{CAS}$ low on DP8422A-25) = 51 ns

   Therefore the tCAC of the DRAM must be 51 ns or less.

8. Minimum setup time of D0 low (from $\overline{DTACK}$0) to $\overline{CLOCK}$ (74AS374 needs 3 ns):

   50 ns (one clock) − 33 ns ($\overline{DTACK}$0 low from CLK high) − 4.5 ns (max delay of 74AS02) = 12.5 ns

9. Minimum PCLK setup to $\overline{CLOCK}$ (rising edge of 74AS374, needs 3 ns):

   50 ns (one clock) − 35 ns (max PCLK delay) − 5 ns (max 74AS04 delay) − 4.5 ns (max delay of 74AS02) = 5.5 ns

10. Minimum $\overline{SRDY}$ setup time to clock where it is sampled (15 ns is needed by the 80286):

    50 ns (one clock period) − 8 ns (max delay low to high of ''Q'' output of 74AS374) − 4.5 ns (max delay of 74AS00) − 4.5 ns (max delay of 74AS00, $\overline{CLOCK}$) = 33 ns

80286, DESIGN #3, ACCESS MODE 0, 25 MHz TIMING (80286-12) WITH ONE WAIT STATE DURING SEQUENTIAL ACCESSES

1. Maximum time to address valid:

   The ''G'' input makes the 74AS373 fall-thru at 7.5 ns (max) from $\overline{CLOCK}$ high (7.5 ns max delay of 74AS175 low to high) + 11.5 ns (74AS373 enable time) = 19 ns

2a. Maximum time to ALE high from CLOCK:

   22 ns (max status valid) + 4.5 ns (74AS00) = 26.5 ns

2b. Maximum time to ALE high from $\overline{CLOCK}$ (DP8422A CLK):

   22 ns (max status valid) + 0 ns (74AS00 delays of $\overline{CLOCK}$ and ALE cancel out) = 22 ns

3. Minimum ALE high setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 15 ns):

   40 ns (one clock period) − 22 ns (#2b, the 74AS00 U1 delays in the $\overline{CLOCK}$ and the ALE path will cancel out) = 18 ns

4. Minimum address setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 18 ns):

   40 ns (one clock period) − 19 ns (#1) = 21 ns

5a. Maximum $\overline{CS}$ valid time from $\overline{CLOCK}$ high:

   37 ns (maximum address valid from phase two of previous clock) + 14 ns (maximum prop delay of 74ALS139) − 1 ns (minimum 74AS00 $\overline{CLOCK}$ delay) = 50 ns,

   THIS IS EQUAL TO 10 NS FROM PHASE ONE OF THE CURRENT ''TS'' INVERTED CLOCK ($\overline{CLOCK}$).

5b. Maximum time to active high gating signal to 74AS373 transparent latch from $\overline{CLOCK}$:

   7.5 ns (max delay of gate ($\overline{D3}$) output of 74AS175 low to high from $\overline{CLOCK}$)

   AS CAN BE SEEN $\overline{CS}$ SUCCEEDS THE ACTIVE HIGH GATING SIGNAL, THEREFORE THE MAXIMUM TIME TO $\overline{CS}$ VALID DETERMINES THE MAXIMUM TIME TO A VALID CHIP SELECT.

5c. Minimum $\overline{CS}$ setup time to $\overline{CLOCK}$ high (DP8422A-25 needs 13 ns):

   40 ns (one clock period) − 10 ns (#5a) − 11.5 ns (maximum enable time to valid output for 74AS373) = 18.5 ns

6. Determining tRAC ($\overline{RAS}$ access time needed by the DRAM):

   240 ns (TS + TC + TC) − 40 ns (one clock) − 4.5 ns (74AS04 delay, $\overline{CLOCK}$) − 8 ns (data setup time) − 7.5 ns (74AS245) − 26 ns (CLK to $\overline{RAS}$ low on DP8422A-25) = 154 ns

   Therefore the tRAC of the DRAM must be 154 ns or less.

7. Determining tCAC ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

   240 ns − 40 − 4.5 − 8 ns − 7.5 ns − 79 ns (CLK to $\overline{CAS}$ low on DP8422A-25) = 101 ns

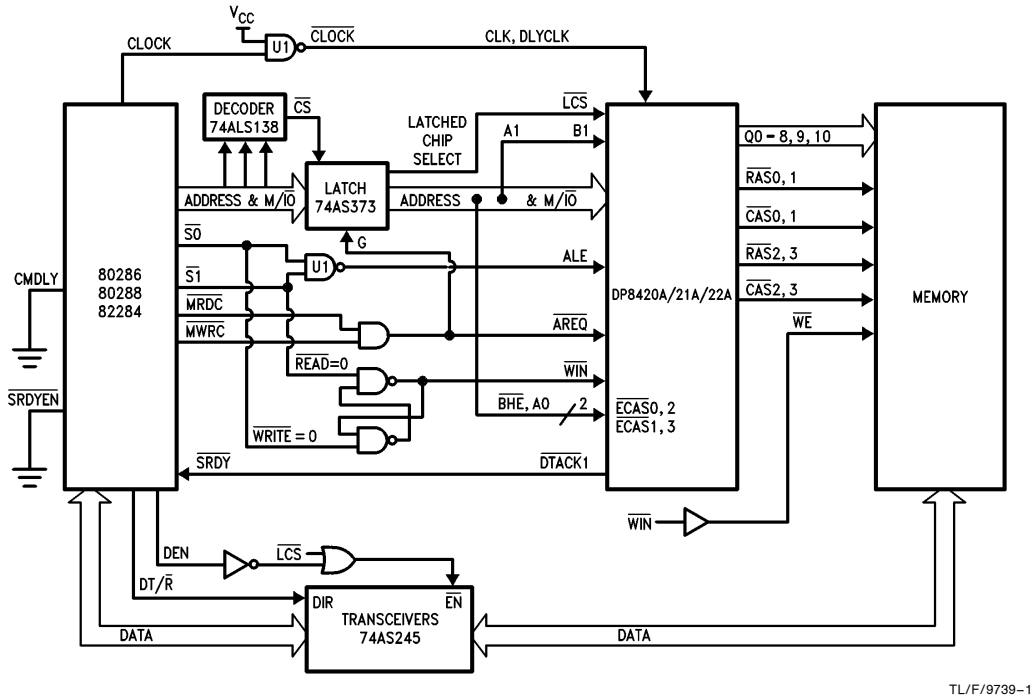
   Therefore the tCAC of the DRAM must be 101 ns or less.

8. Minimum setup time of $\overline{D2}$ low (from $\overline{DTACK}$2) to $\overline{CLOCK}$ (74AS175 needs 3 ns):

   40 ns (one clock) − 28 ns ($\overline{DTACK}$2 low from CLK high) − 4.5 ns (max delay of 74AS02) = 7.5 ns

9. Minimum $\overline{SRDY}$ setup time to clock where it is sampled (15 ns is needed by the 80286):

   40 ns (one clock period) − 10 ns (max delay high to low of $\overline{Q}$ output of 74AS175) − 4.5 ns (max delay of 74AS00, $\overline{CLOCK}$) = 25.5 ns



TL/F/9739–1

FIGURE 1. 80286 Block Diagram of Design # 1, Mode 0, up to 16 MHz

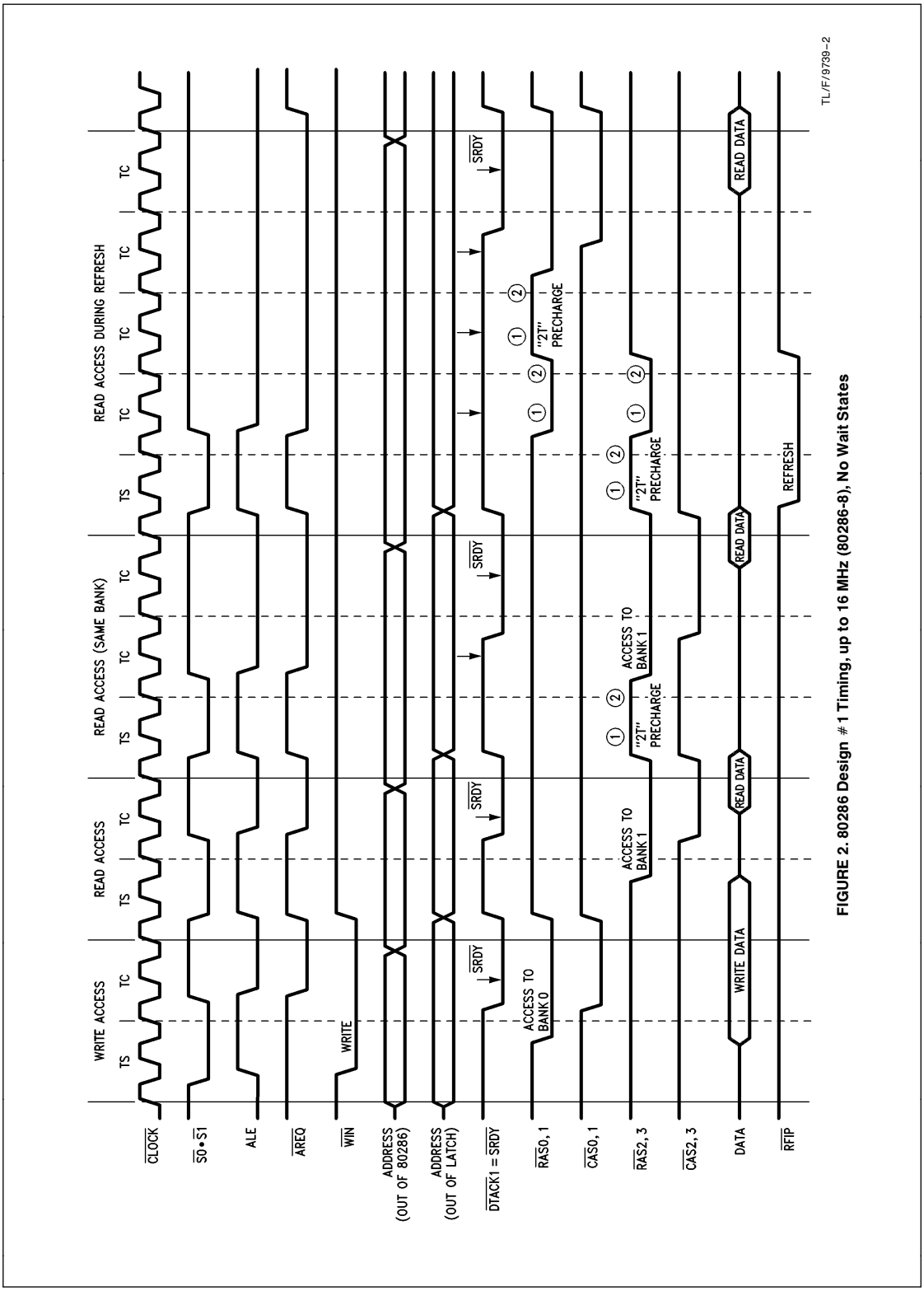
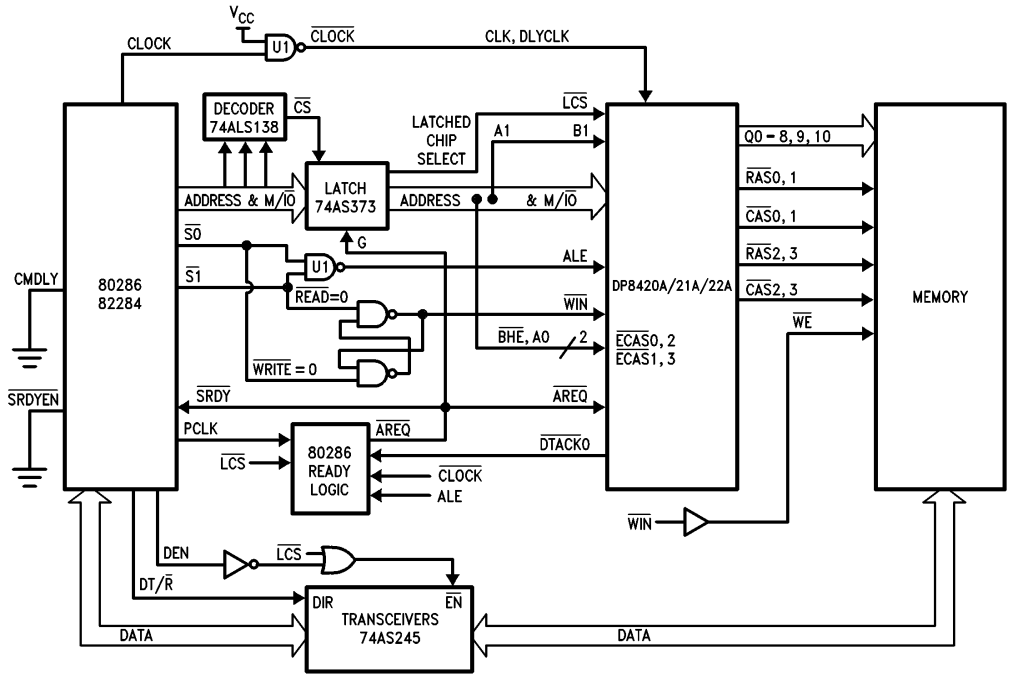
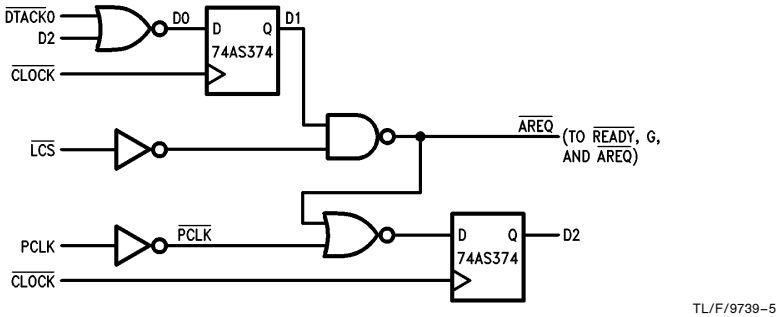


FIGURE 2. 80286 Design #1 Timing, up to 16 MHz (80286-8), No Wait States



TL/F/9739–4

FIGURE 3. 80286 Block Diagram of Design #2, Mode 0, up to 20 MHz



TL/F/9739–5

FIGURE 4. 80286 Ready Logic for Design #2

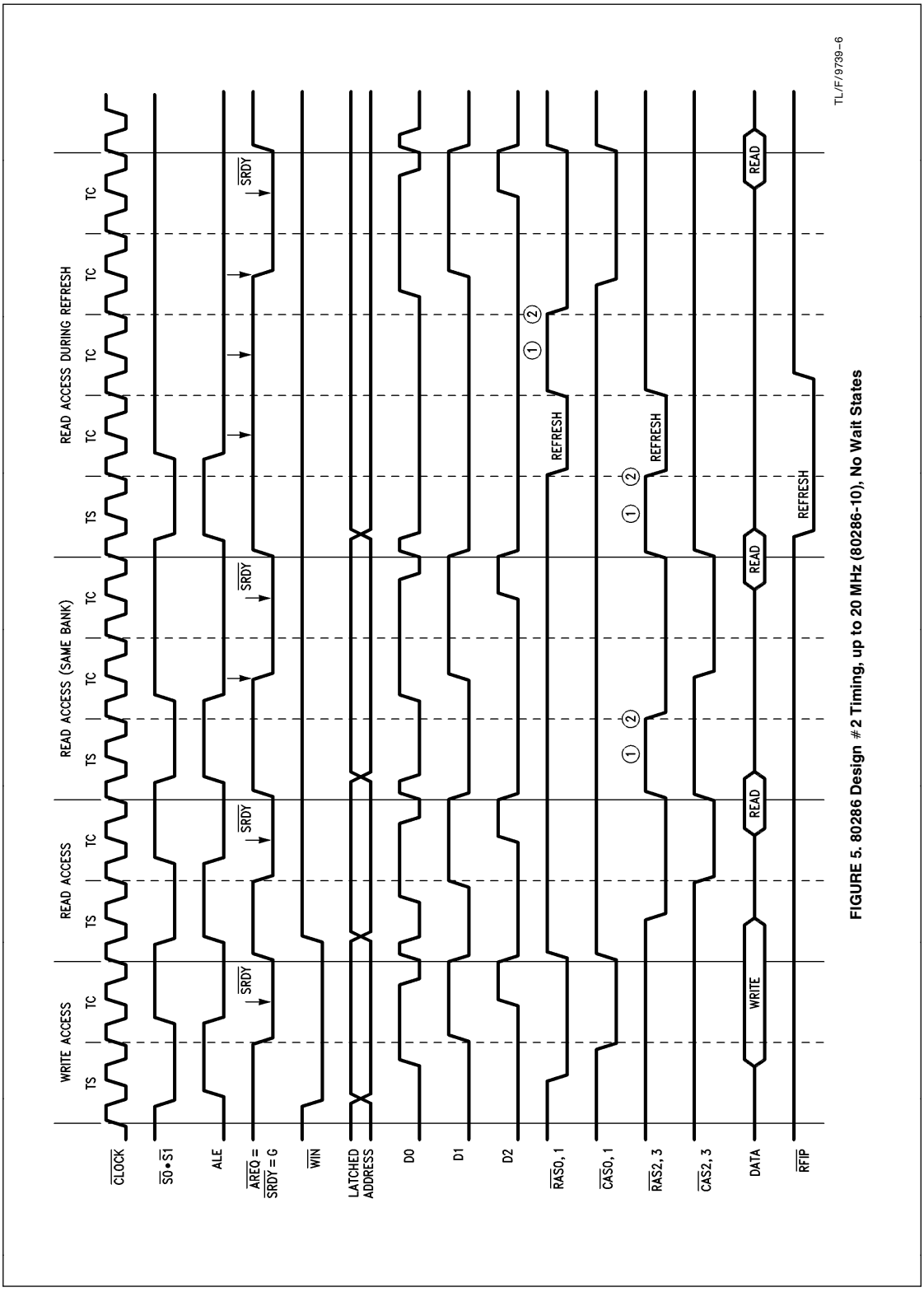
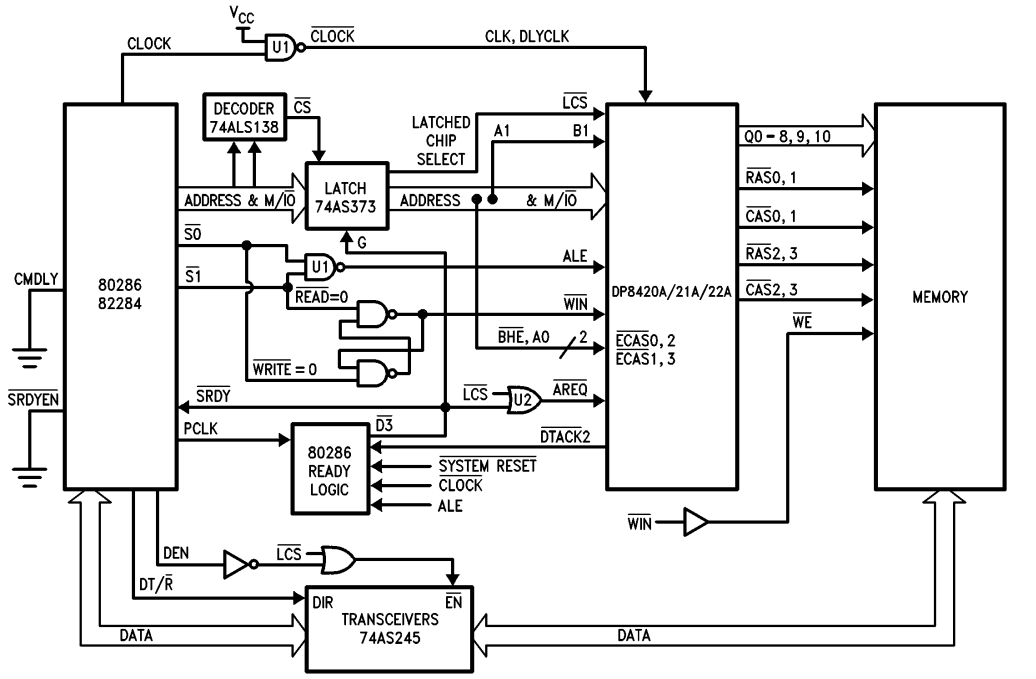
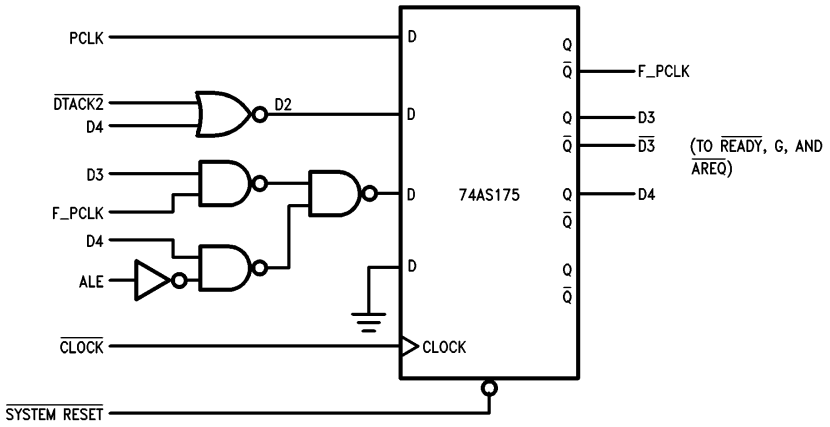


FIGURE 5. 80286 Design #2 Timing, up to 20 MHz (80286-10), No Wait States



TL/F/9739–8

FIGURE 6. 80286 System Block Diagram of Design #3, Mode 0, up to 25 MHz



TL/F/9739–9

FIGURE 7. 80286 Ready Logic for Design #3

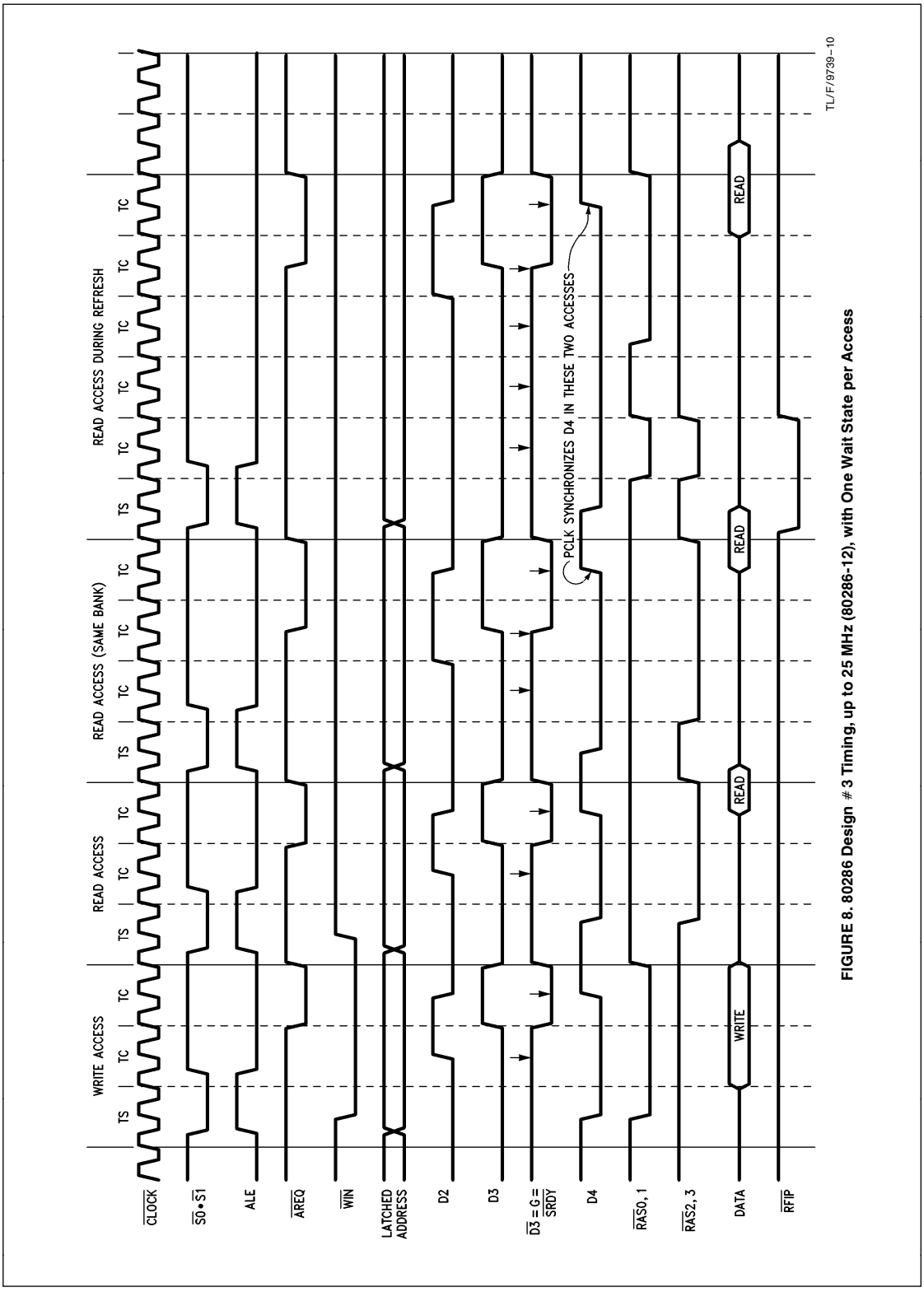
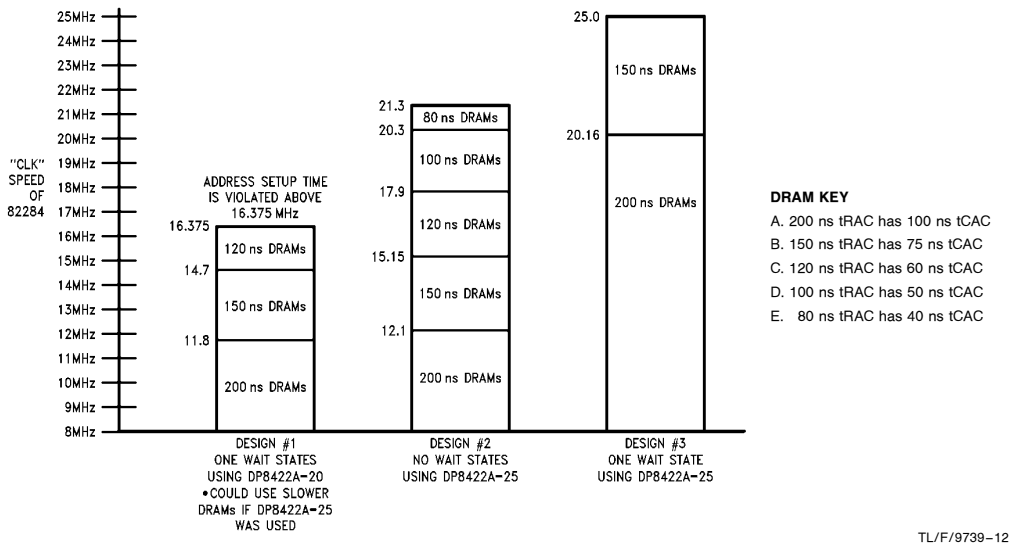


FIGURE 8. 80286 Design # 3 Timing, up to 25 MHz (80286-12), with One Wait State per Access



TL/F/9739–12

FIGURE 9. 80286, DRAM Speed vs. Processor Speed (the Processor Speed is Referencing the "CLK" Output of 82284, the DRAM Speed is Referencing the $\overline{RAS}$ Access Time "tRAC" of the DRAM)

Lit. # 100545

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408