Interfacing the DP8420A/21A/22A to the 29000 Utilizing the Burst Access Mode

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INTRODUCTION

This application note describes how to interface the 29000 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). The DP8422A supports the 29000 in the burst access mode. It is assumed that the reader is already familiar with 29000 access cycles and the DP8422A modes of operation.

IA. Description of Designs #1 and #2, the 29000 in burst access mode on the instruction bus, allowing operation up to 25 MHz with four wait states in normal accesses and one or two wait states in burst accesses

The two designs of this application note consist of the DP8422A DRAM controller, a single PAL® (PAL16L8D), several flip-flops, and several logic gates. These parts interface to the 29000 as shown in the block diagrams. This design accommodates two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4M-bit X 1 DRAMs).

This memory design supports burst accesses by the 29000 to the instruction bus but could also support burst accessing to the data bus given a few minor changes. Design #1 inserts 4 wait states in normal accesses and 2 wait states in burst accesses. Design #2 inserts 4 wait states in normal accesses and 1 wait state in burst accesses. When idle states occur during a burst access the next occurring access will only have one wait state.

This application allows page mode DRAMs to be used by holding $\overline{RAS}$ low after an access is completed ($\overline{IRDY}$ low) until either a refresh request or a new access request ($\overline{IREQ}$) is generated. If $\overline{IBREQ}$ (Instruction Burst Request) has transitioned low the next sequential word is accessed from the DRAM via a page mode access. This access involves incrementing the column address (DP8422A COLINC input high) and toggling the $\overline{CAS}$ outputs via the PAL $\overline{ECAS}$ output. The instruction burst acknowledge ($\overline{IBACK}$) input is driven low except in the case of a refresh request ($\overline{RFRQ}$) or a new access ($\overline{IREQ}$) being requested.

If the user wants to do dual accessing with the DP8422A DRAM controller, address buffers (74AS244s) must be added to the address, $\overline{ECAS}$0–3, $\overline{LOCK}$, and $\overline{WIN}$ inputs.

Note that the DP8422A DRAM controller could be used to allow instruction memory accessing thru Port A. The instruction memory could be loaded thru a data memory interface to Port B.

The logic shown in these applications form a complete 29000 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, and refreshing the DRAM:
B. the insertion of wait states to the processor (Port A) when needed;
C. remaining in burst access mode unless a refresh request ($\overline{RFRQ}$) or new instruction request is generated;
D. incrementing the column address during burst mode accesses; and
E. guaranteeing the $\overline{RAS}$ and $\overline{CAS}$ low and precharge times.

The timing calculations for this design are included in this application note.

When using the DP8420A/21A/22A at or above 20 MHz the user should program three clock periods of precharge. This is because two clock periods of precharge at 20 MHz will only guarantee 77 ns of $\overline{RAS}$ precharge (2 $\times$ 50 ns $-$ tD1, parameter #50 ''14 ns'' $-$ clock (20 MHz) to $\overline{AREQ}$ high ''9 ns'').

IB. High Performance NO WAIT State 29000 System

A higher performance 29000 system (similar to the ones discussed in this application note) could be designed using the DP8422A by accessing four $\overline{RAS}$ banks at once, this could allow zero wait state burst accesses. An example of this method using 2 DRAM banks is shown at the end of this application note. If 2 DRAM controllers were used (4 BANKs) burst accesses could execute in zero wait states. The COLINC inputs to the two DRAM controllers would be staggered in time as well as the four $\overline{ECAS}$ outputs (B0$\overline{ECAS}$–B3$\overline{ECAS}$) from the 29000 control logic block.

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II. 29000 Programming mode bits

Programming Bits	Description
R0 = 1 R1 = 1	$\overline{RAS}$ low four clocks, $\overline{RAS}$ precharge of three clocks
R2 = 1 R3 = 0	$\overline{DTACK}$ will be asserted on the positive edge of CLK following the access $\overline{RAS}$
R4 = 0 R5 = 0 R6 = X R7 = 1	No WAIT states during burst accesses $\overline{DTACK}$ output
R8 = 1 R9 = X	Non-address pipelining to support burst accessing
C0 = X C1 = X C2 = X	Select based upon the input clock frequency. Example: if the DELCLK frequency is 20 MHz then choose C0,1,2 = 0,0,0 (divide by ten, this will give a frequency of 2 MHz).
C3 = X	
C4 = 0 C5 = 0 C6 = 1	$\overline{RAS}$ and $\overline{CAS}$ groups selected by ''B1''. This mode allows two $\overline{RAS}$ and four $\overline{CAS}$ outputs to go low during an access.
C7 = 1 C8 = 1	Column address setup time of 0 ns. Row address hold time of 15 ns
C9 = 1	Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low.
B0 = 0 B1 = 1	Latching of the address inputs, needed for the burst accessing capability of the 29000 (COLINC input in particular). Access mode 1

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either low voltage level (don't care condition)

III. 29000 25 MHz timing calculations for Design #1 and Design #2, with four wait states per normal access and one or two wait states per burst access

1. Maximum time to address valid (with respect to 25 MHz clock):

   14 ns (29000 data sheet #6)

2. Maximim time to $\overline{ADS}$ low (with respect to 25 MHz clock):

   9 ns (74AS374 clock to Q, tPHL)

3. Minimum $\overline{ADS}$ low setup time to CLK high (DP8422-25 needs 25 ns, #400b):

   40 ns (one clock period, 25 MHz) − 9 ns (#2) = 31 ns

4. Minimum address setup time to $\overline{ADS}$ low (DP8422-25 needs 14 ns, #404):

   40 ns (One clock period, 25 MHz) + 2 ns (minimum 74AS374 clock to Q) − 14 ns (#1) = 28 ns

5. Minimum $\overline{CS}$ setup time to CLKA high (DP8422-25 needs 5 ns, #401):

   24 ns (#4) − 9 ns (74AS138 decoder = 15 ns

6. Determining tRAC ($\overline{RAS}$ access time needed by the DRAM):

   200 ns (five clock periods at 25 MHz) − 40 ns (one clock period, T1) − 9 ns (#2) − 6 ns (29000 data setup time, #9a) − 7 ns (74F245) − 29 ns (CLK to $\overline{RAS}$ low) = 109 ns

   Therefore the tRAC of the DRAM must be 109 ns or less.

7. Determining tCAC ($\overline{CAS}$ access time needed by the DRAM) and tAA (column address access time):

   200 ns − 40 ns − 9 ns − 6 ns − 7 ns − 82 ns (CLK to $\overline{CAS}$ low) = 56 ns

   Therefore the tCAC and tAA (access time from the column address) of the DRAM must be 56 ns or less. COMMON 100 ns DRAMS WILL MEET THIS tRAC, tAA, AND tCAC PARAMETER.

8. Minimum setup of $\overline{DTACK}$1 to the 74AS374 ONLY, (need 2 ns):

   40 ns (one clock period) − 28 ns (DP8422A-25 $\overline{DTACK}$1 delay, #18) = 12 ns

9. Minimum $\overline{IRDY}$ setup time to $\overline{IRDY}$ being sampled (12 ns is needed by the 29000, #9):

   40 ns (one clock period) − 9 ns (maximum 74AS374 clock to Q output delay) = 31 ns

10a. Determining tCAC during a burst access for Design #1:

120 ns (3 clock periods) − 20 ns (one half clock period during which $\overline{CAS}$ is high) − 10 ns (PAL16L8 maximum propagation delay) − 12 ns (74AS32 propagation delay driving ≈ 125 pF with damping resistor and other associated delays) − 6 ns (data setup time) − 7 ns (74F245) = 65 ns

Therefore the tCAC of the DRAM must be ≤ 65 ns

10b. Determining tCAC during a burst access for Design #2:

80 ns (2 clock periods) − 20 ns (one half clock period during which $\overline{CAS}$ is high) − 10 ns (PAL16L8 maximum propagation delay) − 12 ns (74AS32 propagation delay driving ≈ 125 pF with damping resistor and other associated delays) − 6 ns (data setup time) − 7 ns (74F245) = 25 ns

Therefore the tCAC of the DRAM must be ≤ 25 ns

11a. Determining tAA during a burst access for Design #1: 160 ns (4 clock periods, because $\overline{IRDY}$ inverted is COLINC) − 39 ns (DP8422A COLINC to Q's valid, #27) = 121 ns ≥ tAA.

11b. Determining tAA during a burst access for Design #2: 120 ns (3 clock periods, because $\overline{IRDY}$ inverted is COLINC) − 39 ns (DP8422A COLINC to Q's valid, #27) = 81 ns ≥ tAA.

IV. 29000 PAL equations, Design #1, 2 wait states during burst accesses. Written in National Semiconductor PLAN™ format

PAL16L8D

CLK $\overline{CS}$ $\overline{IREQ}$ $\overline{IBREQ}$ $\overline{DTACK2}$ $\overline{AREQ}$ $\overline{IRDY}$ $\overline{IRDY3}$ $\overline{RFRQD}$
GND $\overline{RESET}$ $\overline{IBACK}$ $\overline{ECAS}$ $\overline{ECAS1}$ $\overline{DOACC}$ $\overline{ENDACC}$ $\overline{IREQH}$
$\overline{IRDY1}$ $\overline{AREQ1}$ VCC

If (VCC) $\overline{IBACK}$ = $\overline{AREQ}$*RFRQD*IREQH*$\overline{DTACK2}$
+ $\overline{AREQ}$*RFRQD*$\overline{IREQH}$*IREQ
+ $\overline{IBACK}$*IREQH*RFRQD

If (VCC) $\overline{ECAS}$ = $\overline{AREQ}$*ECAS1*$\overline{DOACC}$*RESET
+ $\overline{AREQ}$*$\overline{DOACC}$*$\overline{IRDY3}$*$\overline{CLK}$*RESET
+ $\overline{AREQ}$*$\overline{DOACC}$*$\overline{IRDY1}$*RESET
+ $\overline{ECAS}$*ECAS1*CLK*RESET
+ $\overline{ECAS}$*$\overline{CLK}$*RESET

If (VCC) $\overline{ECAS1}$ = $\overline{IRDY}$*$\overline{CLK}$
+ $\overline{ECAS1}$*CLK

If (VCC) $\overline{DOACC}$ = $\overline{AREQ}$*RFRQD*$\overline{IBREQ}$*RESET
+ $\overline{CS}$*$\overline{IREQ}$*IREQH*$\overline{AREQ}$*RESET
+ $\overline{DOACC}$*IRDY*RESET

If (VCC) $\overline{ENDACC}$ = $\overline{IREQ}$*$\overline{IREQH}$
+ $\overline{RFRQD}$*$\overline{IRDY}$
+ $\overline{RFRQD}$*$\overline{AREQ}$*$\overline{IREQH}$
+ $\overline{ENDACC}$*$\overline{AREQ}$
+ $\overline{RESET}$

If (VCC) $\overline{IREQH}$ = $\overline{AREQ}$*IREQ
+ $\overline{IREQH}$*$\overline{AREQ}$*RESET

If (VCC) $\overline{IRDY1}$ = $\overline{DTACK2}$*$\overline{AREQ}$*IRDY*IRDY3*IREQH
+ $\overline{AREQ}$*IRDY*IRDY3*$\overline{IREQH}$*CLK*$\overline{DOACC}$
+ $\overline{IRDY1}$*IRDY*IRDY3*$\overline{AREQ}$

If (VCC) $\overline{AREQ1}$ = $\overline{CS}$*$\overline{IREQ}$*IRDY*ENDACC*RESET
+ $\overline{AREQ1}$*ENDACC*RESET
+ $\overline{AREQ1}$*$\overline{DOACC}$*RESET

29000 PAL equations, Design #2, 1 wait state during burst accesses. Written in National Semiconductor PLAN format

PAL16L8D

CLK $\overline{CS}$ $\overline{IREQ}$ $\overline{IBREQ}$ $\overline{DTACK2}$ $\overline{AREQ}$ $\overline{IRDY}$ $\overline{IRDY3}$ $\overline{RFRQD}$
GND $\overline{RESET}$ $\overline{IBACK}$ $\overline{ECAS}$ $\overline{ECAS1}$ $\overline{DOACC}$ $\overline{ENDACC}$ $\overline{IREQH}$
$\overline{IRDY1}$ $\overline{AREQ1}$ VCC

If (VCC) $\overline{IBACK}$ = $\overline{AREQ}$*RFRQD*IREQH*$\overline{DTACK2}$
+ $\overline{AREQ}$*RFRQD*$\overline{IREQH}$*IREQ
+ $\overline{IBACK}$*IREQH*RFRQD

If (VCC) $\overline{ECAS}$ = $\overline{AREQ}$*ECAS1*$\overline{DOACC}$*RESET
+ $\overline{AREQ}$*$\overline{DOACC}$*$\overline{IRDY3}$*$\overline{CLK}$*RESET
+ $\overline{AREQ}$*$\overline{DOACC}$*$\overline{CLK}$*RESET
+ $\overline{ECAS}$*ECAS1*CLK*RESET
+ $\overline{ECAS}$*$\overline{CLK}$*RESET

If (VCC) $\overline{ECAS1}$ = $\overline{IRDY}$*$\overline{CLK}$
+ $\overline{ECAS1}$*CLK

If (VCC) $\overline{DOACC}$ = $\overline{AREQ}$*RFRQD*$\overline{IBREQ}$*RESET
+ $\overline{CS}$*$\overline{IREQ}$*IREQH*$\overline{AREQ}$*RESET
+ $\overline{DOACC}$*IRDY*RESET

If (VCC) $\overline{ENDACC}$ = $\overline{IREQ}$*$\overline{IREQH}$
+ $\overline{RFRQD}$*$\overline{IRDY}$
+ $\overline{RFRQD}$*$\overline{AREQ}$*$\overline{IREQH}$
+ $\overline{ENDACC}$*$\overline{AREQ}$
+ $\overline{RESET}$

If (VCC) $\overline{IREQH}$ = $\overline{AREQ}$*IREQ
+ $\overline{IREQH}$*$\overline{AREQ}$*RESET

If (VCC) $\overline{IRDY1}$ = $\overline{DTACK2}$*$\overline{AREQ}$*IREQH
+ $\overline{AREQ}$*IRDY*$\overline{IREQH}$*CLK*$\overline{DOACC}$
+ $\overline{IRDY1}$*IRDY*$\overline{AREQ}$

If (VCC) $\overline{AREQ1}$ = $\overline{CS}$*$\overline{IREQ}$*IRDY*ENDACC*RESET
+ $\overline{AREQ1}$*ENDACC*RESET
+ $\overline{AREQ1}$*$\overline{DOACC}$*RESET

Key: Reading PAL equations written in PLAN

EXAMPLE EQUATIONS: $\overline{READ}$: = CS__RD*ADS1D*$\overline{CLKA}$
+ $\overline{READ}$*$\overline{ADS1D}$
+ $\overline{READ}$*CLKA

This example reads: the output "$\overline{READ}$" will transition low on the next rising "CLK" clock edge (given that one of the following conditions are valid a setup time before "CLK" transitions high);

1. the input "CS__RD" is high AND the input "$\overline{ADS1D}$" is high AND the input "CLKA" is low, OR
2. the output "$\overline{READ}$" is low AND the input "$\overline{ADS1D}$" is low, OR
3. the output "$\overline{READ}$" is low AND the input "CLKA" is high

V. 29000 application note PAL and 74AS374 outputs

What follows is a brief explanation of the PAL and 74AS374 outputs:

$\overline{\text{AREQ}}$1 This combinational output of the PAL is sampled at the next rising clock edge (74AS374) to provide the $\overline{\text{ADS}}$ and $\overline{\text{AREQ}}$ outputs that drive the DP8422A DRAM accesses. This output is held low to allow burst accessing until either a new access is requested by the 29000 ($\overline{\text{IREQ}}$) or a refresh is requested ($\overline{\text{RFRQ}}$).

$\overline{\text{IRDY}}$1 This combinational output of the PAL is sampled at the next rising clock edge (74AS374) to provide the $\overline{\text{IRDY}}$ output that terminates each 29000 access.

$\overline{\text{IREQH}}$ This combinational output of the PAL is used internal to the PAL as an indication of $\overline{\text{IREQ}}$ having transitioned high. It is useful in determining when the 29000 is terminating a burst access to request an access to another page ($\overline{\text{IREQH}}$ = $\overline{\text{IREQ}}$ = low).

$\overline{\text{ENDACC}}$ This combinational output of the PAL is used internal to the PAL as an indication of when to terminate a burst, or single, access. It indicates a new page access ($\overline{\text{IREQ}}$), a refresh request ($\overline{\text{RFRQ}}$), or a hardware reset ($\overline{\text{RESET}}$) operation. Accesses are only terminated after $\overline{\text{IRDY}}$ is issued or during idle states when no accesses are pending.

$\overline{\text{DOACC}}$ This combinational output of the PAL is used internal to the PAL to keep track of requested accesses, single ($\overline{\text{IREQ}}$) or burst ($\overline{\text{IBREQ}}$ and $\overline{\text{IBACK}}$).

$\overline{\text{ECAS}}$1 This combinational output of the PAL is used internal to the PAL to allow the $\overline{\text{ECAS}}$ output to have minimum delay following the CLK high and low.

$\overline{\text{ECAS}}$ This combinational output of the PAL is used to toggle the $\overline{\text{CAS}}$ outputs of the DP8422A during burst accessing.

$\overline{\text{IBACK}}$ This combinational output of the PAL is used as an input to the 29000 to indicate when the DP8422A is available to support burst accessing. This output is pulled high during refresh requests ($\overline{\text{RFRQ}}$) and out of page accesses ($\overline{\text{IREQH}}$ = $\overline{\text{IREQ}}$ = low).

$\overline{\text{AREQ}}$ See $\overline{\text{AREQ}}$1 explanation.

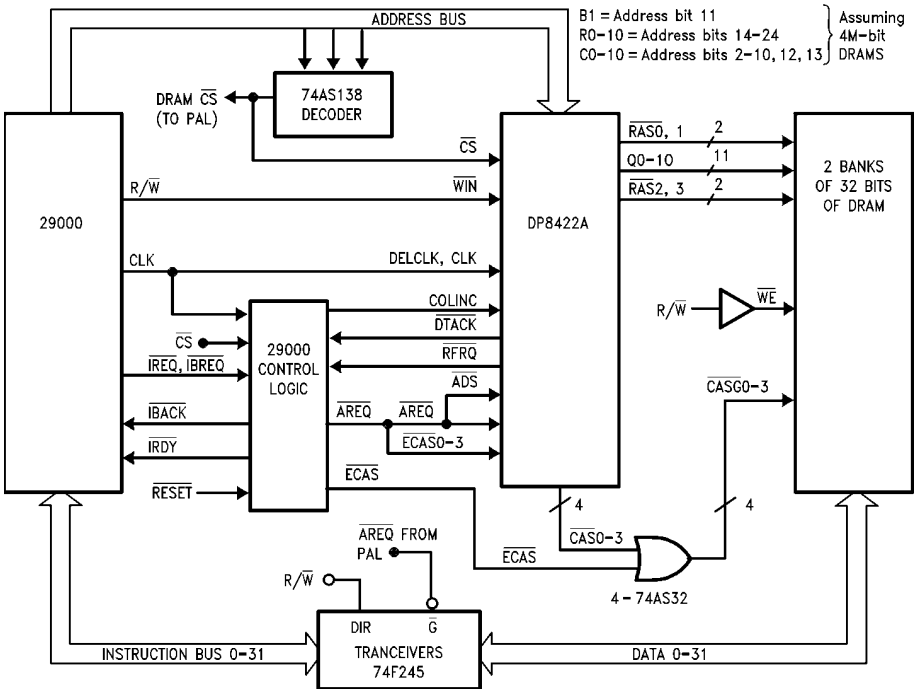
$\overline{\text{IRDY}}$ See $\overline{\text{IRDY}}$1 explanation.

$\overline{\text{IRDY}}$3 This output (74AS374) is used as a state input to the PAL. This term is $\overline{\text{IRDY}}$ delayed by one clock period.

$\overline{\text{RFRQD}}$ This clocked output is used to synchronize the DP8422A $\overline{\text{RFRQ}}$ output.

$\overline{\text{DTACK}}$2 This clocked output is generated from the DP8422A $\overline{\text{DTACK}}$1 output and is synchronized to the next rising clock edge.

Block Diagram of 29000/DP8422A Design at 25 MHz (Instruction memory interface to Port A, Port B could be used as a data memory interface to load the instructions into the DRAM)



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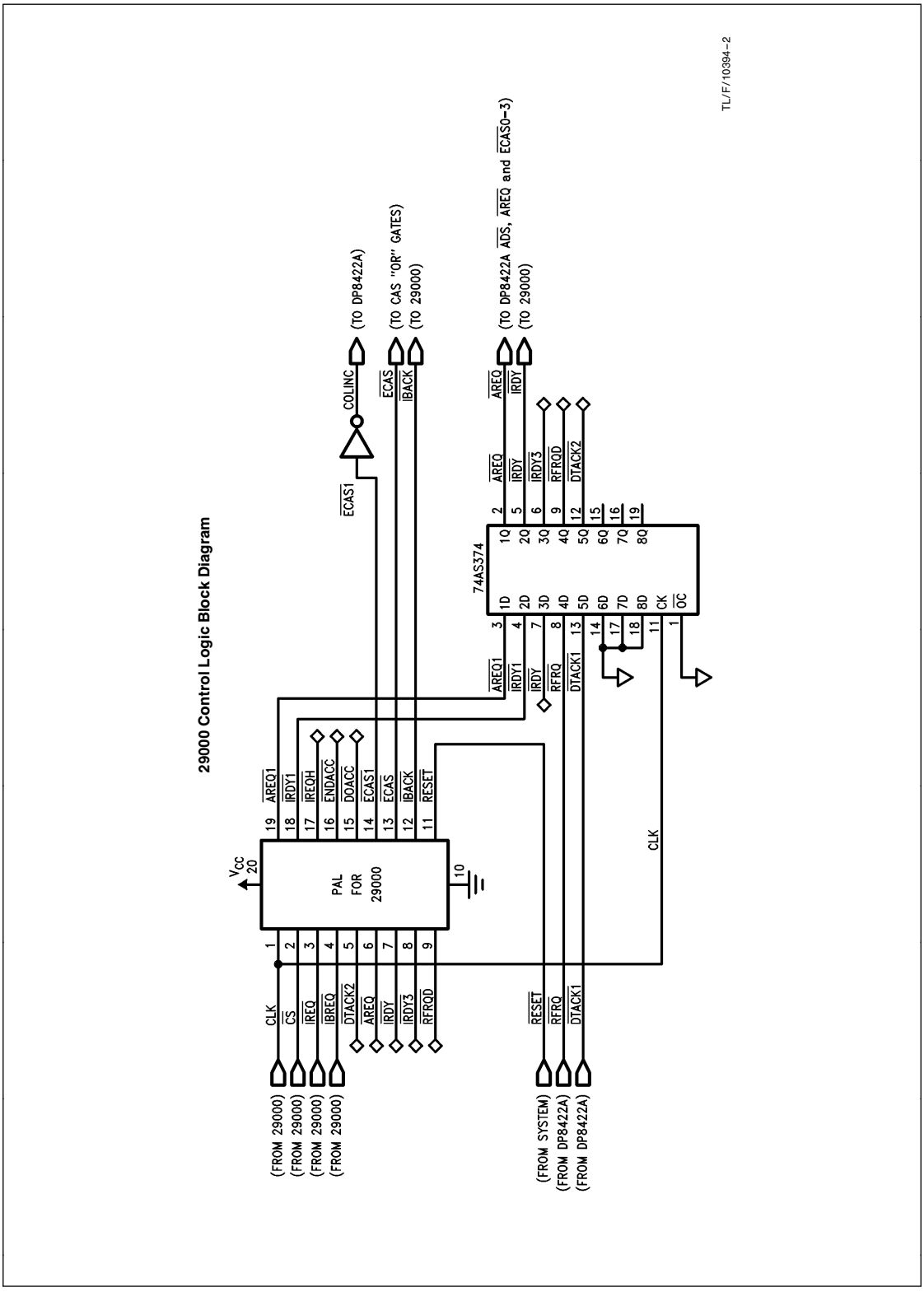
29000 Control Logic Block Diagram
PAL FOR 29000
74AS374
(FROM 29000) CLK
(FROM 29000) CS
(FROM 29000) IREQ
(FROM 29000) IBREQ
(FROM 29000) DTACK2
AREQ
IRDY
IRDY3
RFRQD
(FROM SYSTEM) RESET
(FROM DP8422A) RFRQ
(FROM DP8422A) DTACK1
AREQ1
IRDY1
IREQH
ENDACC
DOACC
ECAS1
ECAS
IBACK
RESET
CLK
COLINC
(TO DP8422A)
(TO CAS "OR" GATES)
(TO 29000)
(TO DP8422A ADS, AREQ and ECAS0–3)
(TO 29000)
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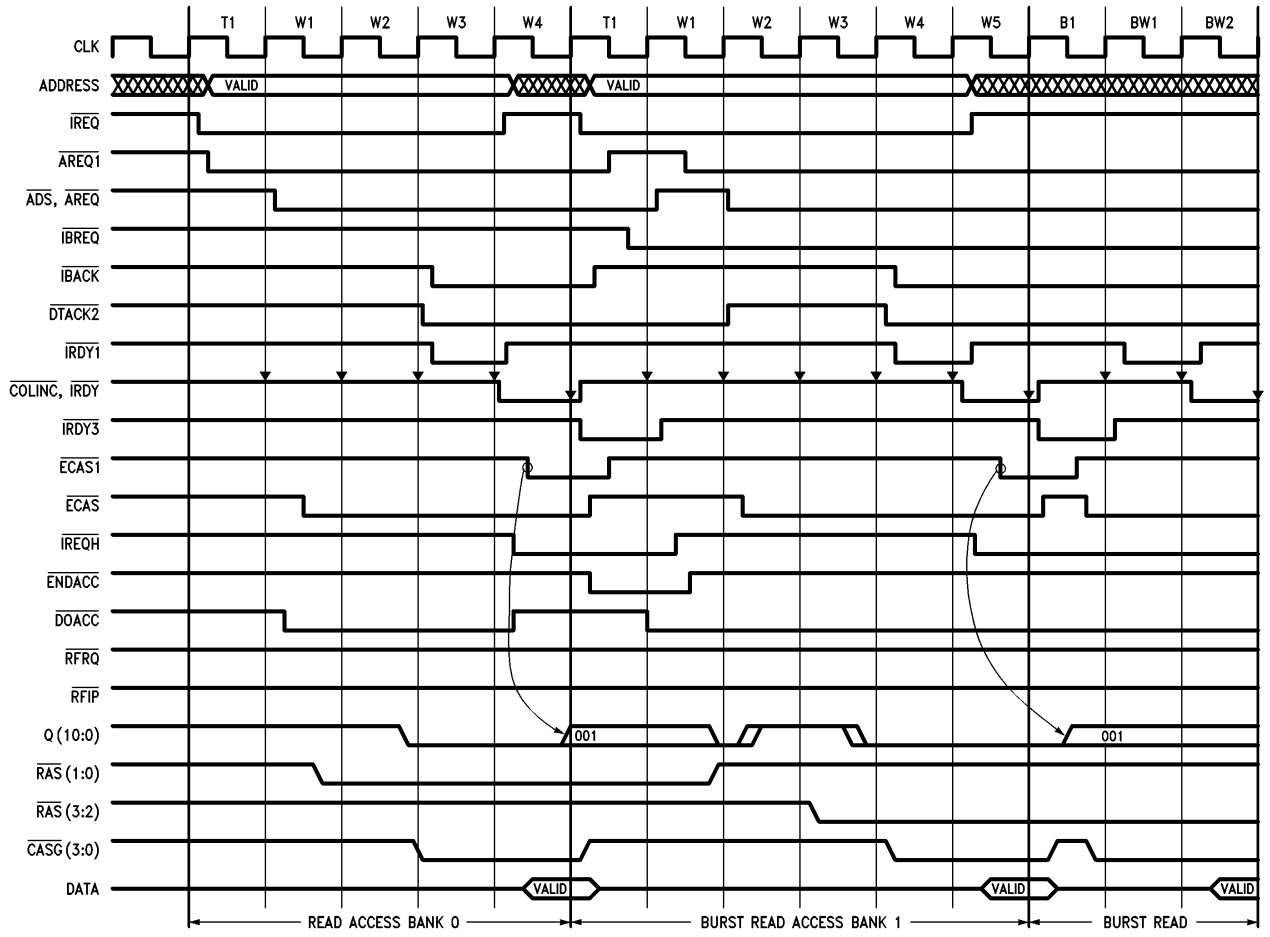
Design # 1 Timing



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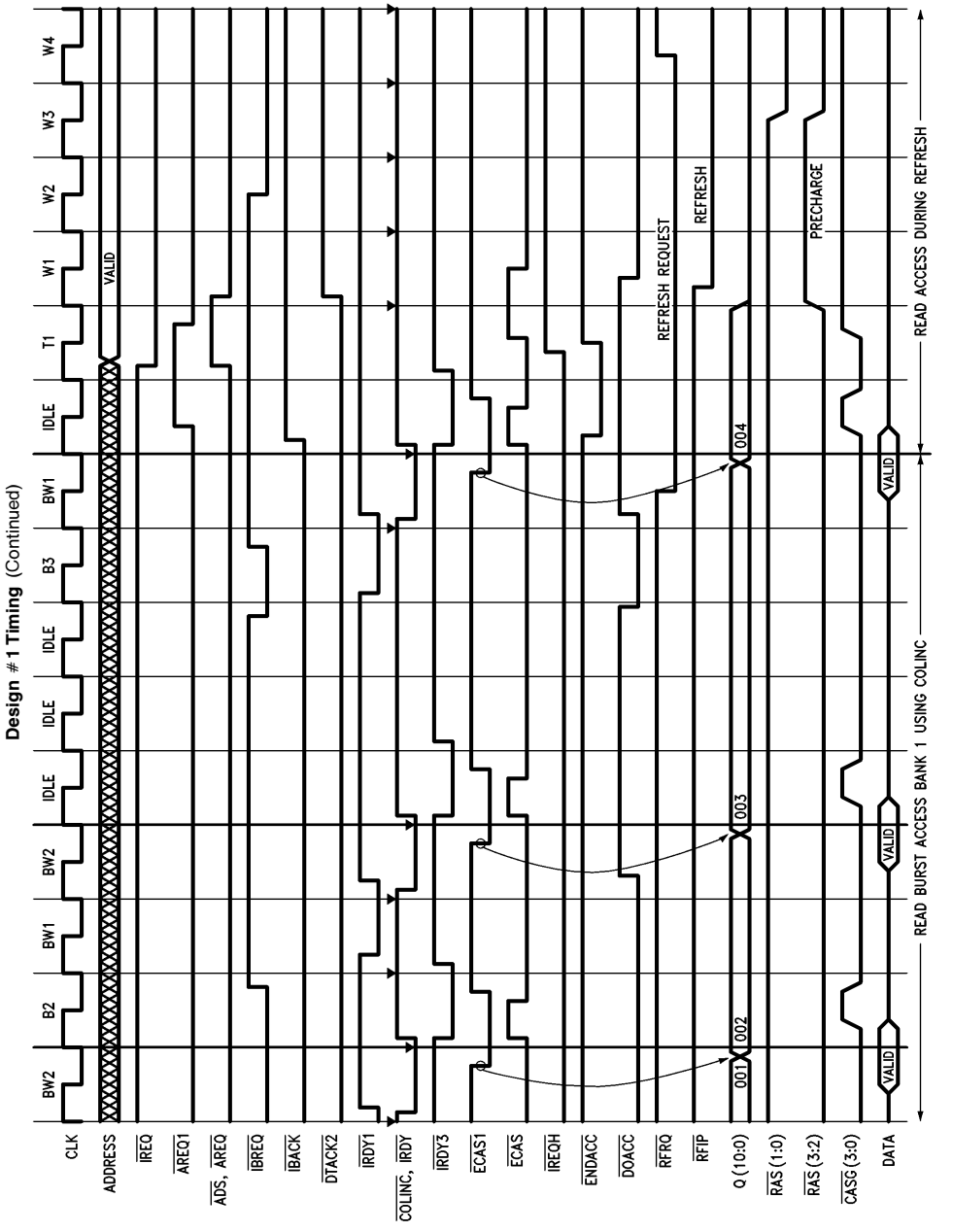
Design #1 Timing (Continued)



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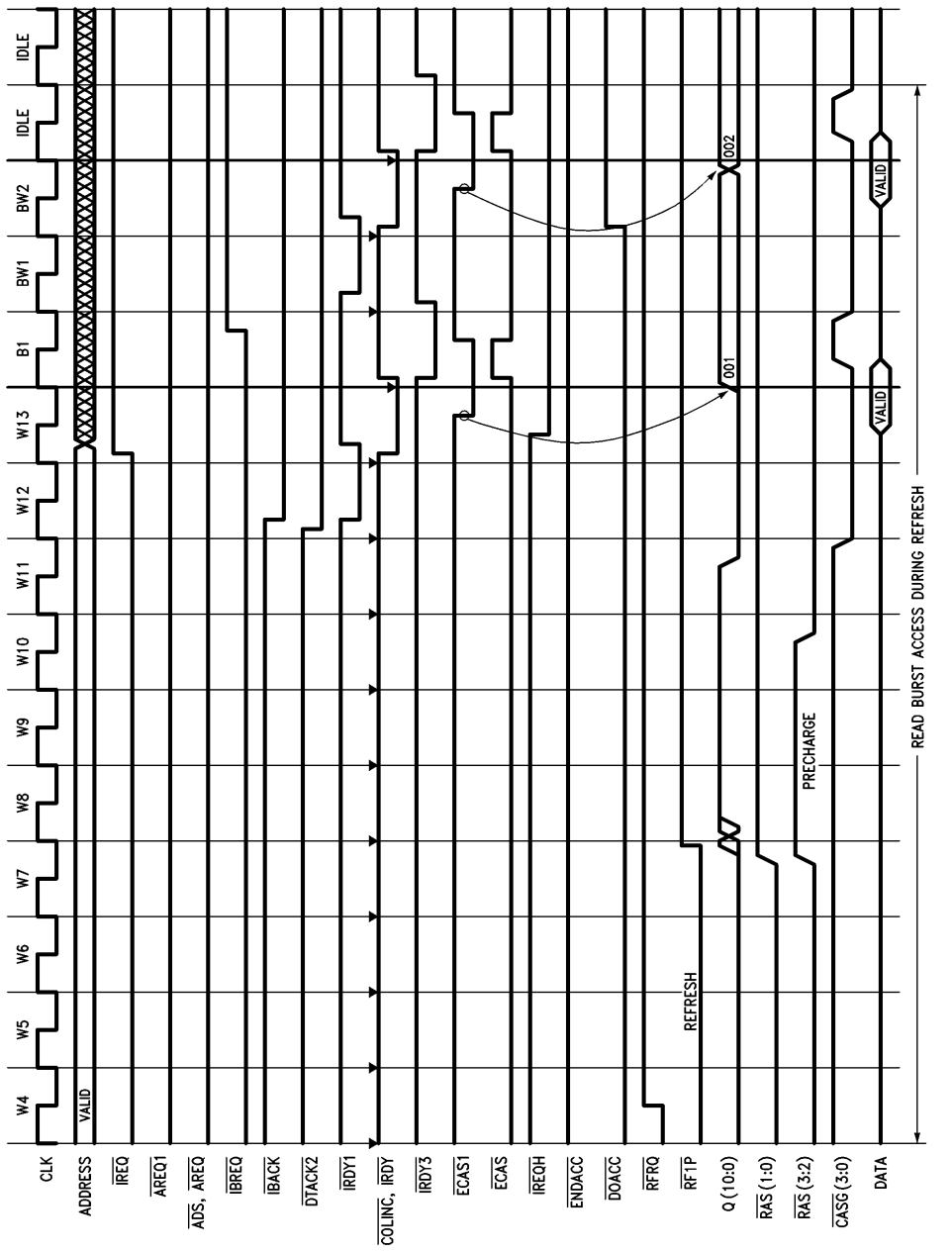
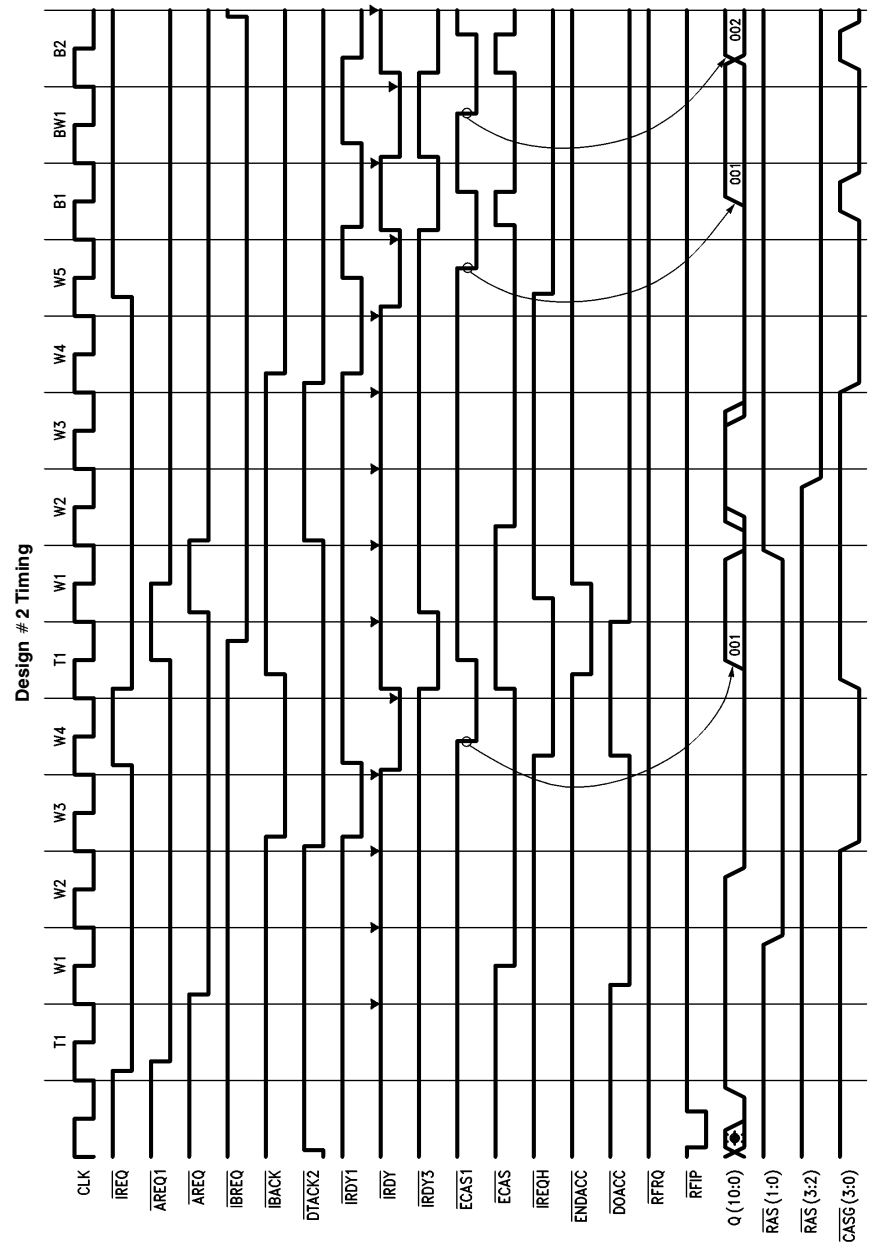
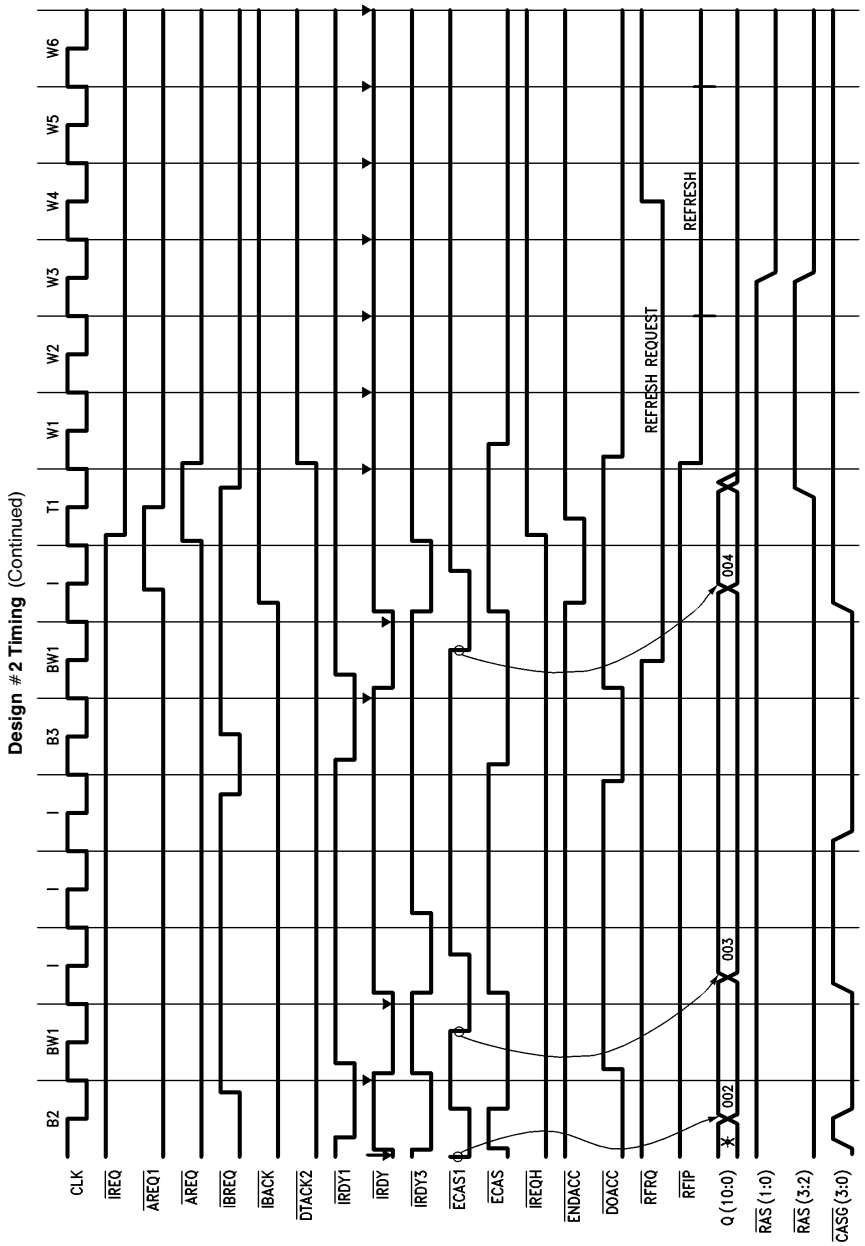
Design #1 Timing (Continued)




Design # 2 Timing
T1
W1
W2
W3
W4
T1
W1
W2
W3
W4
W5
B1
BW1
B2
CLK
IREQ
AREQ1
AREQ
IBREQ
IBACK
DTACK2
IRDY1
IRDY
IRDY3
ECAS1
ECAS
IREQH
ENDACC
DOACC
RFRQ
RFIP
Q (10:0)
RAS (1:0)
RAS (3:2)
CASG (3:0)
001
001
002
TL/F/10394–9

Design #2 Timing (Continued)



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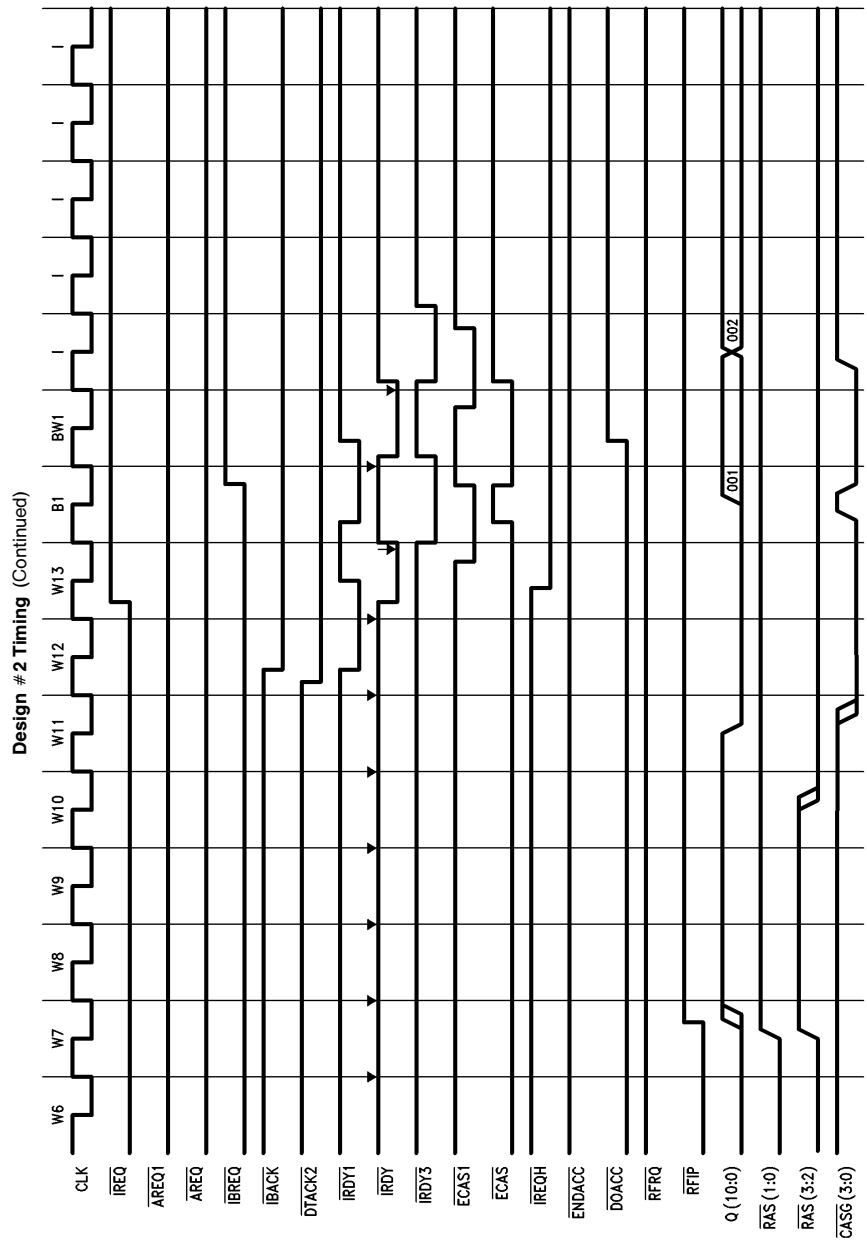
Design #2 Timing (Continued)



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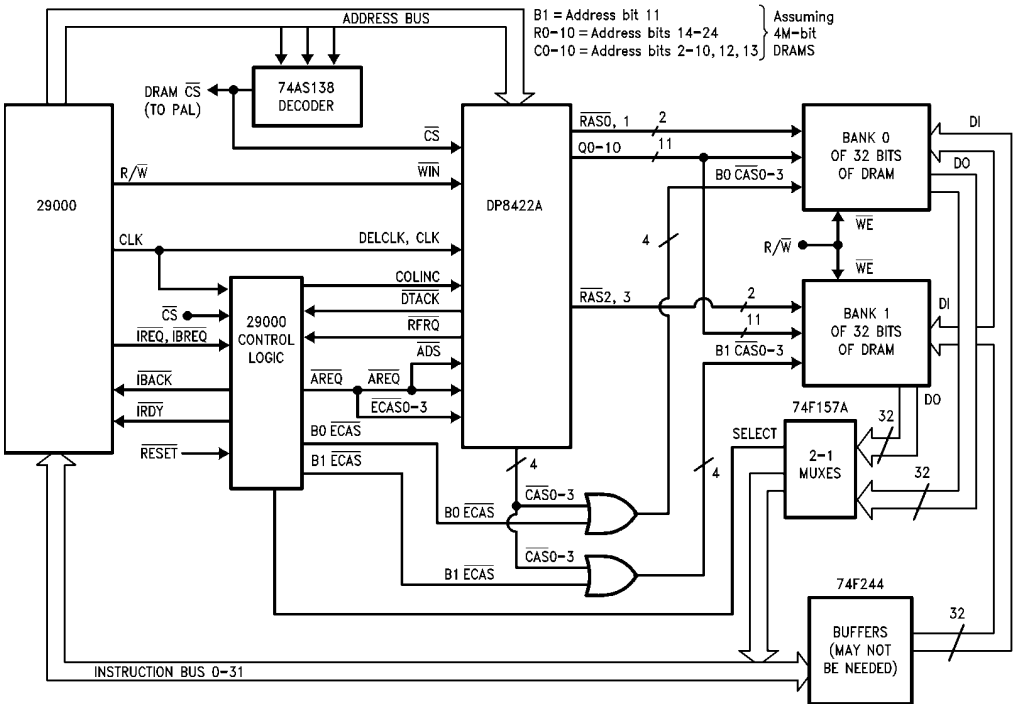
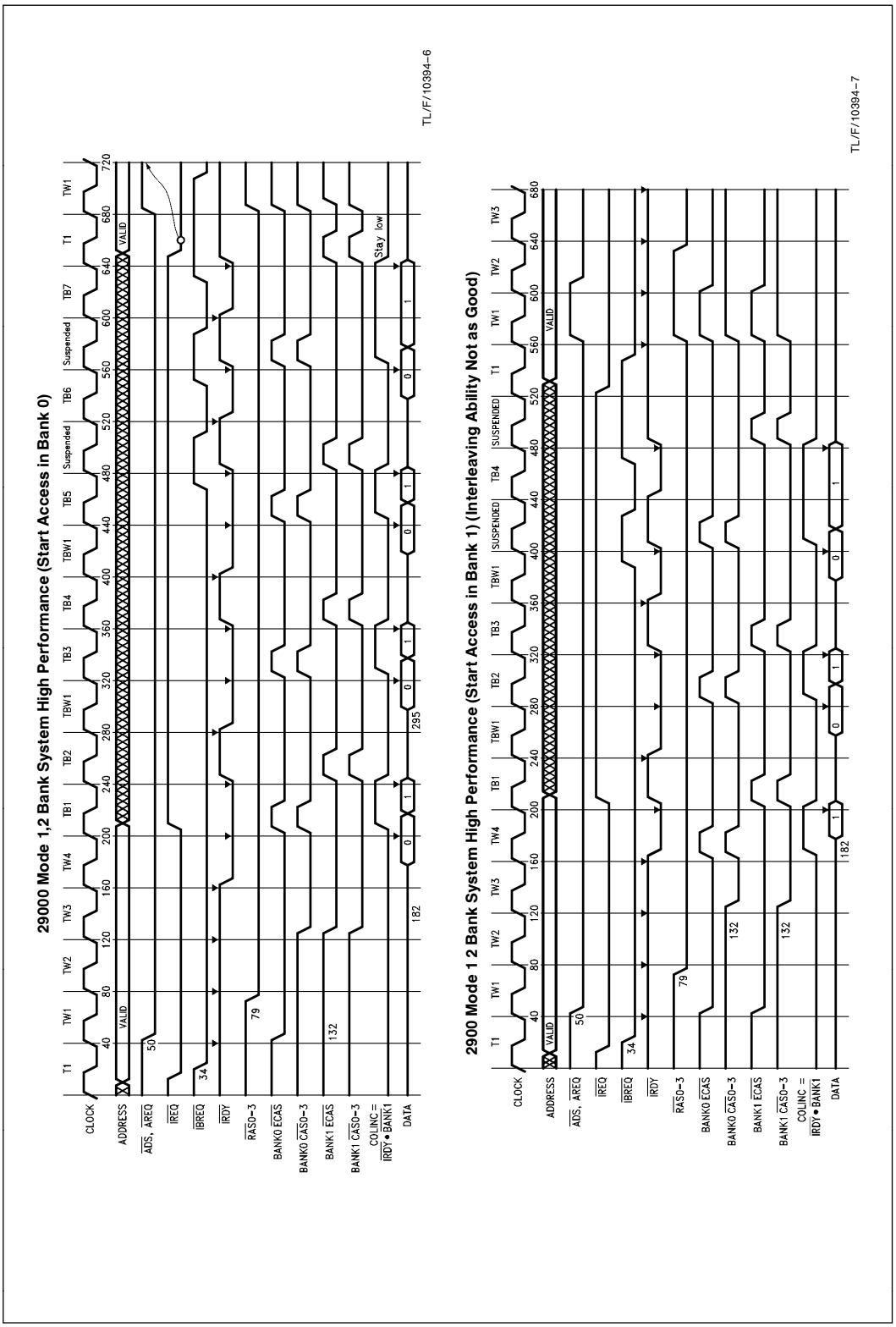
High Performance 2900 System Block Diagram Using 2 DRAM Banks, This System Could Be of Still Higher Performance by Extending it to 4 DRAM Banks




29000 Mode 1,2 Bank System High Performance (Start Access in Bank 0)
CLOCK
ADDRESS
ADS, AREQ
IREQ
IBREQ
IRDY
RAS0–3
BANK0 ECAS
BANK0 CAS0–3
BANK1 ECAS
BANK1 CAS0–3
COLINC = IRDY • BANK1
DATA
T1 TW1 TW2 TW3 TW4 TB1 TB2 TBW1 TB3 TB4 TBW1 TB5 Suspended TB6 Suspended TB7 T1 TW1
40 80 120 160 200 240 280 320 360 400 440 480 520 560 600 640 680 720
VALID
VALID
50
34
79
132
182
295
Stay low
TL/F/10394–6
2900 Mode 1 2 Bank System High Performance (Start Access in Bank 1) (Interleaving Ability Not as Good)
CLOCK
ADDRESS
ADS, AREQ
IREQ
IBREQ
IRDY
RAS0–3
BANK0 ECAS
BANK0 CAS0–3
BANK1 ECAS
BANK1 CAS0–3
COLINC = IRDY • BANK1
DATA
T1 TW1 TW2 TW3 TW4 TB1 TBW1 TB2 TB3 TBW1 SUSPENDED TB4 SUSPENDED T1 TW1 TW2 TW3
40 80 120 160 200 240 280 320 360 400 440 480 520 560 600 640 680
VALID
VALID
50
34
79
132
132
182
TL/F/10394–7

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