Interfacing the DP8422A to the 68020 (Zero Wait State Burst Mode Access)

National Semiconductor
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INTRODUCTION

This application note describes interfacing the DP8422A DRAM controller (also applicable to DP8420A/21A) to the 68020 with slower memories. This design is based upon burst mode access by holding $\overline{RAS}$ low and toggling $\overline{CAS}$. It is assumed that the user is familiar with the DP8422A and 68020 mode operations.

DESIGN DESCRIPTION

This design consists of the DP8422A DRAM controller, two PALs (16R4D and 16L8D), and a page detector (ALS6311). This design accommodates two banks of DRAM, each bank being 32 bits in width, giving maximum memory capacity of either 8 Mbytes (using 1M x 1 DRAMs) or 32 Mbytes (using 4M x 1 DRAMs). This design is based on 1M x 1 DRAM running at 16 MHz clock. The schematic diagram of interfacing DP8422A to the 68020 is shown in *Figure 1*. The DP8422A is operated in Mode 1. An access cycle begins when the 68020 places a valid address on the address bus and asserts the Address Strobe ($\overline{AS}$) if a refresh or Port B access (DP8422A only) is not in progress. The proper $\overline{RAS}$ and $\overline{CAS}$ will be asserted respectively, depending upon programming bits C6, C5, and C4 for $\overline{RAS}$ and $\overline{CAS}$ configuration after guaranteeing the programmed value of row address hold time and the column address setup time.

The High Speed Access ($\overline{HSA}$) output signal of page detector indicates whether the current access is in the same page as previous access or not. $\overline{ADS}$ ($\overline{AREQ}$) is kept low if the current access is in the page, otherwise $\overline{ADS}$ ($\overline{AREQ}$) will be forced to go high to terminate the burst access. Internal refresh logic automatically generates refresh request every 15 μs. The timing diagrams are shown in *Figure 2* and *Figure 3*.

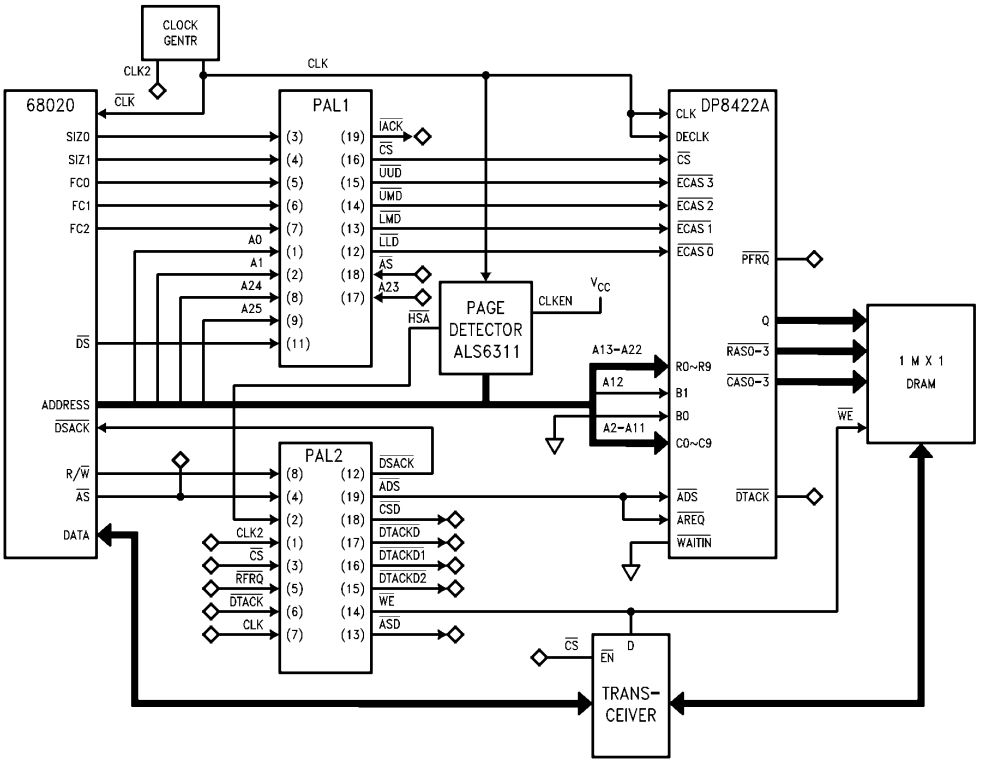

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FIGURE 1. Schematic Diagram of Interfacing DP8422A/68020 Burst Access

  RRD-B30M75/Printed in U. S. A.

DP8422A PROGRAMMING BITS

u = User Defined

Programming Bits		Description
R0, R1	= 0, 1	$\overline{RAS}$ High and Low Times
R2, R3	= 0, 0	$\overline{DTACK}$ Generation Mode for Nonburst Access
R4, R5	= 0, 0	$\overline{DTACK}$ Generation Mode for Burst Access
R6	= 0	Add Wait States if $\overline{WAITIN}$ is Low
R7	= 1	$\overline{DTACK}$ Mode Select
R8	= 1	Noninterleave Mode
R9	= u	All $\overline{RAS}$'s or Staggered Refresh Select
C0, C1, C2	= 0, 1, 0	Refresh Clock Divisor Select
C3	= 0	Refresh Clock Divider Select
C4, C5, C6	= 0, 0, 1	$\overline{RAS}$ and $\overline{CAS}$ Configuration Mode
C7	= 1	t_{ASC} Mode Select
C8	= 1	t_{RAH} Mode Select
C9	= u	Delay $\overline{CAS}$ during Write Access Mode Select
B0	= 1	Fall through Mode
B1	= 1	Mode 1 Access
$\overline{ECAS0}$	= 1	Extend $\overline{CAS}$ and Refresh Request

DESIGN TIMING PARAMETERS

Timing parameters are referenced to the numbers shown in the DP8422A data sheet timing parameters. Numbered times starting with a "$" refer to DP8422A timing parameters. Numbered times starting with a "#" refer to 68020 timing parameters.

16 MHz t_{CP} = 62.5 ns

$400: $\overline{ADS}$ Asserted Setup to CLK
½ t_{CP} − PAL t_{CLK} Max.
= 31.25 ns − 8 ns
= 23.25 ns

$401: $\overline{CS}$ Setup to $\overline{ADS}$ Asserted
2 t_{CP} + PAL t_{CLK} Min. − #6 $\overline{CLK}$ to Address Valid − PAL t_P Max.
= 125 ns + 5.5 ns − 30 ns − 10 ns
= 90.5 ns

$416: $\overline{AREQ}$ Negated to $\overline{ADS}$ Asserted
t_{CP} − (PAL t_{CLK} Max. − PAL t_{CLK} Min.)
= 62.5 ns − 2.5 ns
= 60 ns

#47: $\overline{DTACK}$ (68020) Low Setup to CLK Low
½ t_{CP} − PAL t_{CLK} Max. − PAL t_p Max.
= 31.25 ns − 8 ns − 10 ns
= 13.5 ns

t_{RAC} (Nonburst Access):
3 t_{CP} − PAL t_{CLK} Max. − PAL t_p Max. − $402 $\overline{ADS}$ Low to $\overline{RAS}$ Low − #27 Data Setup − F245 Transceiver t_p Max.
= 187.5 ns − 8 ns − 10 ns − 29 ns − 5 ns − 6 ns
= 129.5 ns (-25 Part)
= 187.5 ns − 8 ns − 10 ns − 35 ns − 5 ns − 6 ns
= 123.5 ns (-20 Part)

t_{CAC} (Nonburst Access):
3 t_{CP} − PAL t_{CLK} Max. − PAL t_p Max. − $403a $\overline{ADS}$ Low to $\overline{CAS}$ Low − #27 Data Setup − F245 Transceiver t_p Max.
= 187.5 ns − 8 ns − 10 ns − 82 ns − 5 ns − 6 ns
= 76.5 ns (-25 Part)
= 187.5 ns − 8 ns − 10 ns − 94 ns − 5 ns − 6 ns
= 64.5 ns (-20 Part)

t_{AA} (Nonburst Access):
3 t_{CP} − PAL t_{CLK} Max. − PAL t_p Max. − $417 $\overline{ADS}$ Low to Column Address Valid − #27 Data Setup − F245 Transceiver t_p Max.
= 187.5 ns − 8 ns − 10 ns − 78 ns − 5 ns − 6 ns
= 80.5 ns (-25 Part)
= 187.5 ns − 8 ns − 10 ns − 92 ns − 5 ns − 6 ns
= 66.5 ns (-20 Part)

t_{CAC} (Burst Access):
2 t_{CP} − #9 $\overline{CLK}$ High to $\overline{DS}$ Low Max. − PAL t_p Max. − $14 $\overline{ECAS}$ Low to $\overline{CAS}$ Low Max. − #27 Data Setup − F245 Transceiver t_p Max.
= 125 ns − 30 ns − 10 ns − 27 ns − 5 ns − 6 ns
= 47 ns (-25 Part)
= 125 ns − 30 ns − 10 ns − 31 ns − 5 ns − 6 ns
= 43 ns (-20 Part)

t_{AA} (Burst Access):
3.5 t_{CP} − #6 $\overline{CLK}$ Low to Address Valid Max. − $26 Address Valid to Q Max. − #27 Data Setup − F245 Transceiver t_p Max.
= 218.75 ns − 30 ns − 35 ns − 5 ns − 6 ns
= 142.75 ns (-25 Part)
= 218.75 ns − 30 ns − 38 ns − 5 ns − 6 ns
= 139.75 ns (-20 Part)

68020PAL EQUATIONS

The Boolean entry operators are listed as

":=" Replaced by (After Clock)

"=" Equality

"*" AND

"+" OR

"/" Complement

"~" Active low

The brief explanation of PAL output signals

CS~ This combinational output signal is Chip Select.

CSD~ This sequential output signal is Chip Select Delayed by one clock.

ADS~ This sequential output signal is Address Strobe (also used as an Access Request, /AREQ, to DP8422A).

DTACKD~ This sequential output signal is Data Transfer Delayed by one clock.

DTACKD1~ This sequential output signal is Data Transfer Delayed by two clocks.

DTACKD2~ This sequential output signal is Data Transfer Delayed by three clocks.

WE~ This sequential output signal is Write Enable to DRAM.

DSACK~ This combinational output signal is Data Transfer and Size Acknowledge.

UUD~ This combinational output signal is to select upper upper byte.

UMD~ This combinational output signal is to select upper middle byte.

LMD~ This combinational output signal is to select lower middle byte.

LLD~ This combinational output signal is to select lower lower byte.

IACK~ This combinational output signal is interrupt acknowledge.

(I) PAL1 (PAL16L8D) EQUATIONS

Inputs: A0, A1, A23, A24, A25, FC2, FC1, FC0, SIZ0, SIZ1, DS~, AS~

Outputs:

/IACK~ = /FC2 + /FC1 + /FC0

/CS~ = /A23 * /A24 * /A25 * /FC2 * /FC1 * FC0 + /A23 * /A24 * /A25 * /FC2 * FC1 * /FC0 + /A23 * /A24 * /A25 * FC2 * /FC1 * FC0 + /A23 * /A24 * /A25 * FC2 * FC1 * /FC0

/UUD~ = /A0 * /A1 * /DS~ * /AS~

/UMD~ = /SIZ0 * /A1 * /DS~ * /AS~ + A0 * /A1 * /DS~ * /AS~ + SIZ1 * /A1 * /DS~ * /AS~

/LMD~ = /A0 * /A1 * /DS~ * /AS~ + /A1 * /SIZ0 * /SIZ1 * /DS~ * /AS~ + SIZ1 * SIZ0 /A1 * /DS~ * /AS~ + /SIZ0 * /A1 * A0 * /DS~ * /AS~

/LLD~ = A0 * SIZ0 * SIZ1 * /DS~ * /AS~ + /SIZ0 * /SIZ1 * /DS~ * /AS~ + A0 * A1 * /DS~ * /AS~ + A1 * SIZ1 * /DS~ * /AS~

(II) PAL2 (PAL16R6D) EQUATIONS

Inputs: CLK2, CS~, HSA~, AS~, RFRQ~, DTACK~, CLK, RW~

/ADS~ = /HSA~ * /ASD~

/DSACK~ = /DTACK~ * /DTACKD~

/DTACKD~ := /DTACK~ * /CLK + /DTACKD~ * CLK

/DTACKD1~ := /DTACKD~ * /CLK + /DTACKD1~ * CLK

/DTACKD2~ := /DTACKD1~ * /CLK + /DTACKD2~ * CLK

/ASD~ := /CSD~ * CLK /AS~ + /CSD~ * /HSA~ * /AS~ + /CSD~ * /RFRQ~ * /AS~ + /RFRQ~ * CSD~ * /AS~ + /RFRQ~ * CLK * /AS~ + /RFRQ~ * /HSA~ * /AS~ + /CSD~ * CLK * RFRQ~ + /CSD~ * /HSA~ * RFRQ~

/WE~ := /RW~ * AS~ * CLK + /WE~ * /CLK

/CSD~ := /CS~ * /CLK + /CSD~ * CLK

Note: PAL1 address inputs, such as A23, A24 and A25, are system memory size dependent.

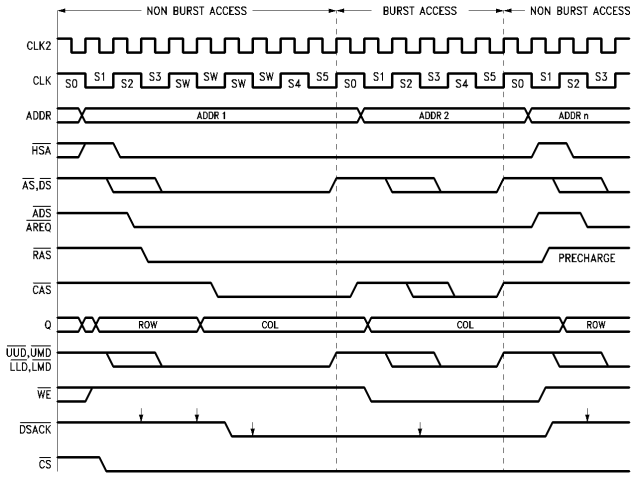

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FIGURE 2. Timing Diagram of Burst and Nonburst Access

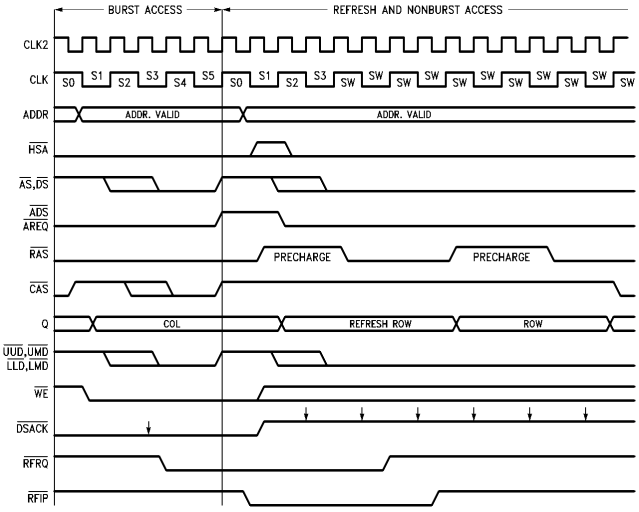

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FIGURE 3. Timing Diagram of Refresh, Burst and Nonburst Access.

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