Generating a Custom-Ready Signal Using the NS32GX32 Evaluation Board

National Semiconductor
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1.0 INTRODUCTION

The NS32GX32 Evaluation Board (EB) has a jumper option that allows the selection of a single wait state or generation of any number of wait states for the $\overline{\text{USER0}}$ address space of 800000–BFFFFF. This application note describes each option and gives an example for the custom-ready option.

2.0 JUMPER DESCRIPTIONS

Jumper W2.3 is provided to select either $\overline{\text{USER0}}$ or $\overline{\text{CRDY}}$ (Custom-Ready) to control $\overline{\text{RDY}}$, the NS32GX32's ready input signal. A portion of the NS32GX32 EB's ready circuit is shown in *Figure 1*.

If $\overline{\text{USER0}}$ is selected to control the NS32GX32's $\overline{\text{RDY}}$ signal, then one wait state will be inserted into each read or write cycle. If $\overline{\text{CRDY}}$ is selected to control $\overline{\text{RDY}}$, then additional logic is needed to generate the desired number of wait states. If neither $\overline{\text{USER0}}$ or $\overline{\text{CRDY}}$ is selected, then $\overline{\text{IORDY}}$ will be used to control $\overline{\text{RDY}}$ and 13 wait states will be inserted into all I/O accesses. $\overline{\text{IORDY}}$ is intended for the slow I/O devices (such as ROMs, UARTs, etc.) within the NS32GX32 EB itself.

Another jumper option (W4.6) enables the transceivers of the user data bus (DO0–DO31). If the W2.3 ready jumper option is set to either $\overline{\text{USER0}}$ or $\overline{\text{CRDY}}$, then a jumper must be installed in W4.6. This option provides a fast access signal, $\overline{\text{FSTAC}}$, which puts the transceivers into the transparent mode for fast I/O accesses. If a jumper is not installed in W4.6, then the transceivers will be controlled by the $\overline{\text{ROM}}$ chip select.

Two other jumpers are shown in *Figure 1*. Jumper W2.1 removes all wait states for high speed static RAM accesses. Jumper W2.2 selects between normal (real-time) or single-step operation.

3.0 USING $\overline{\text{USER0}}$

Figure 2 shows the worst-case timing at 30 MHz with $\overline{\text{USER0}}$ selected. The CONF signal is used to clear the J-K flip-flop in state T1 of the bus cycle and to initialize the $\overline{\text{RDY}}$ input signal to the ready state. The J input is high for I/O accesses and the K input is valid at least 6.8 ns before the falling edge of $\overline{\text{CLK1}}$. Therefore, the Q output will toggle with both J and K at logic state 1 and $\overline{\text{RDY}}$ will switch to the not ready state. A single wait state will be inserted into the cycle since $\overline{\text{RDY}}$ will be set up for at least 19 ns before the rising edge of state T2W.

The $\overline{\text{RDY}}$ signal will then become active or back to the ready state after the next falling edge of $\overline{\text{CLK1}}$ since the J-K flip-flop will toggle again. The bus cycle will then be completed, since $\overline{\text{RDY}}$ will be sampled active on the rising edge of state T1.

4.0 USING CUSTOM-READY ($\overline{\text{CRDY}}$)

If custom-ready ($\overline{\text{CRDY}}$) is selected to control the microprocessor's $\overline{\text{RDY}}$ signal, then the user can generate the number of wait states required for a particular application. An example of a custom-ready circuit is shown in *Figure 3*.

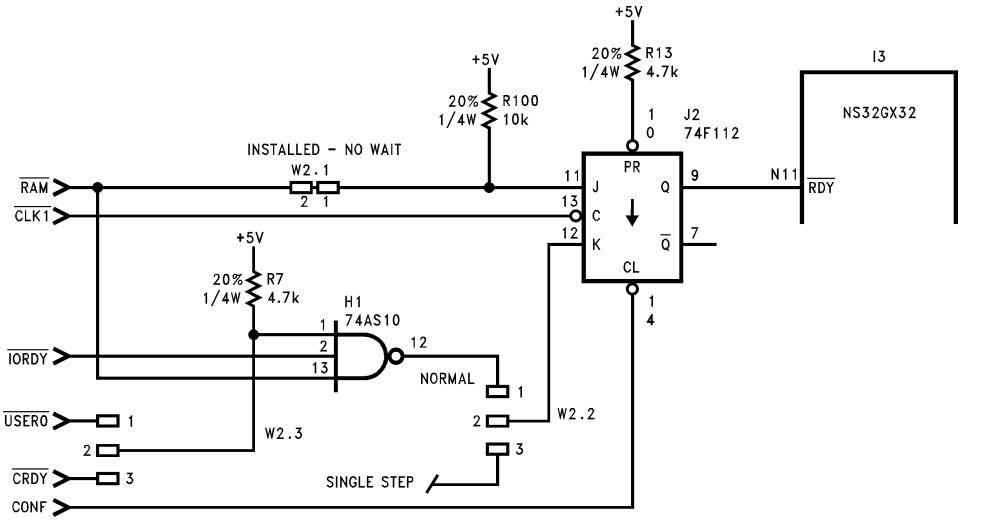

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FIGURE 1. NS32GX32 Evaluation Board Ready Circuit

RRD-B30M75/Printed in U. S. A.

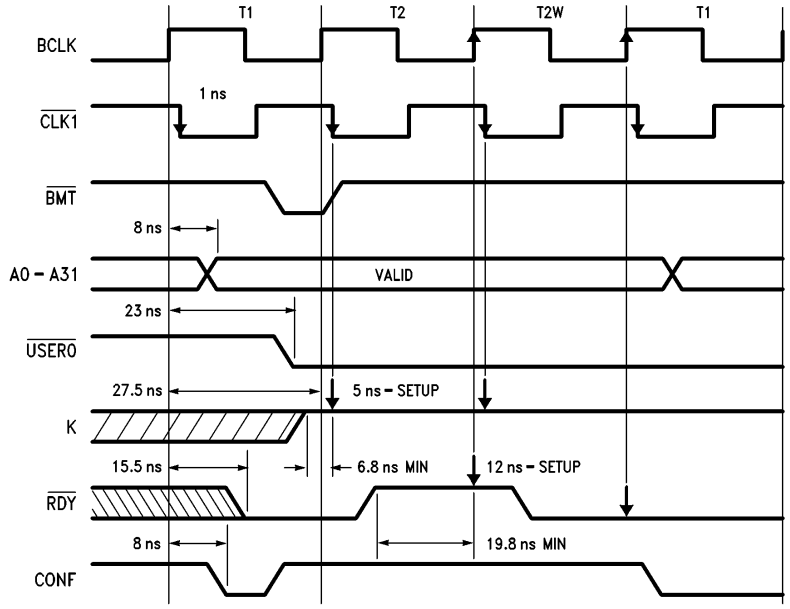

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FIGURE 2. Worst-Case Timing at 30 MHz with $\overline{\text{USER0}}$

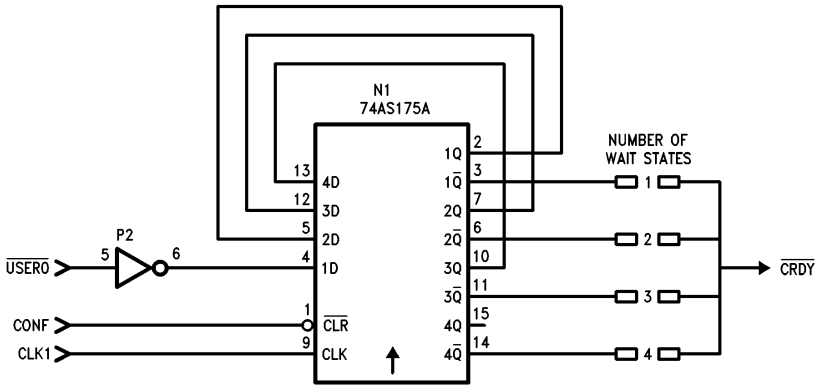

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FIGURE 3. A Custom-Ready Circuit

In this example, a single 74AS175A quad D flip-flop package and an inverter for the designer kit's $\overline{\text{USER0}}$ signal provides four wait state options. One to four wait states can be inserted into each I/O bus cycle for the $\overline{\text{USER0}}$ address space by installing the appropriate jumper for the $\overline{\text{CRDY}}$ signal. *Figure 4* shows the worst-case timing at 30 MHz with $\overline{\text{CRDY}}$ selected.

The timing diagrams show maximum propagation delays and minimum setup time requirements. At the beginning of a new bus cycle (state T1), the confirm bus cycle signal ($\overline{\text{CONF}}$) initializes the custom ready to the ''not ready'' state ($\overline{\text{CRDY}} = 1$), and the microprocessor's ready signal to the ready state ($\overline{\text{RDY}} = 0$).

In state T2, since the setup requirement of at least 5 ns is satisfied by the K input, the microprocessor's ready signal will switch to the ''not ready'' state ($\overline{\text{RDY}} = 1$).

A T2 wait state (T2W state) will be inserted into the bus cycle since the setup requirement of at least 12 ns will be satisfied by the $\overline{\text{RDY}}$ input. Depending on which jumper is installed, either another T2W state will be inserted, or the cycle will end since the K input will switch to the high state, forcing the Q output of the J-K flip-flop to toggle the ready input back to the ready state ($\overline{\text{RDY}} = 0$).

CLK1 is a delayed bus clock signal (BCLK), used to trigger each stage of the 74AS175A quad D flip-flop package on its rising edge. $\overline{\text{USER0}}$ is a chip select and is used as the source for the custom-ready logic. The $\overline{\text{CONF}}$ signal is extended along with the bus cycle and clears all flip-flops simultaneously at the end of the complete cycle.

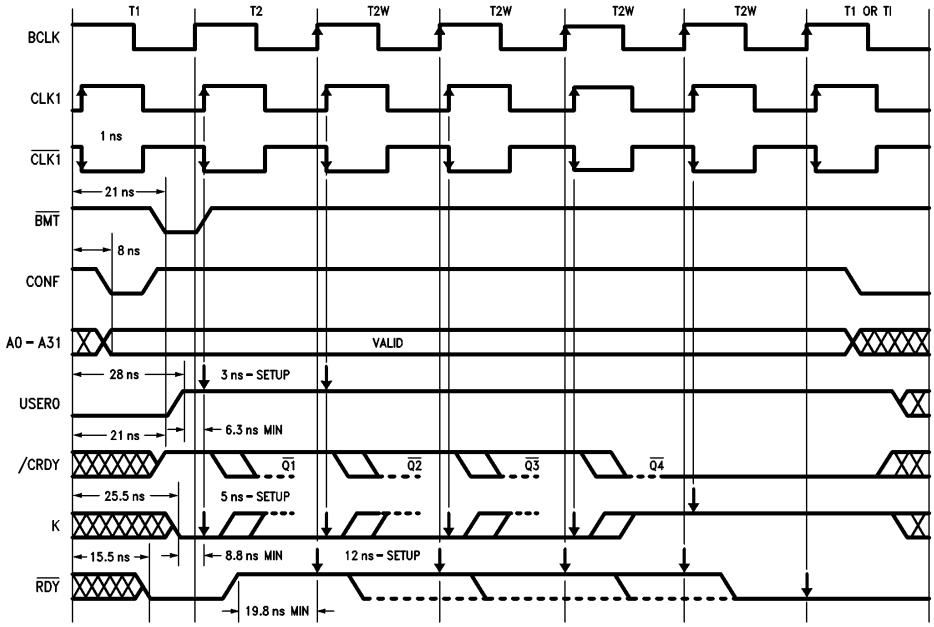

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FIGURE 4. Worst-Case Timing at 30 MHz with $\overline{\text{CRDY}}$

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998