Interfacing the NS32381 as a Floating-Point Peripheral

National Semiconductor
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This note is a guide for users who wish to interface the NS32381 Floating-Point Unit (FPU) as a peripheral unit to CPUs other than those of the Series 32000 family. This is not a particularly expensive procedure, but it requires some in-depth information not all of which is available in the NS32381 data sheet. Three basic topics covered here are:

1. An overview of the architecture of the NS32381 as seen in a stand-alone environment.
2. The protocols used to sequence it through the execution of an instruction.
3. Special guidelines for connecting and working with the NS32381 as a peripheral component.

References are made here to the NS32381 data sheet and the Series 32000 Programmer's Reference Manual. The reader should have both of these documents on hand.

1.0 Architecture Overview

1.1 REGISTER SET

The register set internal to the NS32381 FPU is shown in *Figure 1*.

1.1.1 Floating-Point Registers

There are eight registers (L0–L7) on the NS32381 FPU for providing high-speed access to floating-point operands. Each is 64 bits long. A floating-point register is referenced whenever a floating-point instruction uses the Register addressing mode for a floating-point operand. All other Register mode usages (i.e., integer operands) refer to the General Purpose Registers (R0–R7) of the CPU, and the FPU transfers the operand as if it were in memory.

Note: These registers are all upward compatible with the 32-bit NS32081 registers, (F0–F7), such that when the Register addressing mode is specified for a double precision (64-bit) operand, a pair of 32-bit registers hold the operand. The programmer specifies the even register of the pair which contains the least significant half of the operand and the next consecutive register contains the most significant half.

1.1.2 Floating-Point Status Register (FSR)

The Floating-Point Status Register (FSR) selects operating modes and records any exceptional conditions encountered during execution of a floating-point operation. The FSR is loaded by executing the LFSR instruction and is examined using the SFSR instruction.

1.2 INSTRUCTION SET AND ENCODING

The encodings used for NS32381 instructions are shown in *Figure 2*. They fall within three formats, labeled from Series 32000 tradition ''Format 9'', ''Format 11'' and ''Format 12''. These formats are distinguished by their least-significant byte (the ''ID Byte''). Execution of an FPU instruction starts by passing first the ID Byte and then the rest of the instruction (the ''Operation Word'') to the FPU.

Fields within an instruction are interpreted by the FPU in the same manner as documented in Chapter 4 of the Series 32000 Programmer's Reference Manual, with the exception of the 5-bit General Addressing Mode fields (*gen1, gen2*). Since the FPU does not itself perform memory accesses, it does not need to use these fields for addressing calculations. The only use it makes of these fields is to determine for each operand whether the value is to be found internal to the FPU (that is, within a register L0–L7, or whether it is to be transferred to and/or from the FPU. See *Figure 3*. A value of 0–7 in a *gen* field specifies one of the Floating-Point registers, L0–L7, respectively, as the location of the corresponding operand. Any greater value specifies that the operand's location is external to the FPU and that its value will be transferred as part of the protocol. Any non-floating operand is always handled by the FPU as external, regardless of the addressing mode specified in its *gen* field.

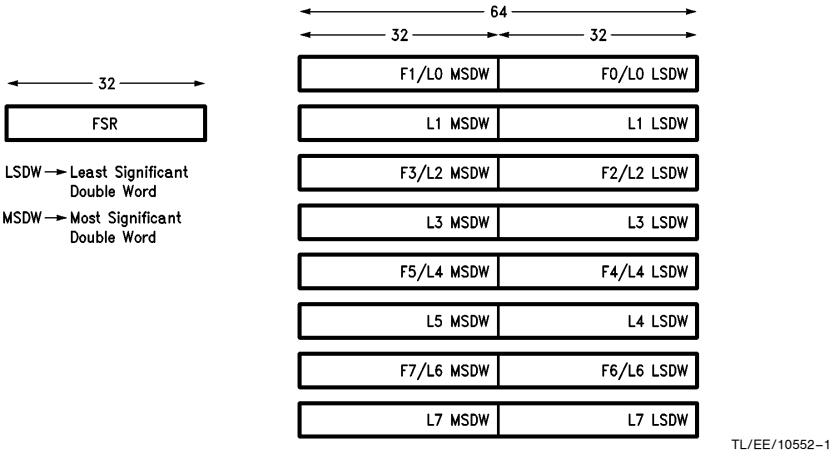

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FIGURE 1. FPU Registers

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1.3 PINOUT

The FPU is packaged in a 68-pin PGA (see *Figure 4*) or a 68-pin plastic package.

The pin functions are as follows:

Supplies

V_{CC} Power: +5V positive supply.

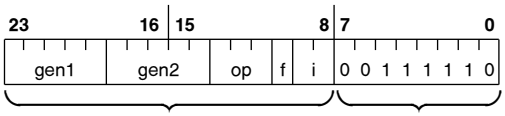
GND Ground: Ground reference for both on-chip logic and drivers connected to output pins.

Input Signals

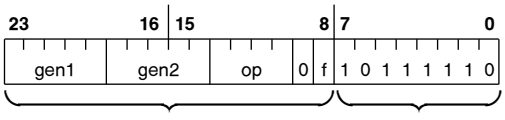
CLK Clock: TTL-level clock signal.

*$\overline{DDIN}$ Data Direction In: Active low. Status signal indicating the direction of data transfers during a bus cycle.

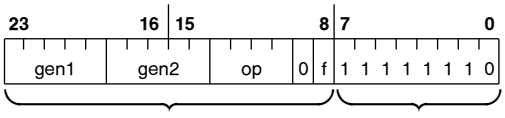
ST0–ST3 The status code. This 4-bit value is sampled by the FPU on the falling edge of $\overline{SPC}$, and informs it of the current protocol phase. ST0 is the least-significant bit of the value. The need filled by the status code is most relevant to Series 32000-based systems, where it serves to allow retry of aborted instructions and to disambiguate the protocol when the $\overline{SPC}$ signal is bussed among multiple slave processors. In microprocessor-based peripheral applications, the status code can generally be provided from the CPU's address lines.



Format 9: LFSR/SFSR/Conversions



Format 11: Movement/Calculation



Format 12: SCALB/LOGB/DOT/POLY

FIGURE 2. FPU Instruction Formats

$\overline{RST}$ Reset: Active low. Resets the last operation and clears the FSR register.

NOE New Opcode Enable: Active high. This signal enables the new opcodes available in the NS32381.

PS0, PS1 Protocol Select: Selects the slave protocol to be used. PS0 is the least significant and rightmost bit.

- 00—Selects 16-bit protocol.
- 01—Selects 32-bit protocol for NS32332.
- 10—Reserved.
- 11—Selects 32-bit protocol for NS32532.

Output Signals

$\overline{SDN332}$ Slave Done 332: Active low. This signal is for use with the NS32332 CPU only. If held active for a half clock cycle and released this pin indicates the successful completion by the FPU of a floating-point instruction. Holding this pin active for two and a half clock cycles indicates TRAP or that the CMPf instruction has been executed.

$\overline{SDN532}$ Slave Done 532: Active low. This signal is for use with the NS32532 CPU only. When active it indicates successful completion by the FPU of a floating-point instruction.

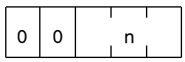
$\overline{FSSR}$ Force Slave Status Read: Active low. This signal is for use with the NS32532 CPU only. When active it indicates TRAP or that the CMPf instruction has been executed.

Input/Output Signals

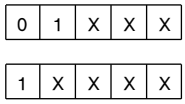
*D0–D31 The 32-bit data bus. The D0 pin holds the least-significant bit of data transferred on the bus.

$\overline{SPC}$ Slave Processor Control; Active Low. This is the data strobe signal for slave transfers. For the 32-bit protocol $\overline{SPC}$ is only an input while for the 16-bit protocol it is a dual purpose pin. It is pulsed low by the FPU to signal that it has completed the internal execution phase of an instruction.

*For the 16-bit Slave Protocol the upper sixteen data input signals (D16–D31 and $\overline{DDIN}$) should be left floating.



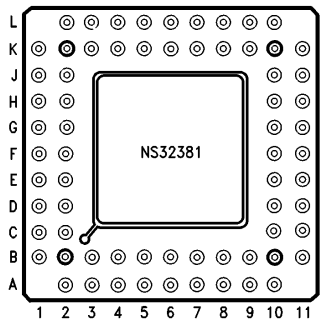
FPU Internal Register: Ln, n = 0 . . . 7



External to FPU

Note: All non-floating operands are always external.

FIGURE 3. FPU Addressing Modes



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Bottom View

Desc	Pin
V_{CC}	A2
D1	A3
D0	A4
PS1 (Note 1)	A5
GND	A6
GND	A7
CLK	A8
$\overline{RST}$	A9
Reserved (Note 2)	A10
Reserved (Note 2)	B1
D2	B2
D17	B3
D16	B4
PS0 (Note 1)	B5
GND	B6
NOE (Note 1)	B7
Reserved (Note 3)	B8
Reserved (Note 2)	B9
V_{CC}	B10
D15	B11
D18	C1
D3	C2
D31	C10
D14	C11
D19	D1
V_{CC}	D2
D30	D10
V_{CC}	D11
D4	E1
D20	E2
D13	E10
D29	E11
Reserved (Note 3)	F1
D5	F2

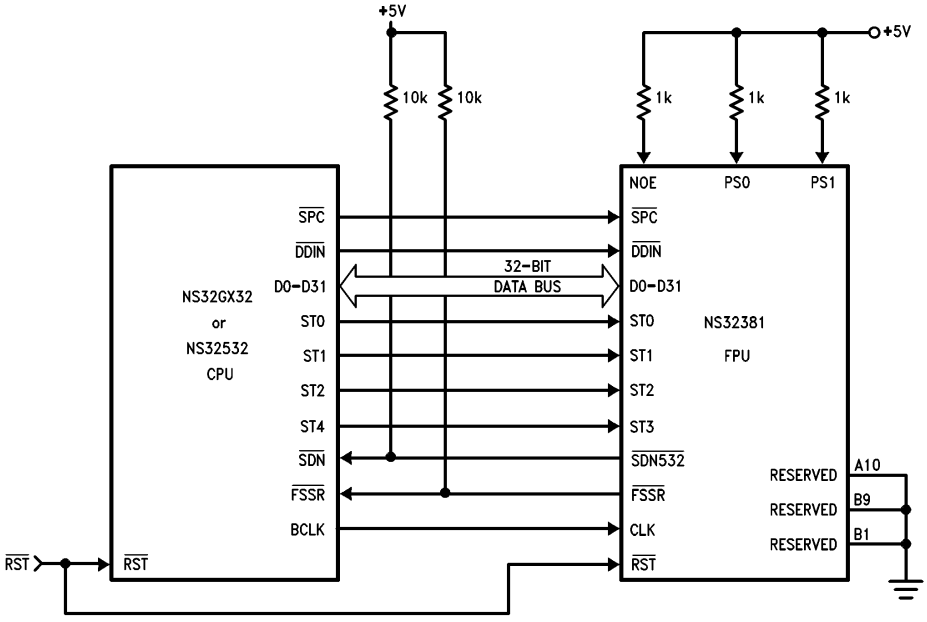
Desc	Pin
D28	F10
GND	F11
GND	G1
D21	G2
D12	G10
D27	G11
D6	H1
D22	H2
D11	H10
$\overline{SDN332}$	H11
D7	J1
D23	J2
$\overline{SPC}$	J10
$\overline{SDN532}$	J11
V_{CC}	K1
D8	K2
GND	K3
D26	K4
GND	K5
V_{CC}	K6
Reserved (Note 3)	K7
ST0	K8
ST1	K9
Reserved (Note 3)	K10
GND	K11
D24	L2
D25	L3
D9	L4
D10	L5
$\overline{DDIN}$	L6
V_{CC}	L7
ST2	L8
ST3	L9
$\overline{FSSR}$	L10

Note 1: CMOS input; never float.

Note 2: Pin should be grounded.

Note 3: Pin should be left floating.

FIGURE 4. NS32381 FPU PGA Pin Descriptions



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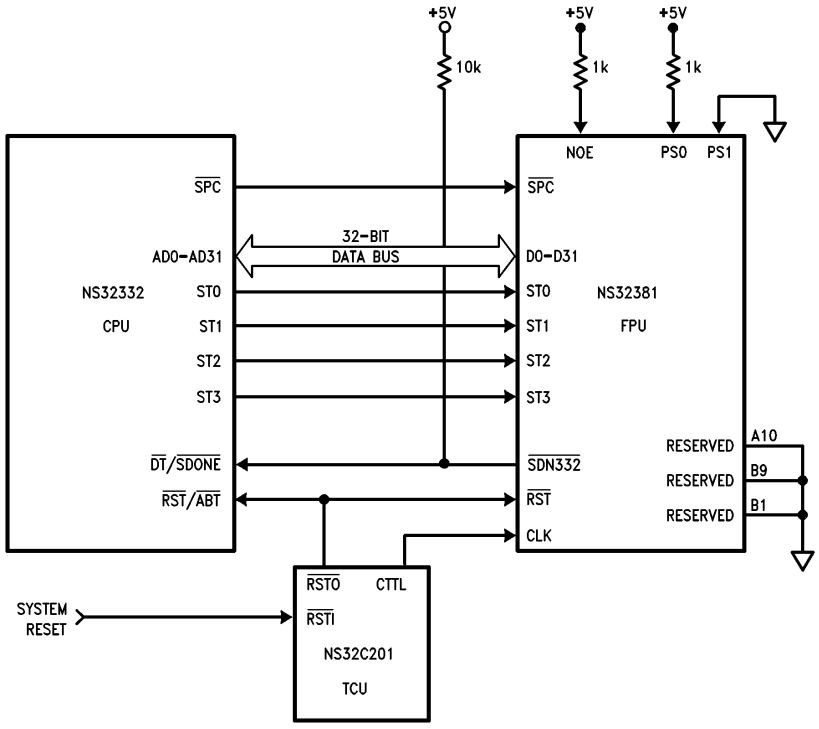
a. System Connection Diagram with the NS32532 or NS32GX32 CPU



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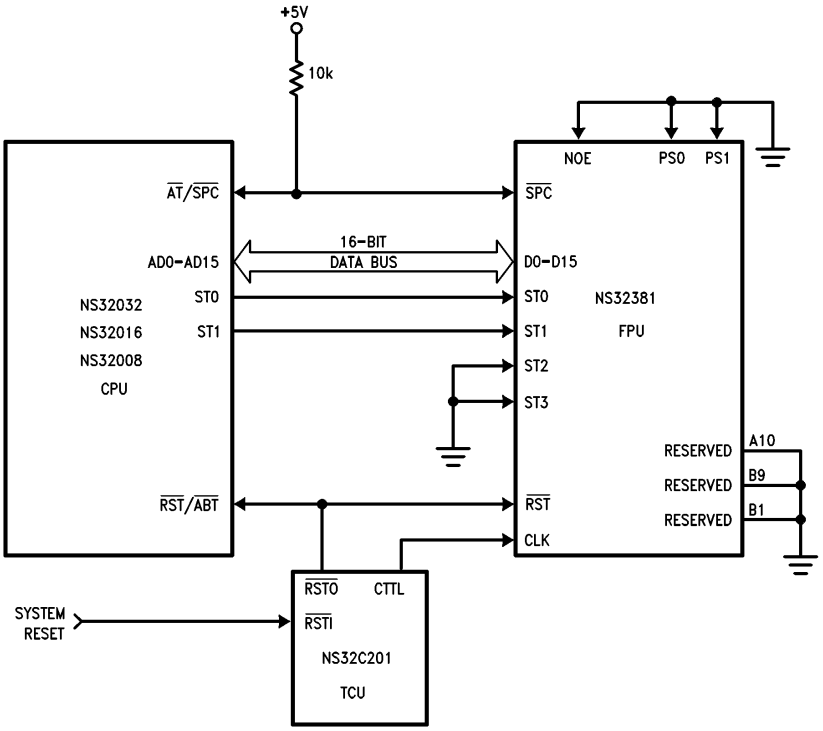
b. System Connection Diagram with the NS32332 CPU

FIGURE 5. NS32381 FPU Connections



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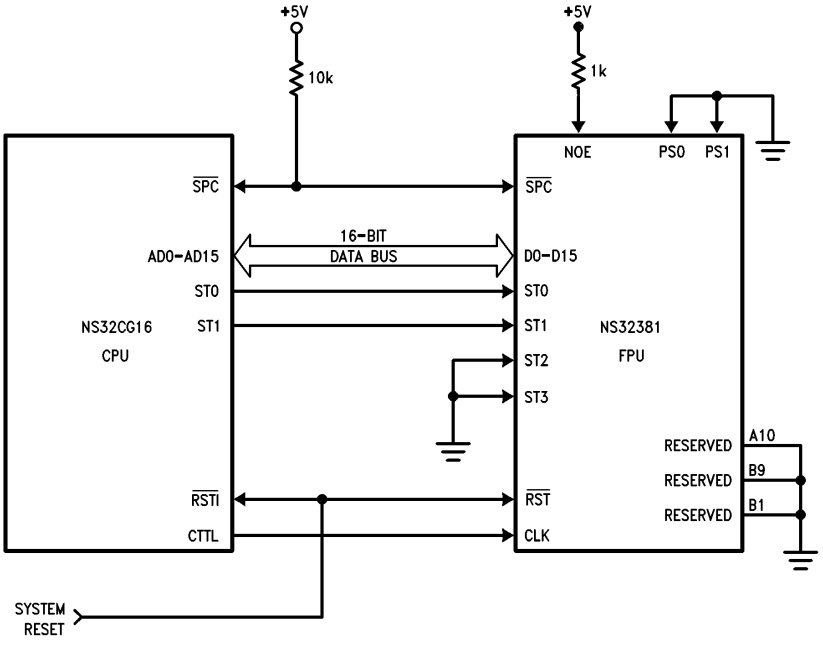
c. System Connection Diagram with the NS32008, NS32016 or NS32032 CPU



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d. System Connection Diagram with the NS32CG16 CPU

FIGURE 5. NS32381 FPU Connections (Continued)

2.0 Protocol

The FPU requires a fixed sequence of transfers (''protocol'') in its communication with the outside world. Each step of the protocol is identified by a status code (asserted to the FPU on pins ST0–ST3) and by its position in the sequence, as shown in *Figure 6*.

The NS32381 supports both the 16-bit and 32-bit general slave protocol sequences.

In the 16-bit protocol: Steps 1 and 2 transfer the instruction to the FPU. Step 1 transfers the first byte of the instruction (the ID Byte) and Step 2 transfers the rest of the instruction (the Operation Word). In Step 2, the two bytes of the Operation Word must be swapped on the bus; i.e., the most-significant byte of the Operation Word must be presented on the least-significant byte of the bus. In the 32-bit protocol, steps 1 and 2 are combined in the first step of the protocol.

Step 3 of the 16-bit protocol, (Step 2 in the 32-bit protocol), is optional and repeatable depending on the instruction. It is used to transfer to the FPU any external operands that are required by the instruction. The operand specified by *gen1* is sent first, least-significant word (or double word for 32 bits) first, followed by the operand specified by *gen2*. If an operand is only one byte in length, it is transferred on the least-significant half of the bus.

The FPU initiates execution upon receiving the last external operand word or, if there are no external operands, upon receiving the Operation Word of the instruction. During this time, the data bus may be used for any purpose by the rest of the system, as long as the $\overline{SPC}$ pin is kept pulled up by a resistor and is not actively driven.

In the 16-bit protocol: Step 5 occurs when the FPU completes the instruction. The FPU pulses the $\overline{SPC}$ pin low to acknowledge that it is ready to continue the protocol. This pulse is called the ''Done pulse''. The bus is not used during this step, and remains floating.

In the 32-bit protocol, $\overline{SPC}$ is only an input to the FPU and dedicated signals indicate DONE/TRAP.

In the 16-bit protocol: In Step 6, the FPU is polled by reading a Status Word. This word indicates whether an exception has been detected by the FPU. In the Compare instruction (CMPf), it also displays the relationship between the operands and serves as the result. This transfer is mandatory, regardless of whether the information presented by the FPU is intended to be used. In the 32-bit protocol this transfer is not mandatory.

Step 7 is, like Step 3 in the 16-bit protocol, (these are the same as Steps 6 and 2 in the 32-bit protocol), optional and repeatable depending on the instruction. Any external result of an instruction is read from the FPU in this step, least-significant word, (or double word), first. If the result is a 1-byte value, it is presented by the FPU on the least-significant half of the bus (D0–D7).

Note: If in Step 6, (Step 5 in the 32-bit protocol), the FPU indicates that an error has occurred, it is permissible, though not necessary, to continue the protocol through Step 7, (Step 6). No guarantee is made regarding the validity of the value read, but continuing through Step 7, (Step 6), will not cause any protocol problems.

If at any time within either protocol another ID byte is sent (ST = 1111), the FPU will prepare itself internally to execute another instruction, throwing away the instruction that was in progress. This is done to support the Abort with Retry feature of the Series 32000 family.

16-Bit General Slave Instruction Protocol

Step	Status	Action
1	ID (1111)	CPU sends ID Byte on least-significant byte of bus
2	OP (1101)	CPU sends Operation Word Bytes swapped on bus
3	OP (1101)	CPU sends required operands (if any), gen1 first, least significant word first
4	—	Slaves starts execution (CPU prefetches)
5	—	Slave pulses $\overline{SPC}$ low
6	ST (1110)	CPU Reads Status Word
7	OP (1101)	CPU Reads Result least significant word first (if destination is memory and if no TRAP occurred)

32-Bit General Slave Instruction Protocol

Step	Status	Action
1	ID (1111)	CPU sends ID and Operation Word
2	OP (1101)	CPU sends required operands (if any)
3	—	Slaves starts execution (CPU prefetches)
4	—	Slave signals DONE or TRAP or CMPf
5	ST (1110)	CPU Reads Status Word (If TRAP was signaled or a CMPf instruction was executed)
6	OP (1101)	CPU Reads Result (if destination is memory and if no TRAP occurred)

FIGURE 6. FPU Instruction Protocol

Because of this feature, however, there is an important consideration when using the FPU in systems that support multitasking: the operating system must not allow a task using the FPU to be interrupted in the middle of an instruction protocol and then transfer control to another task that is also using the FPU. The partially-executed instruction would be thrown away, leaving the first task with a garbage result when it continues. This situation can be avoided easily in software but, depending on the system, some cooperation may be required from the user program. Other solutions involving some additional hardware are also possible.

3.0 Interfacing Guidelines

There are some special interfacing considerations that are required:

1. After the FPU generates the Done pulse, it is necessary to leave the $\overline{SPC}$ pin high for an additional two cycles of CLK before performing the Read Status Word transfer.
2. After performing the Read Status Word transfer, it is necessary to wait for an additional three cycles of CLK before reading a result from the FPU.

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