Interfacing the Dual Port DP8422A to the TMS320C30 and the VME Bus

National Semiconductor
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Lawson Chang
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INTRODUCTION

This application note describes how to interface the TMS320C30 Digital Signal Processor (DSP) and the VME bus to the DP8422A DRAM Controller. This system is running at 16 MHz. It is assumed that the reader is familiar with the DP8422A, TMS320C30, and VME bus operations.

DESCRIPTION

This design consists of Port A of the DP8422A interfaced to the primary bus of TMS320C30 DSP and Port B interfaced to the VME bus. The DP8422A is operated in access Mode 1 and uses the interleaving capability on chip. A Port A access cycle begins when the TMS320C30 places a valid address on the address bus and asserts the strobe (/STRB) signal, only if a refresh or Port B (VME bus) access is not in progress. GRANTB of the DP8422A indicates which port is currently granted to do an access. Port A is the default port upon power up. This design accommodates 4 banks of DRAM (256K x 4), 32 bits in each bank, giving maximum memory capacity of 4M bytes. The schematic diagram is shown in *Figure 1* and simple timing diagrams are shown in *Figures 2* and *3*.

PROGRAMMING MODE AND BITS

Programming the DP8422A is on the first TMS320C30 DSP write after power up. 60 ms initialization period is needed right after this chip access write access programming.

Programming Bits

u = user defined, x = don't care.

R0, R1 = u, u

R2, R3 = u, u

R4, R5, R6 = x, x, x

R7 = 1

R8 = 0

R9 = u

C0, C1, C2 = 0 1 0 (16 MHz)

C3 = 0

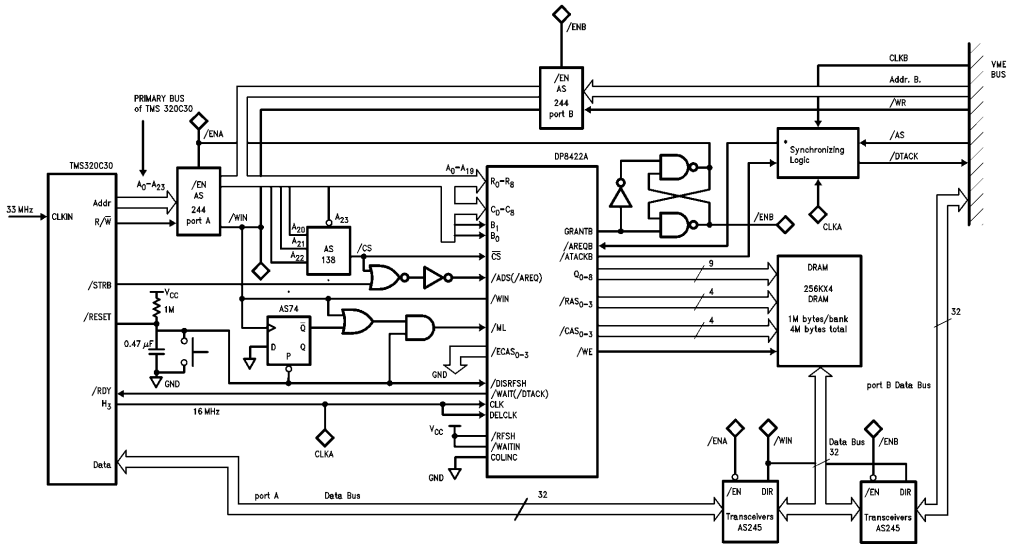
C4, C5, C6 = u, u, u (or 0, 1, 1)

C7, C8 = u, u

C9 = 1

B0 = 0

B1 = 1



TL/F/10558–1

FIGURE 1. Interfacing DP8422A/TMS320C30 Schematic Diagram (Interleave Mode)

*Please refer to Interfacing the DP8422A to an Asychronous Port B in a Dual 68020 System application note.

  RRD-B30M75/Printed in U. S. A.

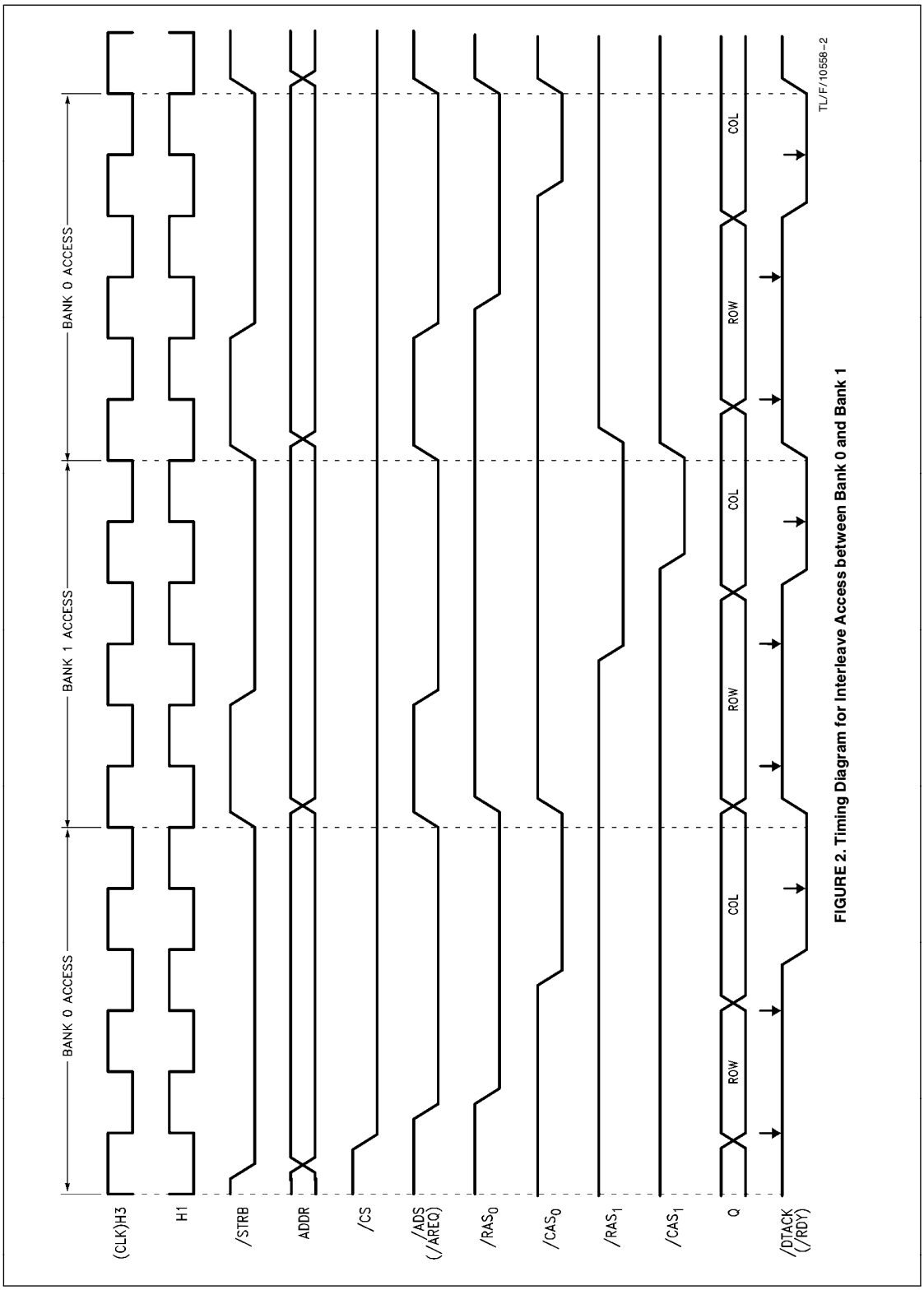
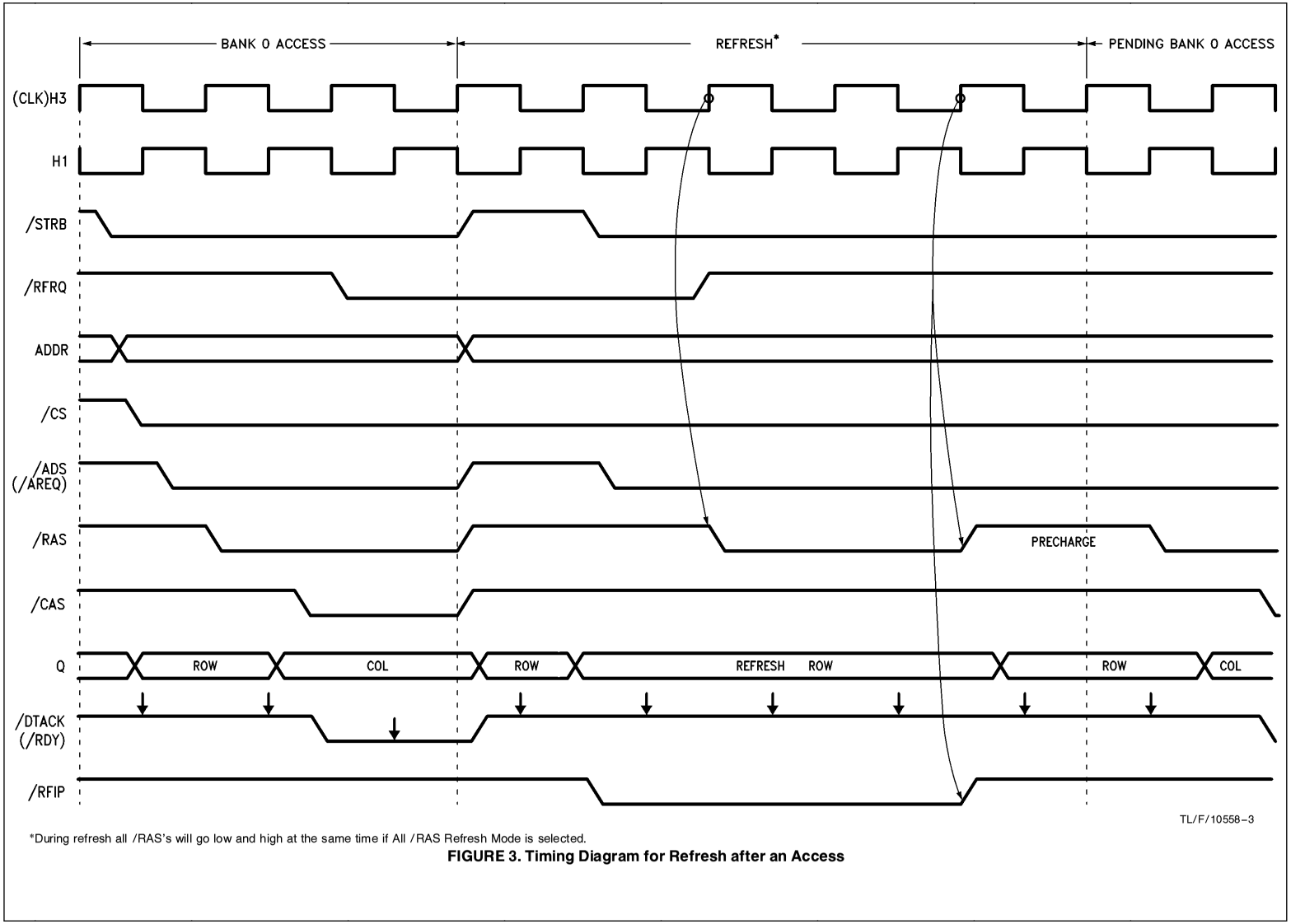


FIGURE 2. Timing Diagram for Interleave Access between Bank 0 and Bank 1



*During refresh all /RAS's will go low and high at the same time if All /RAS Refresh Mode is selected.

FIGURE 3. Timing Diagram for Refresh after an Access

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998