Dynamic Threshold for Advanced CMOS Logic

National Semiconductor
Application Note 680
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INTRODUCTION

Most users of digital logic are quite familiar with the threshold specifications found on family logic data sheets. Designers using products with TTL level input thresholds will see numbers like $V_{IH} = 2.0V$ and $V_{IL} = 0.8V$. These threshold guarantees are static, a part's response to these levels during switching transients can be undesirable. Through the course of this paper the reader should gain an understanding for the difference between a static threshold and a dynamic threshold. This paper will also discuss how various products respond dynamically, how dynamic thresholds are tested, and specified. Lastly, this paper will look at how FACT Quiet Series™ has addressed and specified dynamic threshold characteristics.

WHAT IS A DYNAMIC THRESHOLD?

If National Semiconductor were able to package its I.C.'s in ''ideal'' packages, then dynamic and static thresholds would be one and the same. However, our package, like that of all our competitors, is not ''ideal'' and has a finite amount of inductance associated with each signal lead. As will be shown later, it is the inductance in the power leads which are the primary cause for the non-ideality.

To understand the phenomena of dynamic thresholds the properties of ground bounce must first be examined. *Figure 1* is a representation for a 74XX00 product which includes package inductance. *Figure 2a* shows an output pulldown making an HL/ZL transition. In discharging the load capacitor a current I_C equaling C*dv/dt flows into the chip, this current is approximated versus time in *Figure 2b*. The changing current, I_C, generates a voltage across the ground inductor represented in *Figure 2c* through the equation L*di/dt. It is the voltage across the ground inductor, commonly known as ground bounce, which is the cause for static and dynamic thresholds to differ.

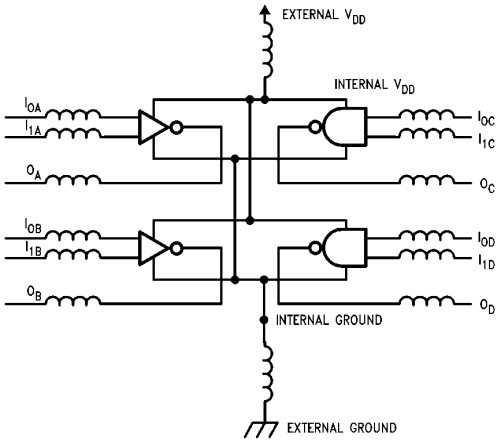

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FIGURE 1. A Typical "00" 2-Input Quad NAND Gate

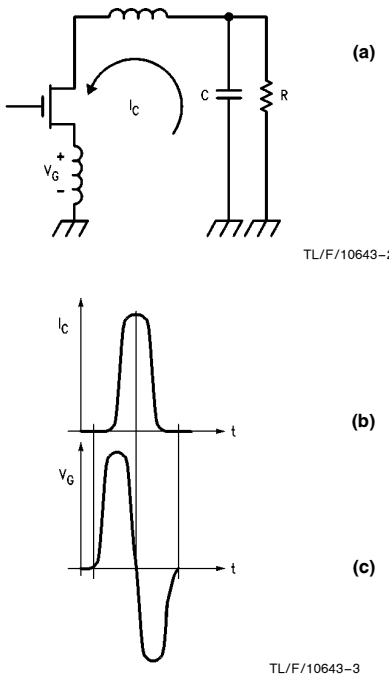

FIGURE 2

The threshold of an IC is referenced to its internal ground. Therefore, voltages induced on the ground inductor are reflected directly as a change in threshold with respect to external ground. *Figure 3* shows the effects of ground bounce on an input threshold. If when the threshold is moving it crosses the input voltage levels, a problem area exists. However, having the threshold cross the input level does not necessarily induce a product failure. The threshold must cross the input level for a period of time for a false switch to occur. (*Figure 4* shows the voltage time relationship). Note that in the high speed technologies two things have come together, faster delays and output edge rates, generally meaning larger di/dt's, and an ability to react to narrower pulses.

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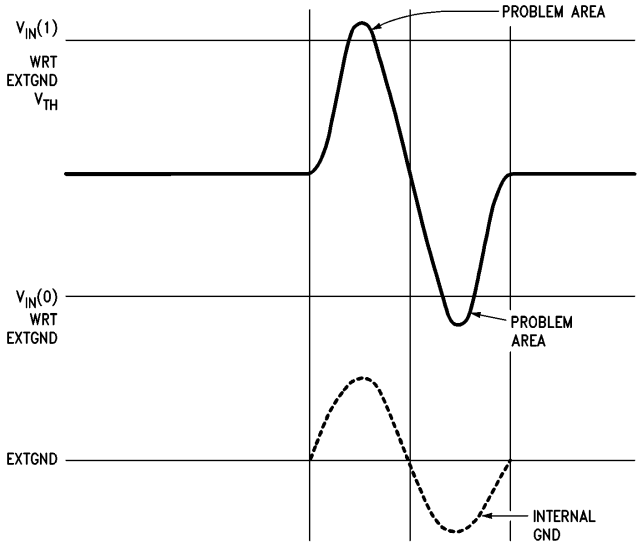

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FIGURE 3

V_{IL} Noise Rejection

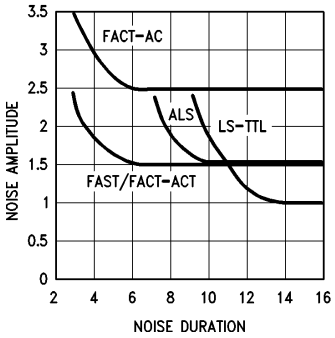

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FIGURE 4

In the example discussed above, ground bounce was outlined as the cause for the threshold change. For bipolar TTL technologies, this is the only noise source of concern since the threshold is created by a V_{BE} stack referenced to ground. As V_{DD} changes in a bipolar circuit, the threshold will change logarithmically as the currents in the transistors change, i.e., a 1V change in V_{DD} creates approximately a 34 mV shift in threshold. CMOS thresholds are set up as a percentage of V_{DD} and track linearly with V_{DD} changes. Therefore, a noise spike on V_{DD} from an LH/ZH transition generates dynamic threshold characteristics which must be considered along with those of the HL/ZL edges. In this example let internal ground bounce to a 1V peak; the bipolar threshold will peak to approximately 2.5V while the CMOS circuit will peak to $((V_{th}/V_{DD}{}^*(V_{DD} - V_{bounce}) + 1.0V) = ((0.3^*(4.0) + 1.0) = 2.2V$. Consider a negative bounce of 1V on the internal V_{DD} bus, the threshold delta for the bipolar product will be negligible, but the CMOS chip's threshold will change as follows: $((V_{th}/V_{DD}{}^*(V_{DD} - V_{bounce})) = (0.3^*(4)) = 1.2V$.

HOW ARE DYNAMIC THRESHOLDS SPECIFIED?

A circuits dynamic threshold characteristics are quantified with the specifications V_{IHD} and V_{ILD}, where the "D" appendage stands for "dynamic". The definitions are as below,

- V_{IHD}— The minimum HIGH input level such that normal switching/functional characteristics are observed during output transients.
- V_{ILD}— The maximum LOW input level such that normal switching/functional characteristics are observed during output transients.

HOW ARE DYNAMIC THRESHOLDS CHARACTERIZED?

The characterization of dynamic thresholds requires some planning for each product. The test will vary depending upon which edge will generate the supply noise; i.e., is the edge an LH or a ZL? Is the test for a data or control pin? This section discusses the planning process for testing an ACQ244, ACQ374, and an FCT534. From this discussion the reader should be able to test other products and understand the FACT Quiet Series dynamic noise specifications.

Test Fixturing/Setup: Dynamic threshold tests are sensitive to the test configuration. The same considerations used to measure AC propagation delays should be exercised. National Semiconductor uses the same fixturing for both AC propagation delay and noise testing. The inputs for this test are driven with a word generator running at 1 MHz which has been deskewed such that no more than 150 ps exists between channels. FACT Quiet Series specifies V_{IHD}/V_{ILD} at 25°C with V_{DD} at 5.0V. For CMOS, true worst case exists where ground bounce is maximized, at cold temp high V_{DD}. Bipolar circuits are not as straightforward; the threshold has a temperature coefficient tracking its V_{BE} stack which can change nearly a volt from −55°C to +125°C. The temperature and V_{DD} that create worst case bounce may not induce worst case V_{IHD}/V_{ILD}.

Each product subject to V_{IHD}/V_{ILD} testing will have multiple test possibilities. Through the case studies below, the reader should gain an understanding for some of the test tradeoffs.

Case 1: Product = ACTQ244 test data pins with LH/HL transitions.

The algorithm for this test is as follows. Maximize the number of outputs switching, N, in this case 8. N − 1 of the inputs will be transitioning to and from nonthreshold levels, 0V–3V. The last input will transition from 3V to V_{ILD} or from 0V to V_{IHD}. *Figure 5* shows the four combinations of tests. It should be noted that values of V_{ILD} and V_{IHD} that induce failure will vary as a function of the test pin. This is due mostly to voltage drops on the internal power bussing. As a result, pins farthest from the ground pin, and sometimes the V_{CC} pin, are likely to be worst case pins.

Case 2: Product = ACTQ244 test data pins with ZL/ZH transitions.

This test will ramp the enable pin from 3V–0V while holding the input under test at threshold, i.e., have all outputs transitioning ZL, with N − 1 inputs at 0V and the input under test at V_{ILD}. The other tests are as follows, N − 1 transitioning ZL pin under test (PUT) at V_{IHD}, all outs going ZH PUT at V_{IHD}, and N − 1 a ZH switch and PUT at V_{ILD}.

Case 3: Product = ACTQ244 test OE pin with HL/LH transitions.

V_{ILD} is the parameter to check here. Data inputs should be switching 0V–3V while the OE pin is being stepped up from 0V to V_{ILD}. While testing the OE pin with an LH output transition, the standard 50 pF, 500Ω load should be used. When testing with an HL on the output, the TRI-STATE® ZL/LZ 500Ω to V_{CC} * 2 should be used. Without the pullup resistor, failure cannot be detected. The LZ and HZ edges create supply noise by switching off currents being sourced or sunk by the device. With standard AC loading, their transients are much less than those of the other edges. Therefore, V_{IHD} for the chip is guaranteed by the data pins.

The test cases discussed in cases 1–3 are all possible test methods, note there are other possible combinations. In practice National has found that tests done in conjunction with HL transitions are worst case, i.e., case 1, and will guarantee V_{ILD} and V_{IHD} for the chip.

Case 4: Product = ACTQ374

This class of function, the non-inverting register, will have very good data and clock pin dynamic threshold characteristics. For instance, take the worst case bounce where all output are transitioning HL. To accomplish this, all inputs are LOW on the active edge of clock. If a V_{IHD} test of the clock were performed, the positive ground bounce at some level of V_{IHD} will stimulate one, if not multiple, false clocks to occur. A failure is not detected because the false clock or clocks merely regenerated an existing low output. The positive ground bounce had the effect of making the logic low data look lower. Always associated with positive bounce is negative bounce, which on an HL transition occurs later. If this negative bounce is able to switch the internal data gate, setup and hold times have been violated and again failure is not detected. Reference *Figure 6* for a representation of this scenario.

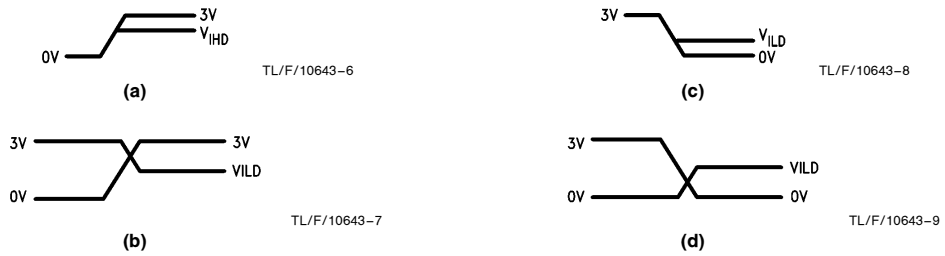
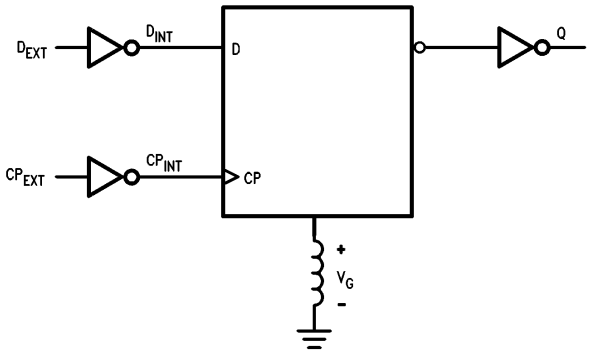


FIGURE 5



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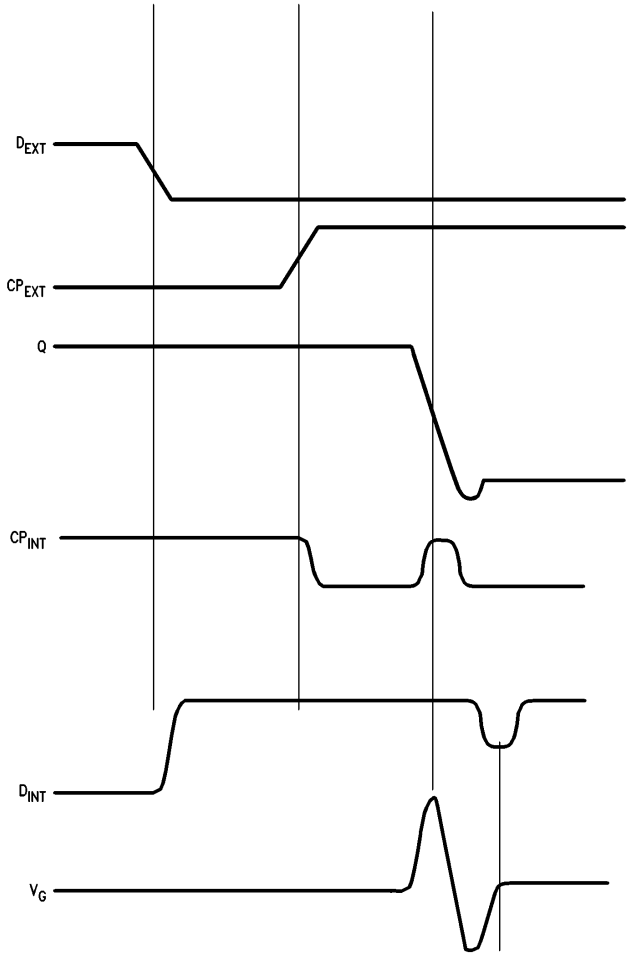
(a)



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(b)

FIGURE 6

The most rigorous test for the non-inverting flop will be to have clock held at V_{IHD}, data at a hard HIGH, and all outputs are transitioning ZL.

Case 5: Product = FCTQ534

The inverting products, as this one is, inherently have poorer V_{IHD}/V_{ILD} characteristics than the non-inverting. While testing a 240 is straightforward, the 534 testing and results require further consideration. While the output is transitioning, both data and clock are HIGH. If data is held at a hard HIGH and clock lowered, false clocks occur, but a failure is not detected. The reverse is also true, as data is lowered, the data gate changes, but no clocks occur. However, as both data and clock HIGH levels are lowered simultaneously a window of V_{IHD} failure will be observed.

Figure 7 plots this ''window of failure''. This plot will be examined by sweeping from right to left. It can be seen that for clock V_{IHD} levels down to approximately 2.6V, proper data continues to clock out for data levels down to 1.5V, the static threshold value. For all V_{IHD} voltages of the clock below 2.6V, false clocking exists. If data is raised high enough, no internal data changes occur and therefore no product test failures. A data is lowered, internal data pulses down (*Figure 8*). The initial internal pulses may not cause device failure either because the voltage has not dropped to a valid logic level or because setup and hold times to the master latch have not been satisified, but eventually failures are observed. It is interesting to note that were the FCT534 to have a more positive hold time, its hold time is slightly negative, the data voltage inducing failure would be much lower.

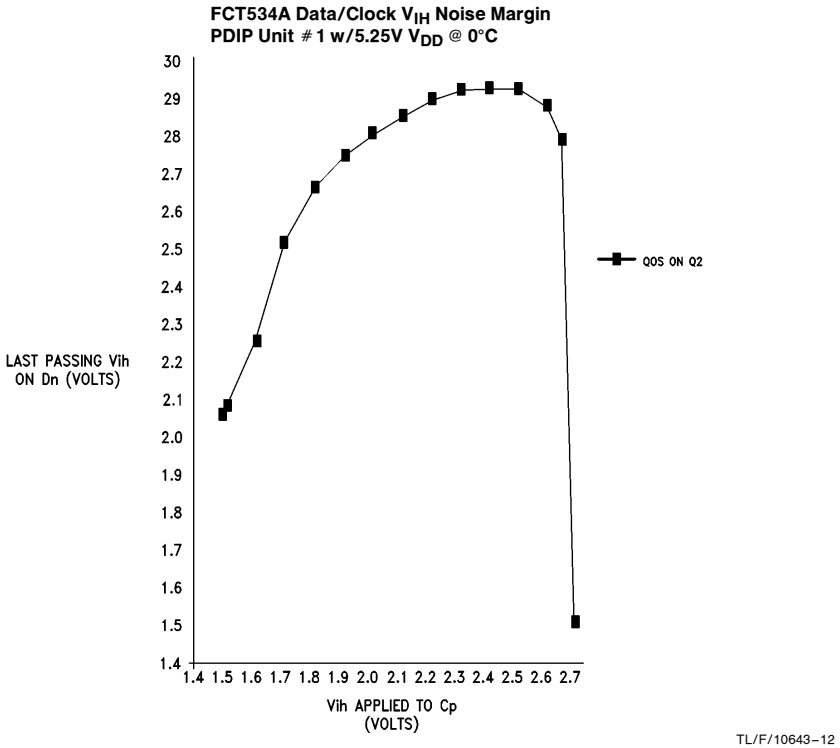

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FIGURE 7

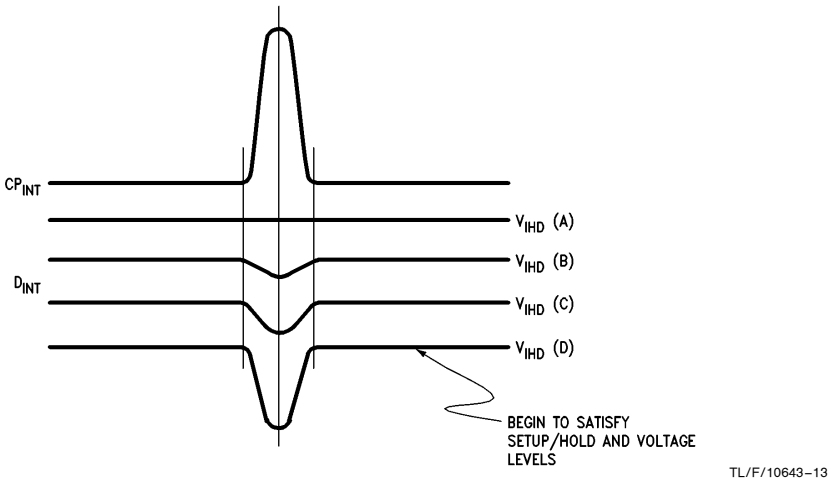

FIGURE 8

The implication of the data in *Figure 7* is that if the high voltage levels droop down to approximately 2.9V on data and 2.6V on clock simultaneously, a system failure is possible. How can these conditions exist at the same time? The temperature of *Figure 7* is 0°C, if the inputs are driven by TTL drivers at a $V_{DD} = 4.5V$, 2.6V V_{OH}'s are possible. However, the V_{DD} of the plot is 5.25, assuming the driver TTL chips are on the V_{DD} bus, the HIGH levels will be greater than 2.6V. There is another variable to be considered before stating that no problem exists: what termination scheme is being used? If both data and clock signals come from transmission lines using either parallel or thevenin termination, HIGH voltage levels below 2.6V are possible. If either or both of the signals are unterminated, series terminated, or AC terminated then functionality is assured. In summary, a problem may exist if this parts data and clock pins are driven by parallel or thevenin terminated transmission lines while the V_{DD} bus is at 5.25V and the junction temperature is 0°C.

HOW DO DYNAMIC THRESHOLD PROBLEMS MANIFEST THEMSELVES?

There are three main modes of failure during dynamic threshold testing. Firstly, the part can malfunction through a state change. Also possible are oscillations, glitches, AC delay changes, and slew rate degradation. One octal register tested recently was seen to exhibit metastable type characteristics. Failure criteria are as follows.

- On a LOW output the LOW level will not rise above a TTL threshold LOW, 0.8V, after the transition of the output.
- On a HIGH output the HIGH level will not drop below a CMOS threshold HIGH, 3.5V @ $V_{DD} = 5.0V$, after the transition of the output.
- If the natural ringing, other than initial switching rail bounce, of the output violates the previous two criteria then the ringing amplitude will be noted. Failure is then defined as a 100 mV movement in the output toward the threshold from the peak ringing amplitude, (*Figure 9*).
- Gross failures will include functional state changes, oscillations, AC delay changes, and slew rates effects.

HOW DO DYNAMIC THRESHOLD PROBLEMS AFFECT DIFFERENT FUNCTIONS?

All the products discussed thus far pass the FACT Quiet Series dynamic threshold limits of $V_{IHD} = 2.2V$ and $V_{ILD} = 0.8V$, which are specified as being tested singularly. The case of the FCTQ534 represents one where much effort was required to observe the failure mode. There are classes of product that will display clock V_{IHD} failures readily. These would be products which toggle the outputs independent of data. The most common functions in the list would be counters and shift registers. If the 74XXX299 clock pin were tested, the initial clock edge would shift data inducing ground bounce. If the clock V_{IHD} is low enough, it will be that observed false clocks will continue until all outputs are in the same logic state as the serial data pin.

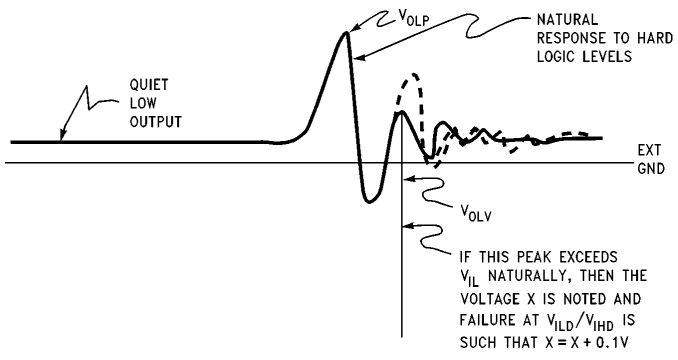

FIGURE 9

WHAT DOES FACT QUIET SERIES DO TO ADDRESS DYNAMIC THRESHOLDS?

The Quiet Series product utilizes two technical innovations to accomplish its performance. First, by using a split ground bus configuration, input and output grounds are given a degree of isolation. Schematically this is shown in *Figures 10a* and *b*. The ground bus for inputs stages and outputs sections are separated on chip and only connected by the common inductance near the shoulder of the package and a mutual inductance between the leadframe fingers. Note, the V_{DD} input and output V_{DD} busses are electrically shorted on chip by the substrate resistance. The leadframe inductance forms a voltage divider such that the input only sees a percentage of the output ground noise. Secondly, a proprietary GTO™ technology, shown in *Figure 10c*, is used to shape the output edge. This then yields an output voltage waveform shown in *Figure 10d*. The soft turn on of the output attenuates the dv/dt, and therefore the di/dt presented to the ground inductance, yielding a reduction in the ground noise.

HOW DOES NATIONAL COMPARE WITH OTHER VENDORS?

The characteristics of National Semiconductor's FACT Quiet Series ensure superior dynamic threshold performance in conventional corner pinned packaging. The split power rail technology used to isolate inputs and outputs addresses a noise issue which goes unresolved in multiple power pin ACL logic families, and most single pin families. The same split rail technology is used in the FACT FCT and FCTA logic lines. Referencing the FCT534 already discussed, *Figure 11* shows one of the dramatic differences created by the Quiet Series technology.

SUMMARY

With the new advanced CMOS technologies, the specifications and characteristics for dynamic thresholds need to be considered along with the other variables that impact the choice of a device type or family. This applications note has discussed the theories of test philosophy, failure criteria, and the root causes of dynamic thresholds. This information should provide the systems designer the tools to analyze any impact to design performance.

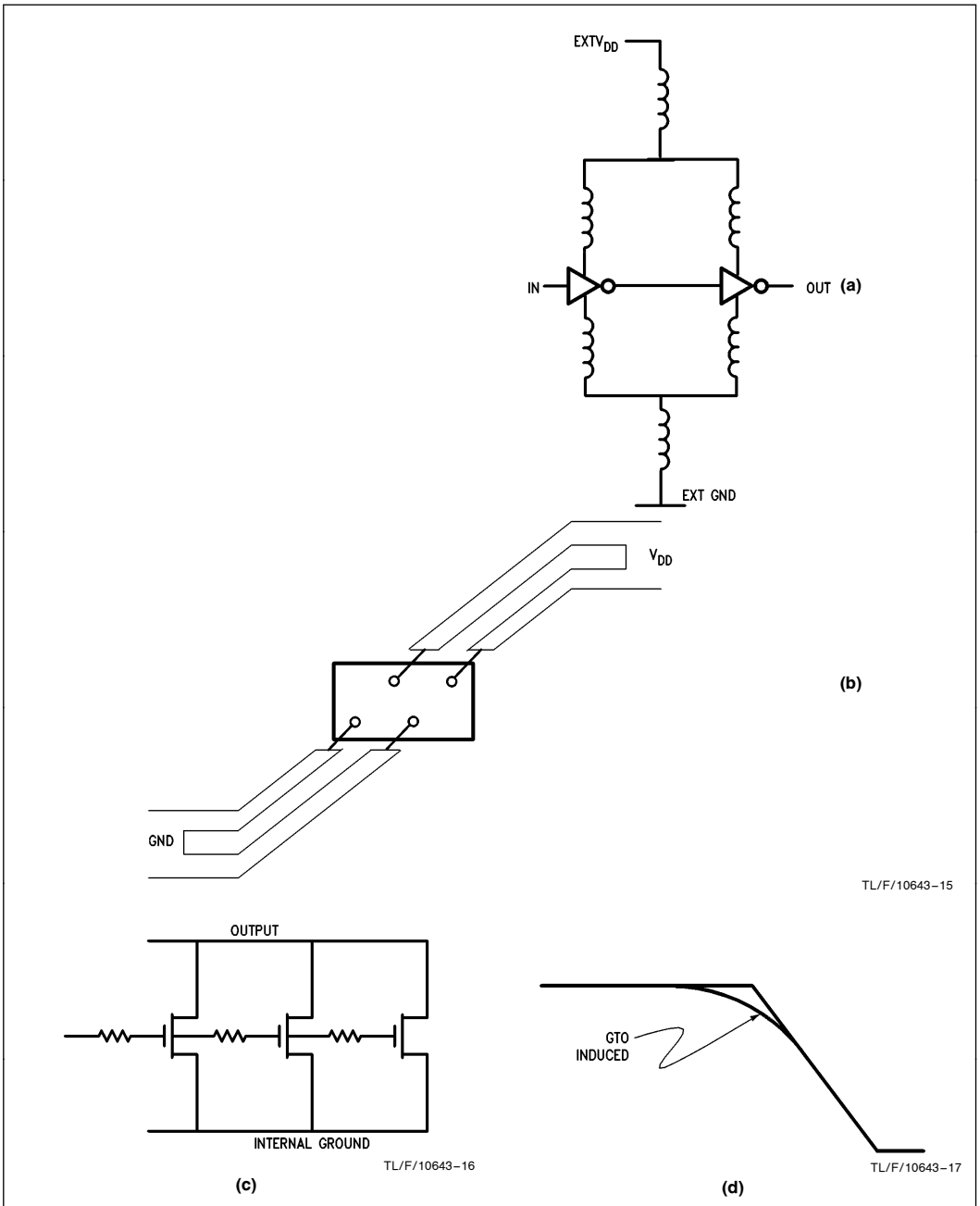
EXTV$_{DD}$
IN
OUT
(a)
EXT GND
V$_{DD}$
(b)
GND
TL/F/10643–15
OUTPUT
INTERNAL GROUND
TL/F/10643–16
(c)
GTO
INDUCED
TL/F/10643–17
(d)

FIGURE 10

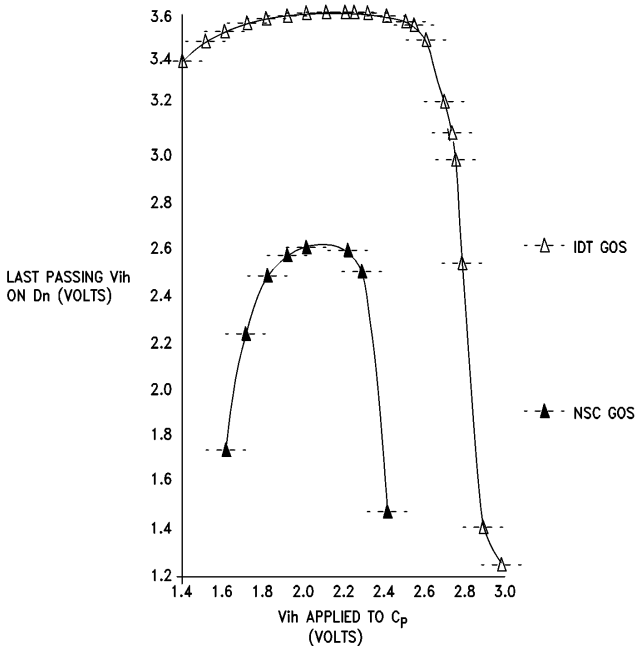

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FIGURE 11. 'FCT534A Data/Clock V_{IH} Noise Margin IDT #5 (PDIP) vs NSC #2 (CDIP) 5.0V V_{DD} @ Room

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