IEEE 896 Futurebus+—A Solution to the Bus Driving Problem

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The IEEE 896 Futurebus+ is a general-purpose bus standard for high-performance microcomputer systems. With a strong emphasis on speed and reliability, IEEE 896 offers a number of innovative features that are not found in other backplane buses.

A major contribution to its performance comes from its electrical specifications. Futurebus+ solves, for the first time, the fundamental problems associated with driving a densely populated backplane—as a result, it provides significant improvements in both speed and data integrity. Two years of effort by the IEEE 896 committee have culminated in a deeper understanding of the physics of the backplane bus, leading to an ingenious solution to the bus problem.

Speed is probably the most important feature of any bus standard. This is especially true for Futurebus+, since its totally asynchronous protocol permits continuous speed enhancements through advances in technology. In fact, the maximum data transfer rate between any two plug-in cards is determined simply by the sum of the response times of the two cards and the bus delay. Ultimately, as logic devices get faster, bus delay will be the dominating factor limiting bus speed.

There are two components to the bus delay in a typical system, namely, the settling time and the propagation delay. The settling time is the time needed for reflections and crosstalk to subside before data are sampled; it is usually several times longer than the backplane propagation delay. As will be shown later, the settling time is the price the user pays for not driving the bus properly.

By using a new technology, BTL = Backplane Transceiver Logic, Futurebus+ not only eliminates the settling time delay but also reduces the propagation delay of the loaded backplane to provide maximum possible bus throughput.

THE PHYSICS OF THE BACKPLANE BUS

For high-speed signals the bus acts like a transmission line with an associated characteristic impedance and propagation delay whose unloaded values, Z_o and t_{po}, are given by

$$Z_o = \sqrt{\frac{L_0}{C_0}}$$

$$t_{po} = \sqrt{L_0 C_0}$$

L = distributed inductance per unit length, and C = distributed intrinsic capacitance per unit length.(1)

These values can be calculated for a typical microstrip backplane *(Figure 1)* by means of the following equations:

$$Z_o = (87/\sqrt{\epsilon_r + 1.41}) \bullet \ln [5.98h/(0.8w + t)]\,\Omega$$

$$t_{po} = 1.017\sqrt{0.475\,\epsilon_r + 0.67}\ \text{ns/ft}$$

where ϵ_r = relative dielectric constant of the board material (typically $\epsilon_r = 4.7$ for fiberglass and w,h,t = the dimensions indicated in *Figure 1*. For a typical backplane, t = 1.4 mils, w = 25 mils, h = 1/16 inch, and $\epsilon_r = 4.7$. By substituting these values we get $Z_o = 100\Omega$ and $t_{po} = 1.7$ ns/ft.

These values correspond to an *unloaded* backplane. When the backplane is uniformly loaded with the capacitance of plug-in cards and connectors at frequent intervals, the loaded values of the impedance, Z_L, and the propagation delay, t_{pL}, are given by

$$Z_L = Z_o/\sqrt{1 + (C_L/C_0)}$$

$$t_{pL} = t_{po}\sqrt{1 + (C_L/C_0)}$$

where C_L = the distributed load capacitance per unit length.(1)

The distributed capacitance, C_0 of the unloaded backplane can be measured in the lab. For our microstrip, it is 20 pF/ft. This does not include, however, the capacitance of the connectors mounted on the backplane and the associated plated-through holes, which can amount to 5 pF per card slot.

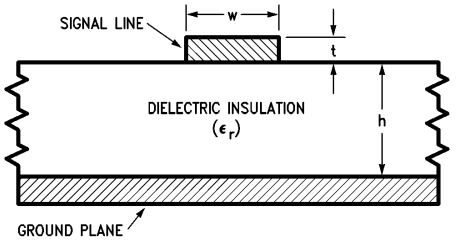

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FIGURE 1. Cross Section of a Microstrip Bus Line

The loading capacitance of the plug-in card, however, is dominated by the loading capacitance of the transceiver, which can be 12–20 pF for TTL devices. Allowing another 3–5 pF for printed-circuit traces and the connector, the total loading per card slot can add up to 30 pF. For a system such as IEEE 896, which has 10 slots per foot, C_L = 300 pF/ft. Therefore,

$$Z_L = 100/\sqrt{1 + (300/20)} = 25\Omega$$

$$t_{pL} = 1.7\sqrt{1 + (300/20)} = 6.8\ \text{ns/ft}$$

As can be seen above, the capacitive loading drastically alters both the impedance and the propagation delay of the bus. This reduces the bus throughput in two ways. One obvious impact is the increased propagation delay. But the not so obvious and even more serious problem is the reduced bus impedance, which is much harder to drive.

For example, to drive the loaded bus properly with a TTL driver which has a 3V nominal swing, the required drive current, I_D, must be

$$I_D = 3V/(Z_L/2)$$

The impedance seen by the driver is half of Z_L, since from a given board two transmission lines are being driven, one towards each terminator *(Figure 2)*. Therefore,

$$I_D = 3/(25/2) = 240\ \text{mA}$$

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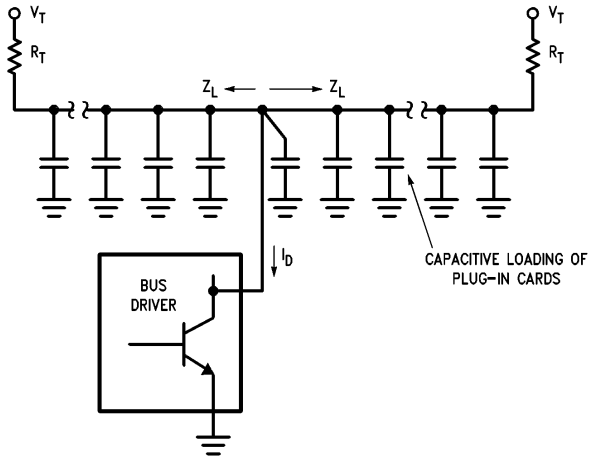

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FIGURE 2. The Loaded Bus—Each Driver Sees Two Loaded Line Impedances in Parallel ($Z_L \| Z_L = Z_{L/2}$).

This is much higher than the standard TTL's drive capability of 50 to 100 mA. *Figure 3* shows the effect of using a 50 mA driver, in this situation, on the bus waveform. The voltage swing on the bus has its first transition at 0.5V, the product of the drive current and $Z_L/2$. This value falls well below the upper threshold limit of the TTL receiver. Therefore, *several round-trip delays to the nearest termination are required for the waveform to cross the receiver threshold region*. In our example, one round-trip delay is $2t_{pL} = 13.6$ ns/ft. Therefore the settling times can exceed 100 ns even for relatively short buses. This long settling time drastically affects bus throughput at high speeds. Even worse, the voltage steps in the threshold region can cause multiple triggering in the cases of the clock and strobe signals.

One way to solve these problems is to use 100 mA drivers with precision receivers that have a narrow threshold region such that the first transition crosses well over the threshold. This technique is widely used for clock lines to avoid multiple triggering. Its use on data/address lines is limited because of the significantly higher power requirement arising from the large number of lines involved (32 address/data lines).

Even if power is not a limitation, switching to higher current drivers provides only a marginal improvement. The reason for this is quite simple. A higher current driver unfortunately has a higher output capacitance, which reduces the bus impedance further. This in turn requires an even higher current drive for proper operation.

The Futurebus+ Transceiver

A more elegant solution—one that is now a part of IEEE 896—directly attacks the root of the problem, namely, the large output capacitance of the transceiver. By simply adding a Schottky diode in series with an open-collector driver output, the capacitance of the drive transistor is isolated by the small reverse-biased capacitance of the diode in the non-transmitting state *(Figure 4)*. The Schottky diode capacitance is typically less than 2 pF and is relatively independent of the drive current. Allowing for a receiver input capacitance of another 2 pF, the total loading of the Futurebus+ transceiver can be kept under 5 pF. IEEE 896 specifies the maximum transceiver capacitance at 5 pF.

In addition to reducing the loading on the bus, the Futurebus+ transceiver features several other enhancements over a conventional TTL transceiver that drastically reduce power consumption and improve system reliability.

A major portion of the power savings comes from a reduced voltage swing—1V—on the bus. Contrary to popular belief, the lower swing does not reduce crosstalk immunity (provided the receiver threshold is tightly controlled).[2] The induced crosstalk from other lines on the bus scales down with the amplitude of the signal transistion causing it. Consequently, if a line receiver has a precision threshold, the noise margin, expressed as a percentage of signal amplitude, remains the same, as does the crosstalk immunity. However, the absolute noise margin, with reference to a noise source external to the bus, does shrink linearly with amplitude. Fortunately, the low impedance and the relatively short length of the bus make this externally generated noise component insignificant in high-speed backplanes. Nevertheless, it is recommended that the backplane be shielded from strong noise sources external to the bus.

Noise Immunity and EMI

The Futurebus+ transceiver has a precision receiver threshold centered between the low and high bus levels of 1V and 2.1V, respectively *(Figure 5)*. Confined to a narrow region of 1.55V ±75 mV (1.47V to 1.62V), the threshold voltage is independent of V_{CC} and temperature. This tight threshold control is achieved by using an internal bandgap reference at the receiver input *(Figure 4).* And with the smaller 1V swing, EMI is also reduced threefold compared with TTL.

DRIVE CURRENT

The backplane impedance in IEEE 896 is specified as 52Ω minimum and 62Ω maximum with the connectors mounted. In our microstrip example, due to the connector and the plated-through holes, a 52Ω minimum impedance translates into a maximum allowable capacitance of 5 pF per slot. This can be easily attained with some care in printed-circuit board design. A fully loaded Futurebus+ backplane therefore, has an impedance whose worst-case value is given by

$$Z_{min} = \frac{100}{\sqrt{1 + \frac{150}{20}}}\ \Omega$$

$$= 34\Omega$$

The drive current required for a 1V swing is

$$I_D = 1/(34/2) = 58\ mA$$

However, with a precision receiver threshold it is possible for the driver to swing past the threshold with a comfortable margin even if the first step climbs to only 75 percent of the final amplitude under worst-case loading (see again *Figure 5*). Therefore, the drive current can be reduced by 25 percent to save power, without affecting performance:

$$I_D = \frac{1}{34/2}\,0.75 = 45\ mA$$

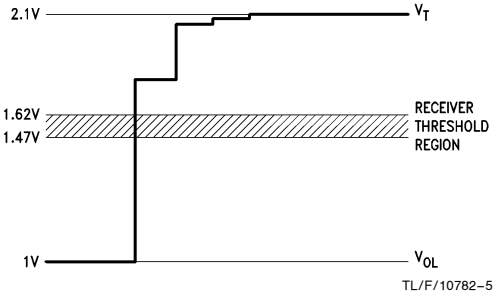

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FIGURE 5. IEEE 896 Signaling Levels and the Worst-Case Bus Waveform

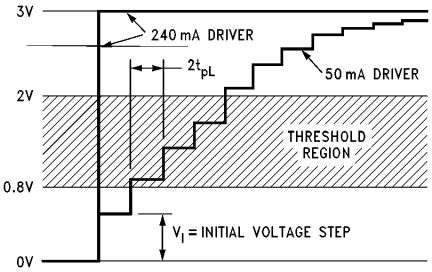

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FIGURE 3. TTL Bus Waveforms—50 mA Driver vs 300 mA Driver

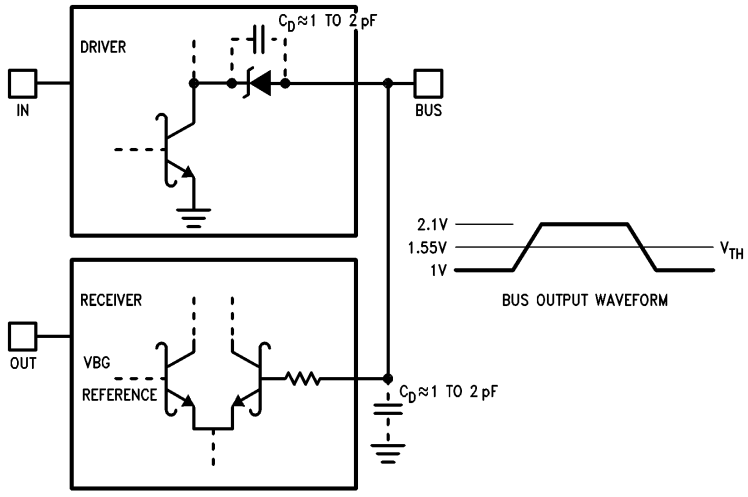

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FIGURE 4. The Futurebus+ Transceiver

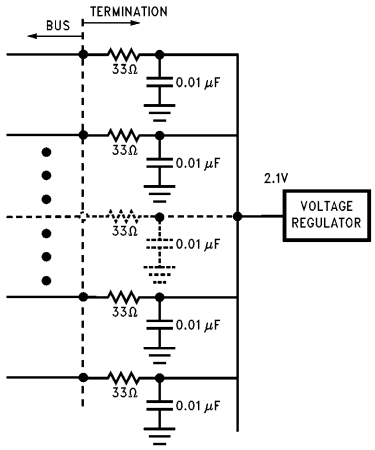

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FIGURE 6. Equivalent Futurebus+ Termination Circuit

OTHER HIGHLIGHTS

Bus Propagation Delay

There is an additional benefit resulting from reducing the capacitive loading on the bus. This benefit arises from the reduced propagation delay, which further improves the bus speed.

Recalculating the loaded propagation delay for the Futurebus+ transceiver yields

$$t_{PL} = t_{po}\sqrt{1 + (C_L/C_0)}$$
$$= 1.7\sqrt{1 + \frac{150}{20}}$$
$$= 4.9\ \text{ns/ft}$$

This is a 30-percent improvement over the TTL example. It should be noted that this is the worst-case delay per foot and that the asynchronous nature of the Futurebus+ protocol will take full advantage of lower propagation delays in a typical system, either due to lower loading levels or due to the closer spacing of two plug-in boards that are in communication.

Termination

The drive current and the signal swing determine the termination resistors. If the drive current is derived properly, the termination will match the bus impedance under the given loading. For IEEE 896, the value of each of the two termination resistors, R_T, is

$$R_T = \left(\frac{1V}{58\ mA}\right) 2 = 34\Omega \approx 33\Omega$$

This value is less than the loaded impedance of the Futurebus+, because simulations by the Futurebus+ Electrical Task Group show it is the best value. In a practical bus, the impedance varies with the loading conditions and the above termination is a compromise. Simulations show that the best noise margins can be maintained by using the 33Ω terminations.

The P896 draft requires that the bus be terminated at both ends, with a single resistor of 33Ω connected to an active voltage source of 2.1V *(Figure 6)*. This arrangement has a significantly lower power dissipation than a ''Thévenin-equivalent'' two-resistor termination connected to ground and the 5V rail. *Figure 6* shows an equivalent circuit that can be used for terminating a few of the bus lines. Since each bus line has the potential of sinking 80 mA, the termination voltage must be able to supply adequate current for the worst case situation of all lines asserted simultaneously. The inherent inductance and decoupling capacitors of the termination voltage supply are crucial to the performance of the system. The source can be shared among bus lines as long as it is properly bypassed for alternating current close to each resistor.

Wire-OR Glitch

One of the advantages of an open-collector bus is a wire-OR capability. This feature is fully exploited in the IEEE 896 bus, particularly in its sophisticated arbitration protocol and broadcast mechanism. Unfortunately, due to the fundamental nature of transmission lines, wire-ORing on the bus can cause erroneous glitches having pulse widths of up to the round-trip delay of the bus. The analysis of the wire-OR glitch is covered well by Theus and Gustavson.[5]

To overcome the wire-OR glitch, the broadcast acknowledge lines (AI* and DI*) and the three arbitration control lines are required to have integrators at the output of the receiver capable of rejecting pulses having widths of up to the maximum round-trip delay of the bus.

And More

Geographic addressing and live insertion and withdrawal capability are some of the other highlights of Futurebus+.

The electrical specification of Futurebus+ is based on a thorough knowledge of backplane operation. A combination of theoretical analysis and bench measurements has been used to create an electrically clean bus environment. Significant improvements have been made in favor of higher performance—at the expense of only a slight increase in today's cost and complexity—to assure a long design lifetime for the standard. The result is a proposed standard that has the performance, in terms of both speed and reliability, to justify the name, ''Futurebus+''.

ACKNOWLEDGEMENT

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