Designing FDDI Concentrators

National Semiconductor
Application Note 675
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INTRODUCTION

The Concentrator plays an important role in the Fiber Distributed Data Interface (FDDI) architecture. This application note introduces the concentrator, discusses its applications and describes its structure. It also illustrates how to build various kinds of concentrators with the National Semiconductor FDDI chip set. After covering Station Management requirements, it concludes with a thorough discussion of clocking considerations, including a set of rules to guide the designer through this important part of the implementation.

WHAT IS A CONCENTRATOR?

FDDI employs dual counter-rotating rings which, among other benefits, allow a network to continue working in the presence of a single failed link or node. Such a failure causes the network to go into ''wrap'', wherein the station directly upstream of a failure re-routes its output to the secondary ring while the station immediately downstream of the failure accepts input from the secondary ring. A subsequent failure segments the network, isolating stations on one segment from those on the other.

The standard defines two classes of stations: a dual attachment station (DAS) which connects directly to both rings and a single attachment station (SAS) which connects to just one of the rings. Concentrators support the connection of single attachment stations to the network, allowing communication between SAS and DAS stations.

A concentrator, which itself can be either a single attachment or dual attachment node, provides ''drops'' to individual nodes, thereby including them on one of the rings. When it senses a failure on one of its drops, it ''heals'' the ring by electronically bypassing that drop. Properly designed concentrators can bypass any number of drops with no degradation in ring performance.

The standard allows dual attachment nodes to connect into a concentrator in the same way as a SAS, creating redundancy at this level. Further, it allows one concentrator to connect into another, providing additional flexibility.

BENEFITS OF USING CONCENTRATORS

Employing concentrators provides multiple advantages:

Improved network reliability: If a network contains only DAS nodes, connected on the dual ring, single failures will normally cause the ring to wrap, and subsequent failures will segment the ring. Since a concentrator can bypass any number of its drops, it makes the ring tolerant to a larger number of failures. This higher reliability makes large FDDI networks more practical.

Simplicity of wiring: Connectivity between a concentrator and SAS attachments matches normal wiring topologies. Most facilities planners wire buildings in star or star-of-stars fashion rather than in rings. Concentrators allow them to install dual fiber cables between offices and wiring closets, making it easy to add, remove or power down nodes on a network with minimal disturbance to other users.

More compact desktop workstations: Manufacturers constantly sustain pressure to reduce the footprint of their desktop workstations. Concentrators, by providing connectivity to SAS nodes, reduce the logic and power requirements of workstations which, in turn, reduces their footprint.

CONCENTRATOR CONFIGURATIONS

The FDDI Station Management (SMT) standard defines the Concentrator Configuration Element (CCE), the interconnection mechanism between individual PHYs and Paths *(Figure 1).* Each CCE connects to an individual PHY and one or more paths. The standard requires the Primary Path, allowing the Secondary and Local Paths as optional. The PHYs attached to the CCEs can be:

PHY M: A master port which supports connection and bypass of nodes.

PHY A and PHY B: Ports used for connection to a dual ring.

PHY S: A slave port used for connection to a master port of a concentrator. A slave can be either a single attachment station or a single attachment concentrator.

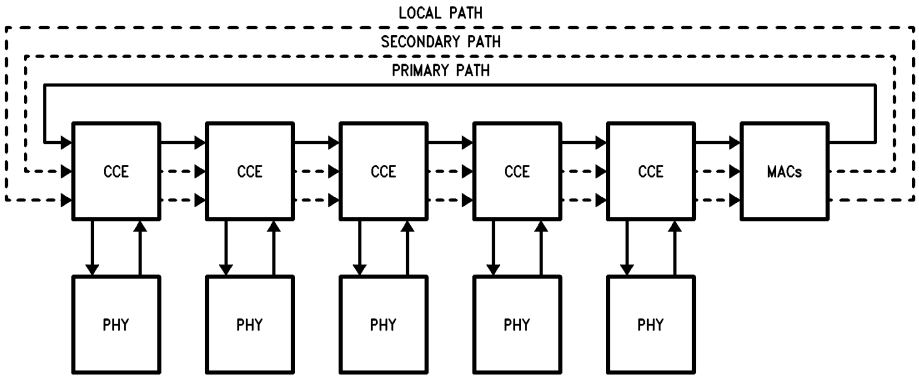

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FIGURE 1. The Concentrator Configuration Element (CCE)

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The general architecture supports many configurations, as indicated by the following examples:

1. A null MAC single attachment concentrator with master ports connecting onto the primary ring *(Figure 2).*
2. Single MAC single attachment concentrator or single MAC dual attachment concentrator with all master ports on the primary ring *(Figure 3).*
3. Single MAC dual attachment concentrator with all master ports switchable to either the primary ring or the secondary ring *(Figure 4).* This allows the attached nodes to participate on one of the rings. In the figure the master ports are shown switched to the secondary ring.
4. Dual MAC dual attachment concentrator with master ports individually switchable to either the primary ring or the secondary ring *(Figure 5).* This example places MACs on the exit ports of the primary and secondary rings.
5. Dual MAC dual attachment concentrator with master ports individually switchable to either ring or to the local path which also has a MAC *(Figure 6).* The local MAC, sometimes called a roving MAC, allows communication between the concentrator and nodes attached to individual master ports before inserting them into the network.

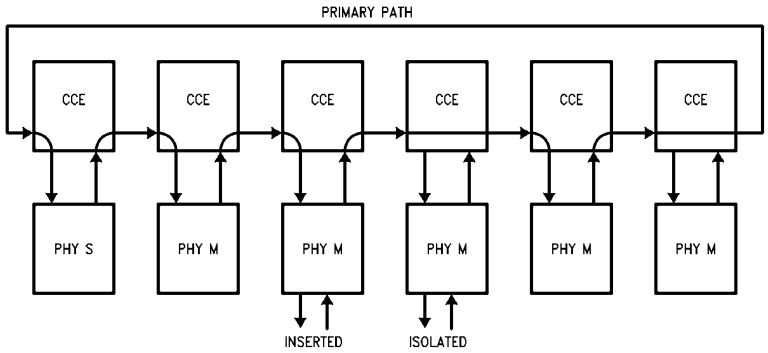

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FIGURE 2. A Null MAC Concentrator

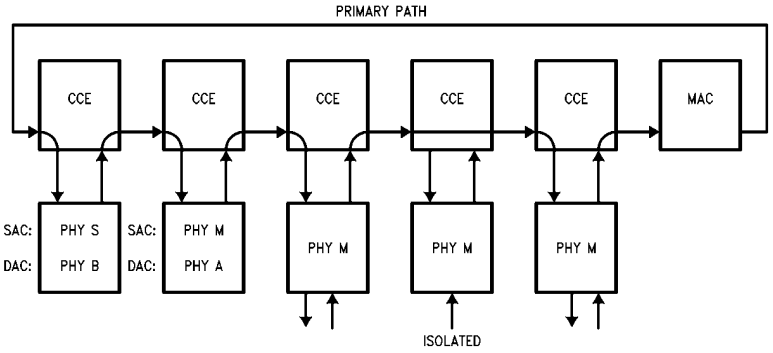

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FIGURE 3. Single MAC Single Attachment Concentrator

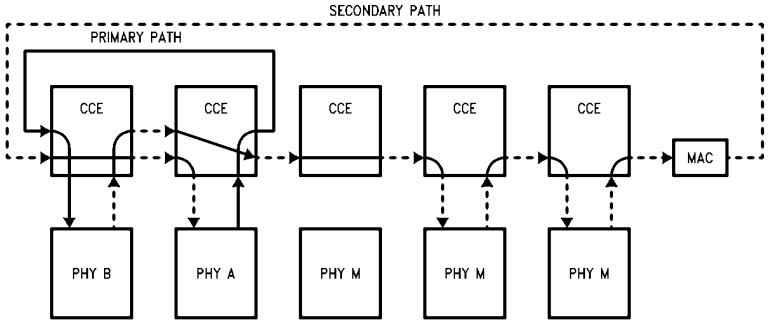

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FIGURE 4. Single MAC Dual Attachment Concentrator

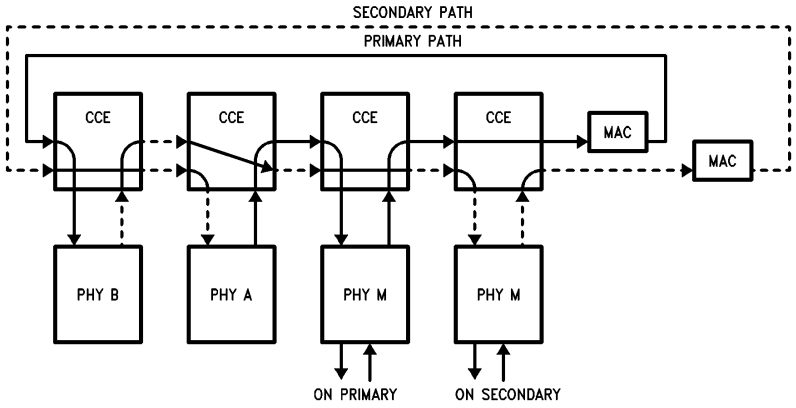

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FIGURE 5. Dual MAC Dual Attachment Concentrator

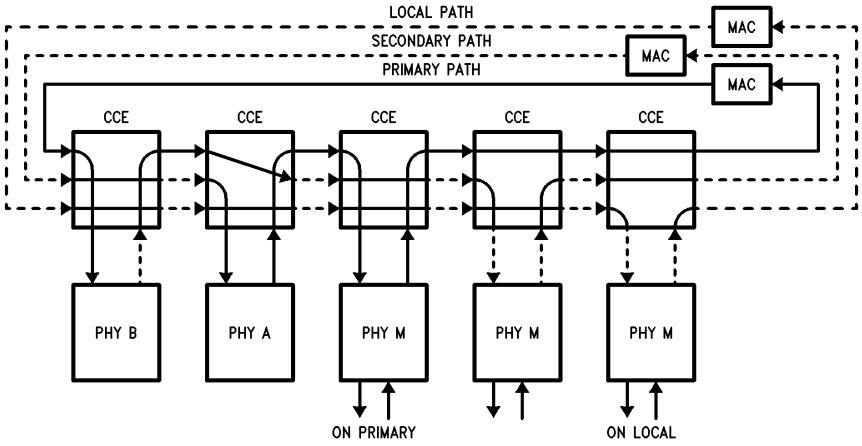

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FIGURE 6. Dual Attachment Concentrator with Local MAC

BUILDING CONCENTRATORS WITH NATIONAL'S CHIPS

The National Semiconductor FDDI chip set supports various types of concentrators. The DP83251/55 Physical Layer Controller (PLAYER™ device) implements the Physical Layer (PHY) of FDDI. The PLAYER device interfaces to the Basic Media Access Controller (BMAC™ device) and other PLAYER devices through two full duplex parallel ports, PORTA and PORTB. The DP83251, with just a single port, provides a more economical solution for single attachment stations and certain concentrator configurations.

The PLAYER device's Configuration Switch provides the flexibility to implement most concentrator configurations without any additional external data path logic. Roving MAC configurations require only minimal external logic, consisting of two-way MUXes and registers. National Semiconductor's BiCMOS technology minimizes the PLAYER device real estate, cost, and power dissipation, making these chips ideal for concentrator applications.

National Semiconductor's FDDI chip set directly supports SMT protocols, eliminating the external ''glue'' otherwise required for this function.

CONCENTRATOR EXAMPLES

The following examples illustrate the simplicity of building concentrators with the National chip set. The figures show the data paths connecting the PLAYER and BMAC chips. Where a PLAYER device is shown, the implementation will also include a DP83231 Clock Recovery Device (CRD™ device) and the fiber optic transceivers. *Figures 7–11* do not show the clocking structure, which depends upon the size of the concentrator. The DP83241 Clock Distribution Device (CCD™ device), discussed later in this application note, simplifies the clocking regardless of functionality or size.

A null MAC concentrator, previously shown in *Figure 2,* employs DP83251 PLAYER chips *(Figure 7).* Adding a MAC to this minimal design *(Figure 8)* creates the hardware necessary for either a single MAC single attachment or single MAC dual attachment concentrator that inserts all master ports in the primary ring as shown in *Figure 3.* The MAC includes the DP83261 BMAC device, buffer memory and a processor. This configuration requires no glue logic between any of the FDDI chips, nor does it need external hardware for SMT support. The fiber optic connector receptacle

keying and the Connection Management protocols executed while connecting to the network distinguish the two concentrator types which this basic design supports.

Figure 9 illustrates an implementation of the single MAC dual attachment concentrator described in *Figure 4.* The DP83255 PLAYER chips replace the DP83251 PLAYER chips for the PHYA and PHYB connections.

Figure 10 shows a dual MAC dual attachment concentrator with the master ports individually switchable to either ring. This requires DP83255 PLAYER chips on all master ports, but again, no additional glue logic is required.

Figure 11 shows the addition of a third ''roving'' MAC that the local bus can connect to any port without disturbing the network. As illustrated, this configuration requires an external 10-input, 2 x 2 crossbar to augment the DP83255s internal configuration switch. A register on the second output of the crossbar avoids improper stacking of propagation delays in the local path. The implementation of each crossbar requires only a pair of PALs.

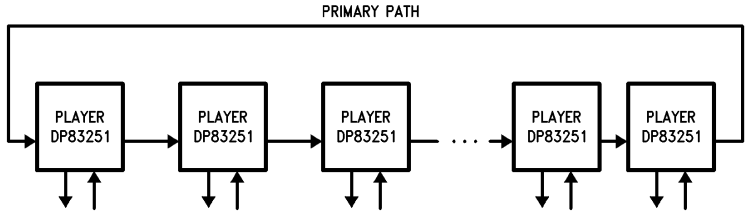

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FIGURE 7. A Null MAC Concentrator Using National's FDDI Chips

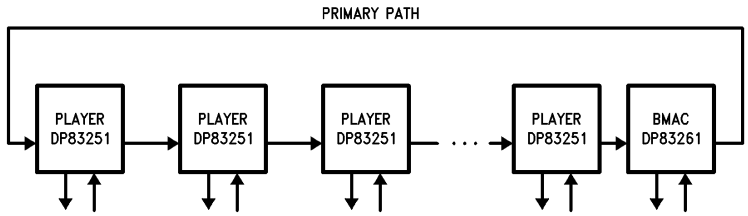

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FIGURE 8. Single MAC Single Attachment Concentrator Using National's FDDI Chips

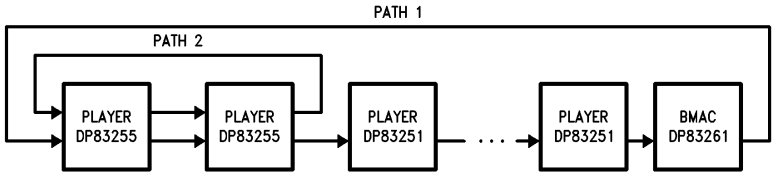

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FIGURE 9. Single MAC Dual Attachment Concentrator Using National's FDDI Chips

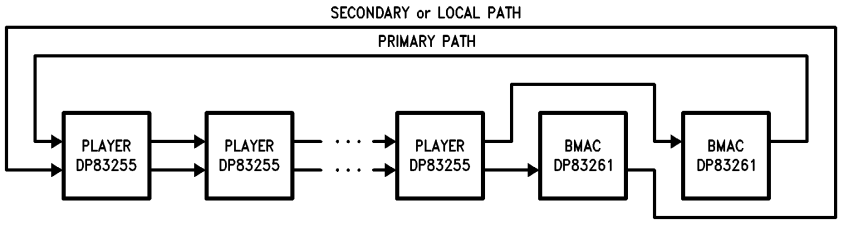

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FIGURE 10. Dual MAC Dual Attachment Concentrator Using National's FDDI Chips

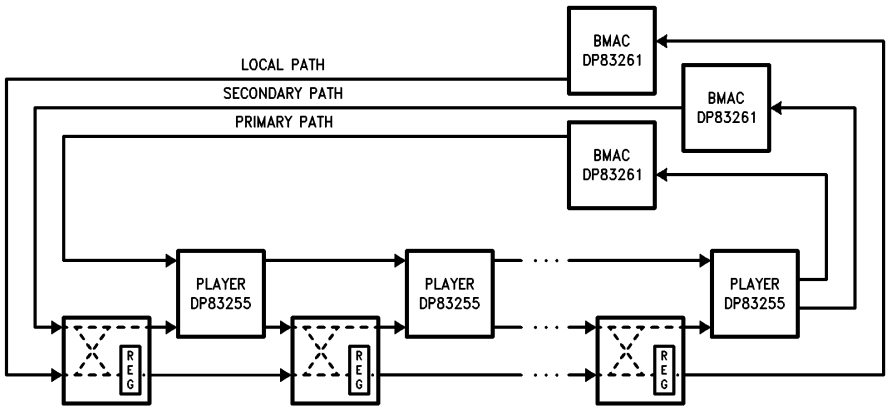

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FIGURE 11. Local MAC Concentrator Using National's FDDI Chips

STATION MANAGEMENT FOR CONCENTRATORS

As indicated above, the National Semiconductor chip set does away with the need for external logic to support SMT. With the following partitioning, a single local processor can execute SMT software for all but the most elaborate configurations:

PHY: Each PLAYER device requires its own separate processes for Physical Connection Management (PCM) and Link Error Monitoring (LEM). The very largest configurations may require one processor for each N PLAYER devices to satisfy PCM's PC__React time. No external hardware is required because the line state history register and the link error detector are contained within the PLAYER chip.

MAC: Each BMAC device requires its own Ring Management (RMT) process.

CONCENTRATOR: The configuration switch built into each PLAYER device fulfills SMT's Configuration Management (CFM) requirement except for roving MAC systems that require the external crossbars shown in *Figure 11.*

CONCENTRATOR CLOCKING STRUCTURE

Poor card layout or clock distribution can forfeit the low error rate benefits of FDDI's fiber optic links. The greater number of PHY elements in concentrators exacerbates any problems in these areas. National Semiconductor designed the DP83241 to simplify the clock distribution.

Concentrators have more stringent packaging demands than most end attachments due to environmental, modularity and reliability considerations. They may range from a single board desktop implementation with a small but fixed number of master ports to large, modular designs that support hot insertion and removal of master port cards. Though systems at these two extremes require different clocking structures, the DP83241 Clock Distribution Device provides reliable solutions.

The DP83261 BMAC and the DP83251/55 PLAYER devices require a 12.5 MHz TTL clock for internal operation and communication between one another. The DP83251/55 PLAYER device also employs a 12.5 MHz ECL clock to drive the parallel to serial conversion in the transmitter and a 125 MHz ECL clock to shift each bit out of the transmitter. The PLAYER device imposes specific timing relationships among these clocks, with relatively tight tolerances between the two ECL clocks and substantially relaxed tolerance between the two 12.5 MHz clocks.

The CDD device guarantees the relationships of the ECL and TTL clocks that it generates to significantly tighter tolerances than the PLAYER chips require. A concentrator clocking structure must distribute and deliver these signals without introducing more skew than the PLAYER chips can accept.

Figure 12 shows the simplest concentrator clocking structure, suitable for small systems, in which the CDD device directly drives all the clocks. The delays for all clocks in this configuration come solely from capacitance and trace lengths. The TTL clock goes to the BMAC device, the buffer and processor interface logic and the PLAYER devices. The ECL clocks run from the CDD device to the PLAYER devices in differential pairs, thus minimizing the introduction of noise and skew. The prudent designer will obey the following check list:

1. Keep all clock lines as short as possible, lowering exposure to problems.
2. Match the trace lengths of all ECL signals to within 0.5″, eliminating one source of skew.
3. Keep the two traces of each pair close and parallel to each other, reducing noise susceptibility and skew.
4. Escort the pairs with ground traces along both sides, further reducing noise susceptibility and providing better control of the clock edges.

5. Minimize the number of layer changes of these signals to minimize spurious reflections.
6. Avoid stubs that cause reflections by running the traces through the destination pins to proper terminations in the characteristic impedance of the board. *Figures 13a* and *13b* illustrate the right and wrong way to avoid stubs at termination. When board space limitations do not permit elimination of stubs, limit them to a maximum of 0.5″.
7. Run the ECL signals above a virtual ground plane that does not carry any TTL current, eliminating a source of noise injection.

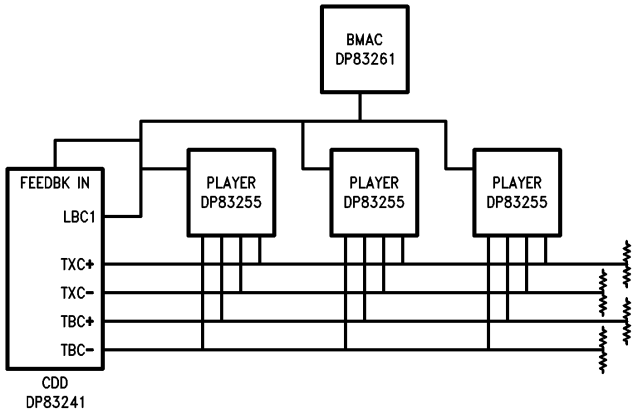

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FIGURE 12. Small Concentrator Clocking Structure

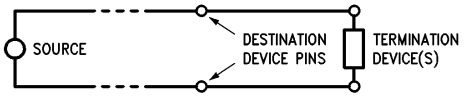

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FIGURE 13a. Proper Termination—No Stub

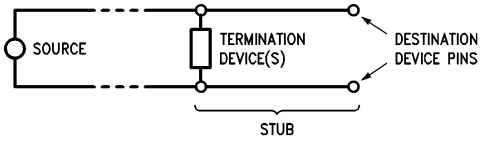

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FIGURE 13b. Improper Termination

Figure 14 shows a slightly larger concentrator clocking structure in which the fanout on the clocks exceeds what the CDD device can directly drive. A non-inverting buffer, such as a 74F08, drives the clocks. Feedback from the output of the driver into the CDD device allows it to compensate for the driver's delay. Skew calculations for this case must include the differential delay through the TTL clock buffers. The delay through the F100115 ECL clock driver chip will also contribute to the skew. Here, the wise designer will add another rule.

8. When distributing the clock through multiple buffers, keep the capacitative and resistive load on each buffer the same. Differing loads can cause differing delays and contribute to skew.

Figure 15 shows the clocking structure on a typical board of a multi-board system which supports field increases in the number of installed boards. This modularity requires a robust clocking structure to accommodate the greater distances between boards, the potential reflections introduced by the interconnection system, and the difference in delays found in components on different boards that come from different manufacturers or different lots, have a different aging history and are operating at different temperatures. The CDD device feedback mechanism allows it to accommodate these vagaries. A single clock source drives the feedback input of a CDD device located on each board. Each CDD device drives the PLAYER and BMAC devices on that board directly as shown in *Figure 12.* Larger board form factors that house more PLAYER or BMAC devices than the single CDD device can handle require additional DP83241s.

CONCLUSION

The Concentrator creates additional degrees of configuration freedom and greater reliability for FDDI networks. The National Semiconductor FDDI chip set provides the basis for robust concentrator designs that require virtually no glue.

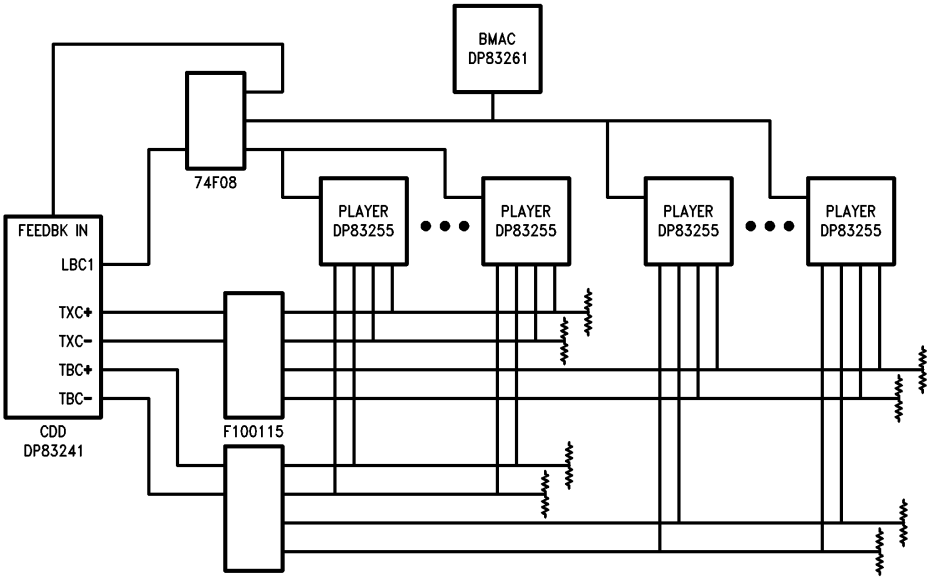

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FIGURE 14. Medium Size Concentrator Clocking Structure

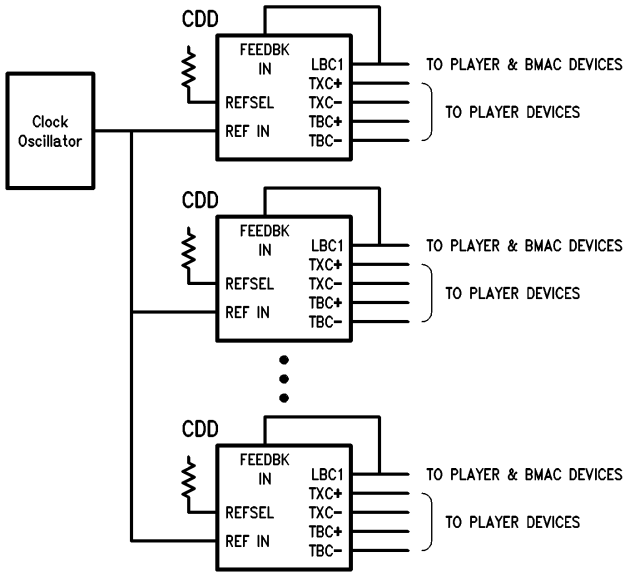

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FIGURE 15. Multi-Board Concentrator Clocking Structure

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