Universal UART PC-AT® Adapter

National Semiconductor
Application Note 692
Brett McCoy
July 1990

INTRODUCTION

The Universal UART PC-AT adapter allows its users to plug in any of National's AT compatible UART products for device testing, or serial/parallel communications. Applicable UARTs include the PC8250C (same as the INS8250, INS8250-B series), the PC8250A (same as the INS8250A, INS82C50A series), the PC16450C (same as NS16450, NS16C450 series), the PC16550C (same as the NS16550AF), and the PC16552C (same as the NS16C552 UART). The PC16451C (NS16C451) and PC16551C (NS16C551) High Integration Peripheral UARTs can be plugged into the board for device testing, or communications as well. This full sized AT board has 1 DIP and 2 PLCC device sockets, interrupt and DMA support logic, and can support all of the features provided by the devices listed above. Source and executable files of UART and parallel port test software are available through the electronic bulletin board on line access network at (408) 245-0671 (also see Appendix A). This document describes the functionality of the board on a level of detail to help users setup for quick and easy operation.

DESIGN CONSIDERATION

Simplicity and flexibility are the two major considerations in the design of the adapter card. A number of jumpers and switches are used instead of configuration registers to configure the board.

BLOCK DIAGRAM

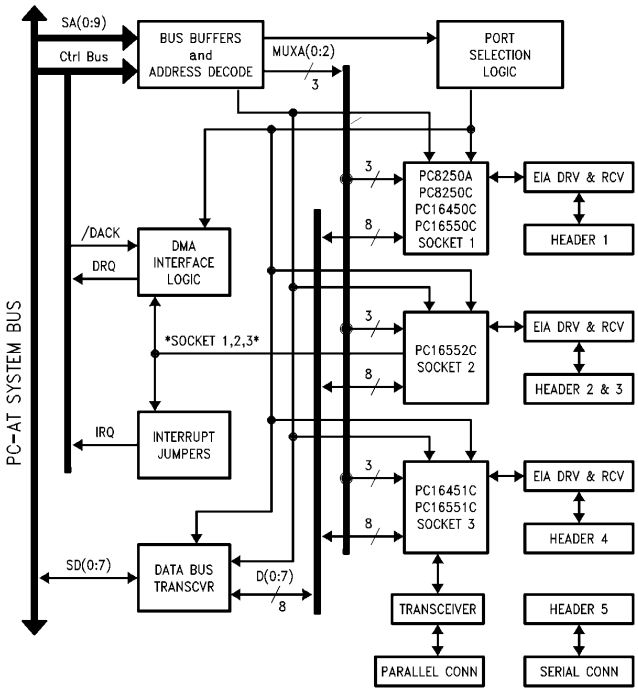
Three sockets are provided on the adapter to plug in all of the different UARTs and High Integration Peripherals. Socket 1 accepts the PC8250C, PC8250A, PC16450C, and the PC16550C, while socket 2 connects the PC16552C. Socket 3 accepts the PC16451C and PC16551C. Support logic on the adapter consists of the following major functional blocks:

1. Bus Buffers and Address Decode.
2. Port Selelction Logic.
3. DMA Interface Logic.
4. Interrupt Jumpers.
5. Data Bus Transceiver.
6. Device Sockets.
7. EIA Drivers and Receivers.
8. Headers and Serial/Parallel Connectors.

1.0 BUS BUFFERS AND ADDRESS DECODE

Two LS244s are used to buffer the system address and control bus signals for CPU read, write, and reset operations. The buffered address lines are gated by AEN and fed

Universal UART PC-AT Test Adapter Block Diagram



TL/F/10849–1

PC-AT® is a registered trademark of International Business Machines Corporation.

RRD-B30M75/Printed in U. S. A.

into two LS138 decoders to generate chip selects for 2 serial and 3 parallel port addresses. The port addresses map into the standard PC-AT serial/parallel I/O address spaces COM1 (3F8–3FF), COM2 (2F8–2FF), LPT1 (3BC–3BE), LPT2 (378–37A), and LPT3 (278–27A). The decoded chip selects are routed into the Port Selection Logic which either routes or blocks the chip select depending on which UARTs are enabled.

2.0 PORT SELECTION LOGIC

The Port Selection Logic consists of all the switches (SW1–SW8), gates, and LEDs (S1COM1, S1COM, etc. …) used to select and indicate the active UARTs and ports. Tables I and II below will help to configure the adapter for easy operation. SW1–SW6 are used to select COM1 and COM2 addresses for all three devices, hence there are two switches per socket. SW7, SW8 are used to select the LPT1, LPT2, LPT3 addresses for socket 3 only, the High Integration Peripheral socket with parallel ports. When using the internal decoder of the PC16551C, the adapter must still be configured to provide chip selects to the device, because the CPU data bus transceiver is enabled by chip selects.

TABLE I

Switch	Position	Socket	Port	LED
SW1	OFF	1	COM1	S1COM1 GREEN
SW2	OFF	1	COM2	S1COM2 RED
SW3	OFF	2	COM1	S2COM1 GREEN
SW4	OFF	2	COM2	S2COM2 RED
SW5	OFF	3	COM1	S3COM1 GREEN
SW6	OFF	3	COM2	S3COM2 RED

Note: If a switch is in the **ON** position, the corresponding port is disabled, and the LED will turn off. Make sure to enable only 1 COM1 port and 1 COM2 port at any given time, or device contention will occur.

TABLE II

Switch			LED	
SW8	SW7	Parallel Port	LPTB	LPTA
ON	ON	LPT1	OFF	OFF
ON	OFF	LPT2	OFF	ON
OFF	ON	LPT3	ON	OFF
OFF	OFF	DISABLED	ON	ON

3.0 DMA INTERFACE LOGIC

The adapter has logic to generate DMA requests from each socket and handle acknowledges when using COM1 (i.e., cannot do DMA transfers when a UART is setup for COM2). Three /TXRDY and three /RXRDY signals are ORed together to generate the DRQ1, DRQ3 signals respectively. The requests are only passed to the DMA controller when SW1, SW3, or SW5 are switched off to activate a COM port. When the request is acknowledged, /DACK1 or /DACK3 is used as a chip select to the requesting device to start the DMA cycle. /DACK also enables the data bus transceiver and selects the grounded inputs of the LS157 address multiplexer to access the UART data registers or FIFOs at address 0.

4.0 INTERRUPT JUMPERS

Jumpers are provided to connect the device interrupt request lines to the serial bus request lines IRQ3, IRQ4, and the parallel request channels IRQ5, IRQ7. The interrupt jumpers are designed for maximum flexibility, but the user must obey a few basic rules. Make sure the jumpers are configured to match what the interrupt controller of your system is programmed for by the software. Also, it is best not to connect multiple devices on the adapter to one IRQ channel. Table III contains the interrupt jumper options.

TABLE III

Jumper	Interrupt Source	IRQ to CPU	Note
J11	Socket 3, IRQ4	4	INTS for 451
J12	Socket 3, IRQ4	3	INTS for 451
J13	Socket 3, IRQ3	4	451 V_{SS} Pin
J14	Socket 3, IRQ3	3	451 V_{SS} Pin
J15	Socket 2, INTR2	4	
J16	Socket 2, INTR2	3	
J17	Socket 2, INTR1	4	
J18	Socket 2, INTR1	3	
J19	Socket 3, IRQ3	(See Schem.)	IRQ/GND Strap
J27	Socket 3, IRQ7	7	INTP for 451
J28	Socket 3, IRQ5	5	NC for 451
J29	Socket 1, INTR	4	
J30	Socket 1, INTR	3	

4.1 Interrupt Jumper Configuration Example

To illustrate an example configuration, consider the following hypothetical scenario. Let's say we want to use National's FACT.C software to do full duplex asynchronous communications testing with FIFOs between two PC-ATs that each have a UART/AT adapter. Machine 1 has a PC16550C in socket 1 with SW1 in the off position (COM1 is activated), and it has a PC16451C in socket 3 for printing. FACT.C programs the PC-AT's interrupt controller to receive interrupts through IRQ4 when COM1 is activated, and IRQ3 is programmed when COM2 is activated. The adapter in machine 1 should have J29 connected to link the PC16550C INTR line to IRQ4 of the CPU, and J27 should be connected to link the PC16451C INTP line to IRQ7 of the CPU. If machine 2 has a PC16552C in socket 2 with SW4 in the off position (COM2 is activated), J16 should be connected to link the INTR2 line to IRQ3 of the CPU.

5.0 DATA BUS TRANSCEIVER

As mentioned before, the data bus transceiver is only enabled when chip selects are active, or when a DMA acknowledge arrives. When using the on board decoder for the PC16551C serial port, the serial chip select line on the chip should be tied to ground rather than decoded to prevent switching of the IRQ lines. Even though the chip select signal from the external decoder does not reach the 551 in this case, the external decoder must still be activated to provide a chip select for the data bus transceiver.

6.0 SOCKET 1 (PC16450C, PC16550C)

Setup of socket 1 is easy. J1 connects power to the device, J6 connects to the 1.8432 MHz crystal, and J5 connects the chip to the crystal network. Do not connect J5 and J6 at the same time. Keep in mind the power jumpers can also be used for I_{CC} measurements.

6.1 Socket 2 (PC16552C)

Socket 2 is similar to socket 1 except the jumper numbers and different. J9 connects power, J8 connects to the 1.8432 MHz crystal, while J7 connects to the crystal network. Do not connect J7 and J8 at the same time.

6.2 Socket 3

Setup of socket 3 for use with the PC16451C or PC16551C requires more attention to detail. J10 connects power to the device, and the CLK input is connected directly to the 1.8432 MHz crystal. Beware of the caution below when configuring the card for use with the PC16451C.

6.2.1 PC16551C

When using the internal decoder of the PC16551C, all of the three prong jumpers J20–J26 should be tied with pin 1 connected to pin 2. J31 pin 2 should be tied to pin 3 (GND) when using the internal decoder. When using the external decoder, make sure to connect J31 pin 1 to pin 2, or else serial chip selects will not reach the device. J19 pin 1 must be tied to pin 2 if the IRQ3 pin is used on the device. Setup of SW9–SW12 is straightforward using Table IV and the 551 datasheet. The two switches adjacent to SW12 are spares, and they do not control any devices. Jumpers J2, J3, J4, J32, J33 should be configured according to Table V. J34 and J35 pin 1 should be tied to pin 2 when using the 551 parallel port.

TABLE IV

Switch	PC16551C Pin	switch on = logic 0, switch off = logic 1
SW9	/DCEN	Off: EXT Decode On: INT Decode
SW10	AEN	If SW9 is on, then SW10 should be on
SW11	/POS	On: Compatible Mode Off: EXT Mode
SW12	COM	On: COM2 Selected Off: COM1 Selected

TABLE V

Jumper	Notes
J2	XCVR DIR to GND. Data Read in Parallel Port.
J3	XCVR DIR to +5V. Data Written Out Parallel Port
J4	XCVR DIR Pin Connected to PC16551C PDIR Pin
J32	Pin 2 to Pin 3. Connects /TXRDY to DMA Logic
J33	Pin 2 to Pin 3 Connects /MF (RXRDY) to DMA Logic

6.2.2 PC16451C

The PC16451C and the PC16551C are socket compatible, but many of the pins with special functions on the PC16551C are V_{SS} or V_{DD} pins on the PC16451C. For J20–J26, J19, connect pin 2 to pin 3, and connect J31 pin 1 to pin 2. To configure the parallel port for output, turn SW11 on, remove J4 and J2, and connect J3. To configure the port for input, turn SW11 off, remove J3, and connect J2.

Caution
PC16451C Configuration

Pay careful attention to Table VI for the following jumpers and switches, because it would be very easy to connect one of the 451s V_{DD} pins to ground which would destroy the chip.

TABLE VI

Switch	Position	Jumper	Pins
SW9	Off	J34	2 to 3
SW10	On	J35	2 to 3
SW12	Off		

7.0 EIA DRIVERS AND RECEIVERS

EIA standard RS-232-C drivers and receivers handle the interface between the UARTs on the adapter card and the headers used to communicate to the external world.

8.0 HEADERS AND SERIAL/PARALLEL CONNECTORS

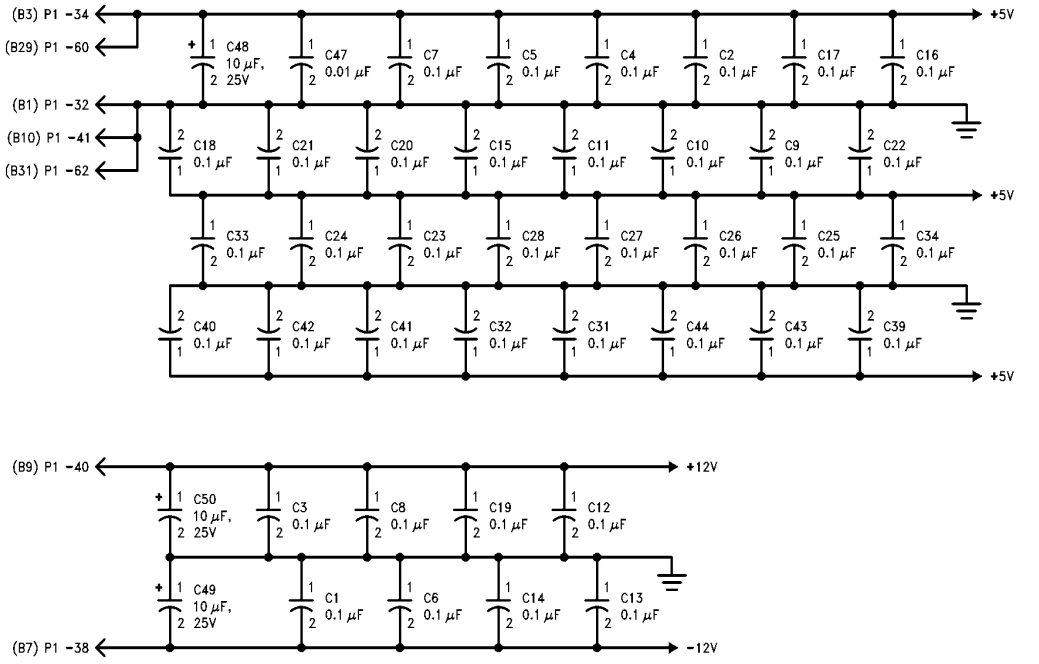
Since there are several UARTs on the adapter and only one 9 pin D type serial connector, 10 pin headers exist to connect for external communications. H1 is for socket 1, H2 and H3 are for socket 2, and H4 is for socket 3. For example, to connect PC16552C channel 1 to the outside world, simply connect a 10 pin jumper cable between H2 and H5. The header H5 is permanently connected to the 9 pin D serial connector. Device-to-device or channel-to-channel communication links can be formed by connecting a null modem jumper from one header to another. The 25 pin D connector is the parallel port of the adapter.

APPENDIX A: SOFTWARE SUPPORT

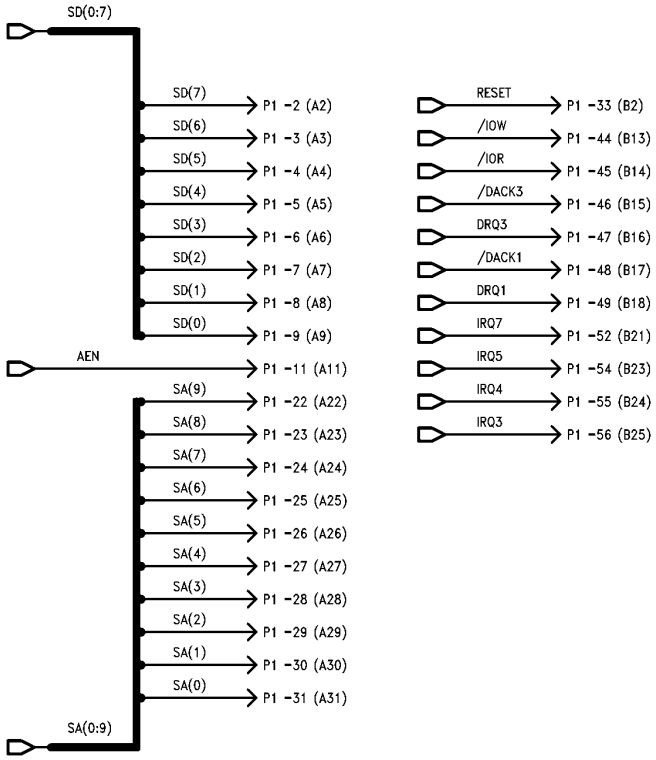
The programs mentioned in this application note are available on National's electronic bulletin board system. Provided by the PC Peripherals Applications Group, this system provides access to an automated information storage and retrieval system that may be accessed over standard telephone lines 24 hours a day at (408) 245-0671. The system's capabilities include a MESSAGE SECTION (electronic mail) for communicating to and from the PC Peripheral Applications group, and FILE SECTION that can be used to search out and retrieve application data about National's UARTs, High Integration Peripherals, and Floppy Disk Controller products. The minimum system requirement is: 1. A dumb terminal. 2. A 300 or 1200 baud modem. 3. A telephone. With a communication package and a PC, the files mentioned in this application note can be downloaded from the FILE SECTION to disk for later use. Table VII lists programs on the system that are applicable to the UART AT adapter.

TABLE VII

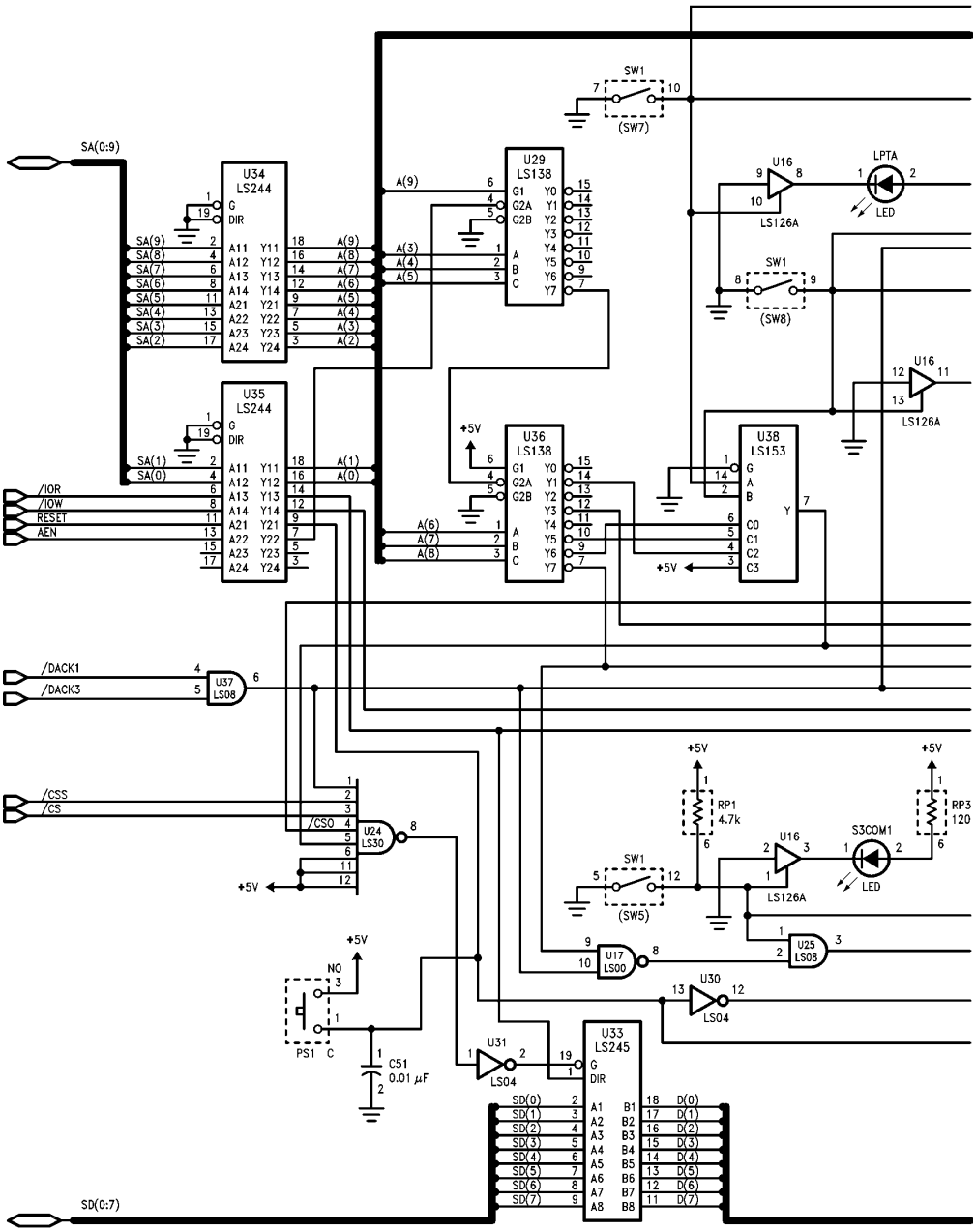
Source File Name	Function
551.ASM	PC16551C Parallel Port Test
ASCTEST.ASM	Full Duplex Async Comm Test
451.ASM	PC16451C Parallel Port Test
FACT.C	Full Duplex Async FIFO Mode Test
LBT.C	External Loopback Test. INT Driven
TOG1.ASM	Full Duplex Async Comm Test
COMTEST.C	Diagnostic Test for all UARTs



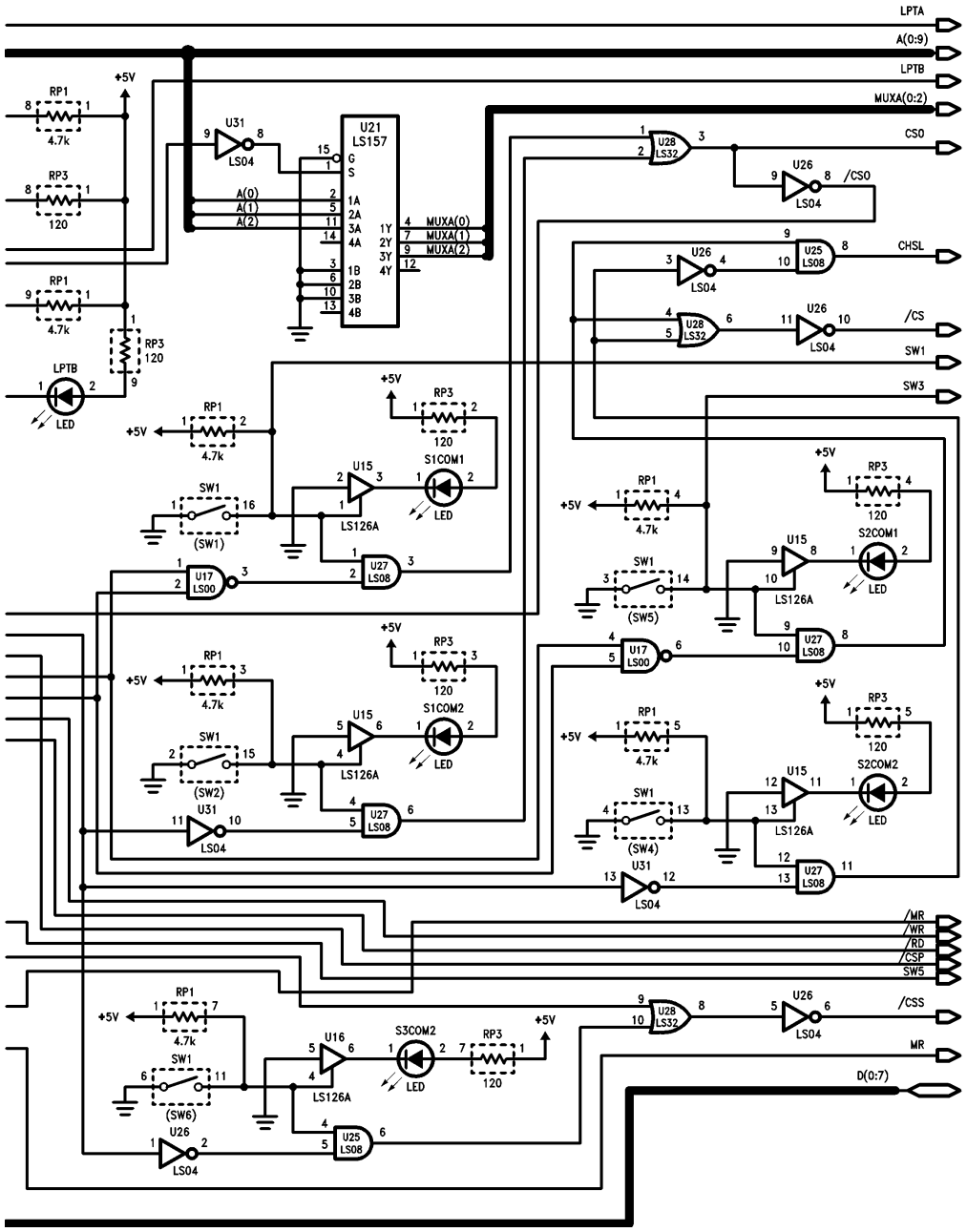
TL/F/10849–2



TL/F/10849–9

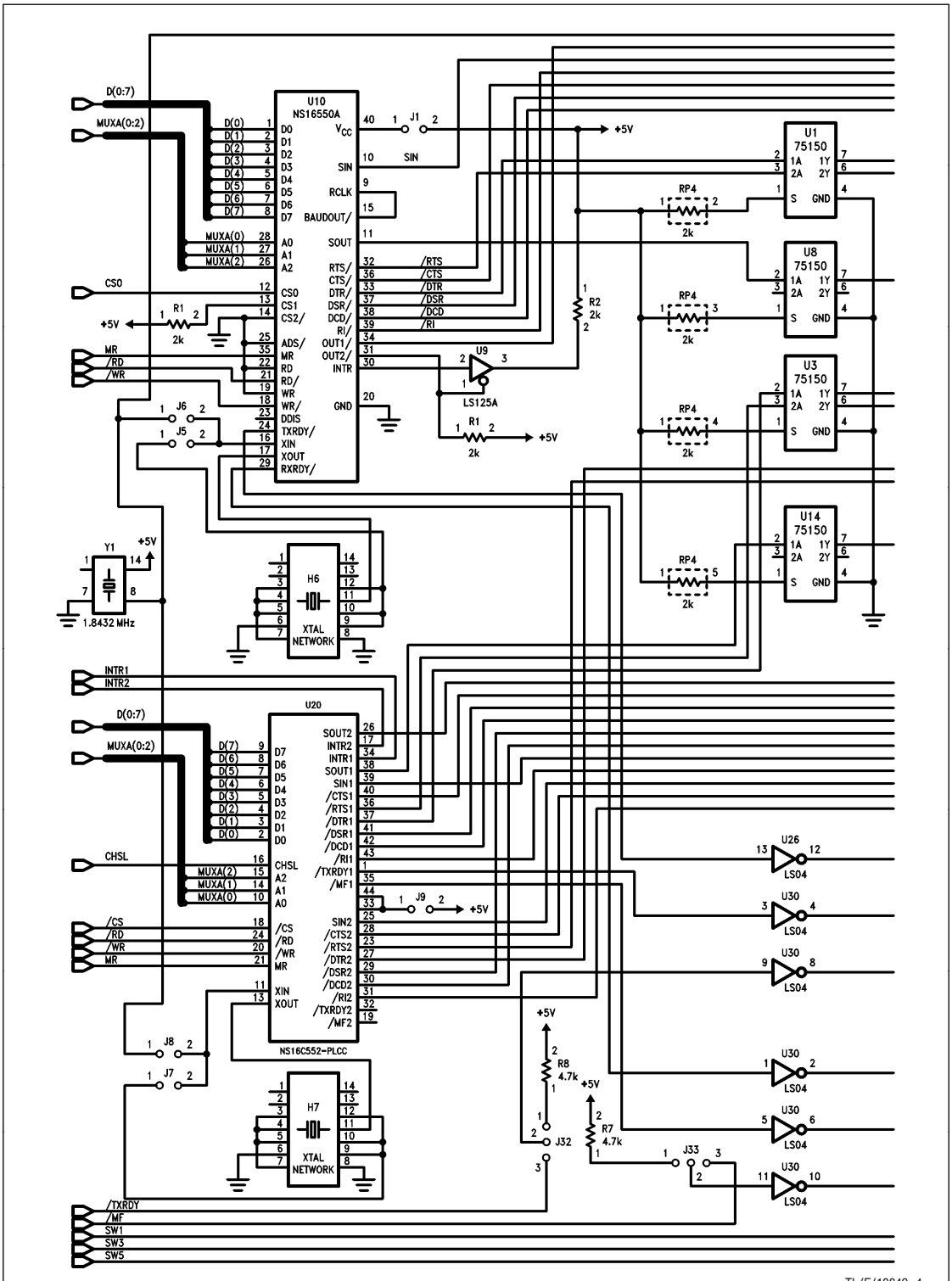

SA(0:9)
U34
LS244
U35
LS244
U29
LS138
U36
LS138
U38
LS153
SW1
(SW7)
SW1
(SW8)
SW1
(SW5)
U16
LS126A
LPTA
LED
S3COM1
/IOR
/IOW
RESET
AEN
/DACK1
/DACK3
U37
LS08
/CSS
/CS
/CS0
U24
LS30
+5V
RP1
4.7k
RP3
120
U17
LS00
U25
LS08
U30
LS04
U31
LS04
NO
PS1
C51
0.01 µF
U33
LS245
SD(0:7)
TL/F/10849–3

Sheet 1A



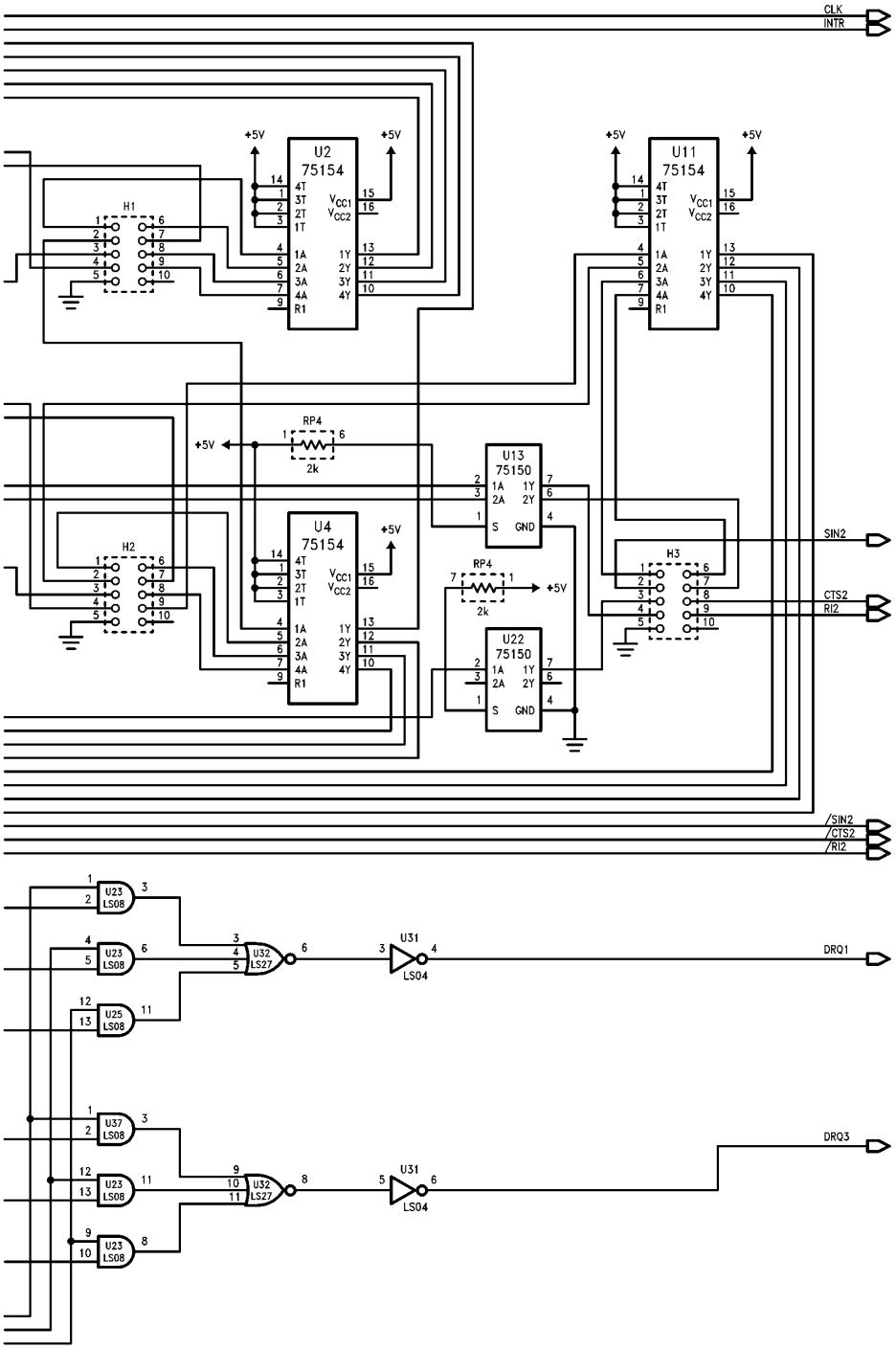
TL/F/10849–8

Sheet 1B



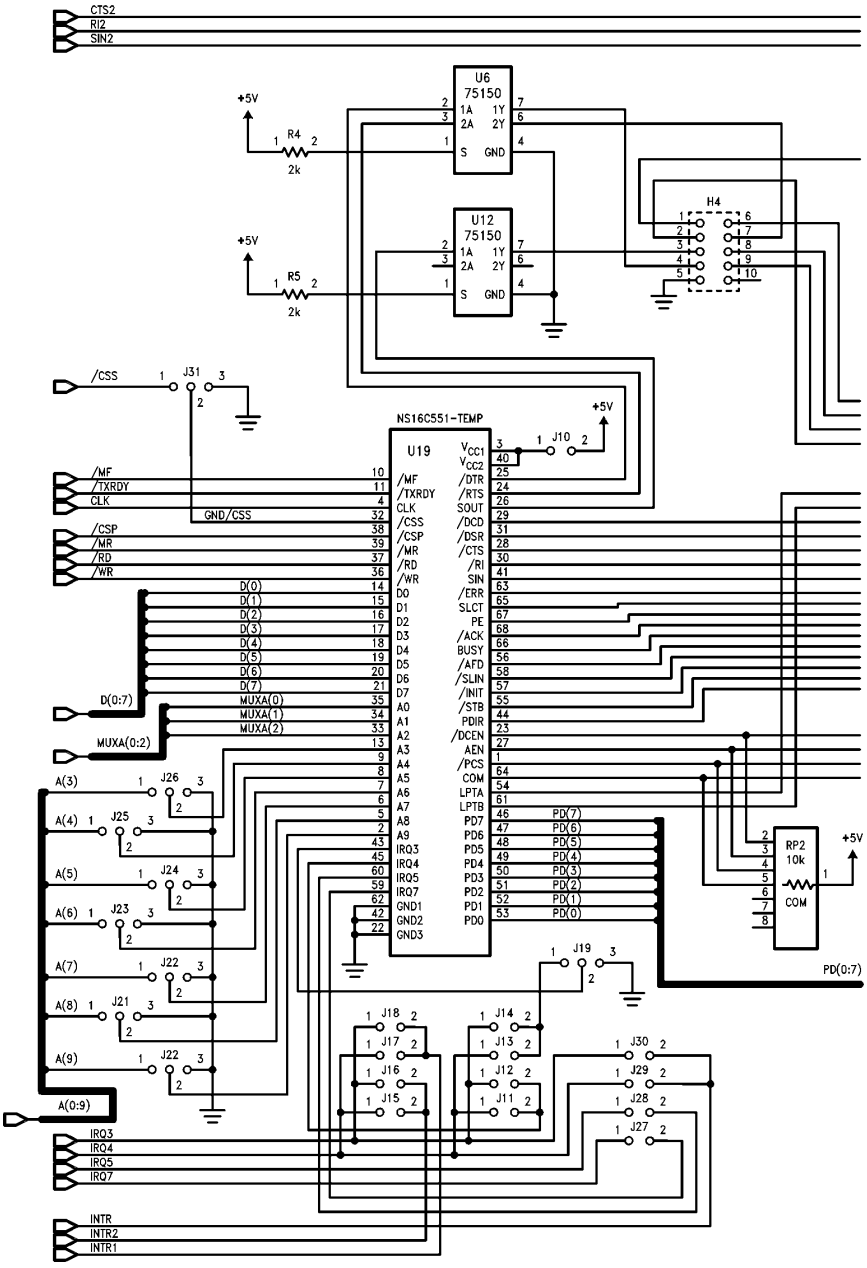
TL/F/10849–4

Sheet 2A



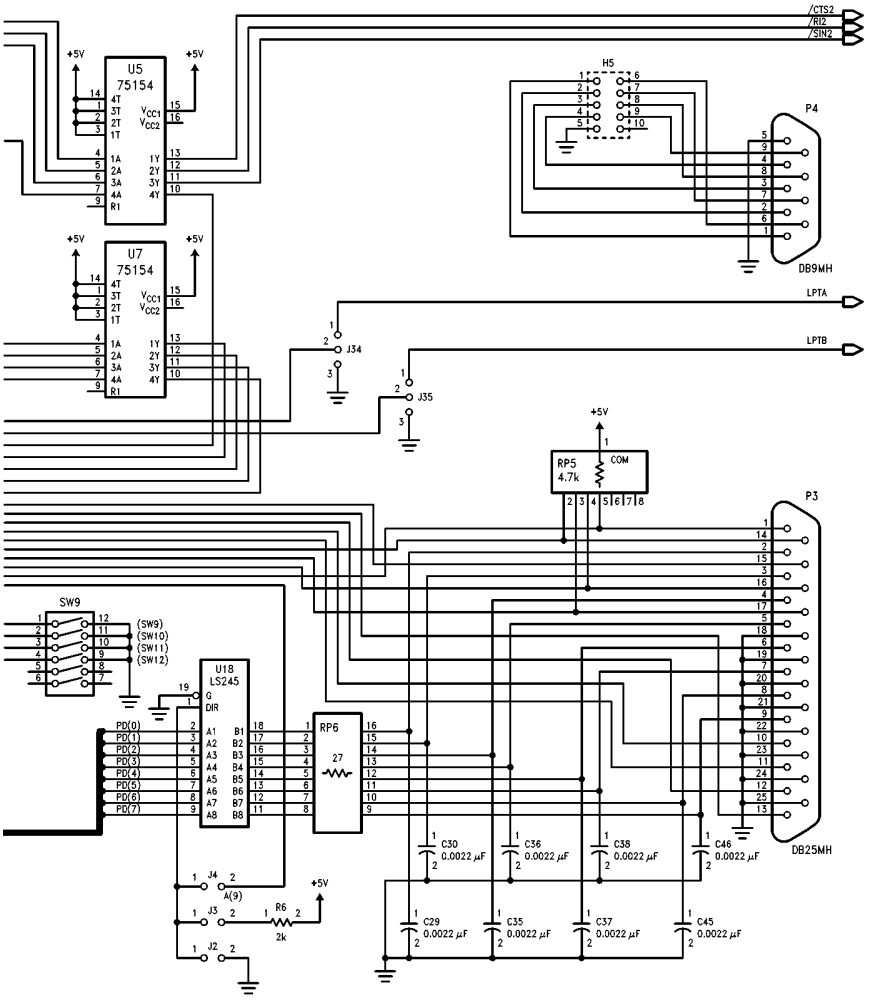
TL/F/10849–6

Sheet 2B



TL/F/10849–5

Sheet 3A



TL/F/10849–7

Sheet 3B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998