Build a Direction-Sensing Bidirectional Repeater

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When designing an EIA-485 control bus to link widely separated machinery and process controllers, devising a scheme to control the repeaters can be one of the more awkward tasks. In long buses, bus segments are joined with repeaters if the distance exceeds the maximum allowed by one cable segment.

Usually the buses are of a master-slave configuration—a bus network can consist of a master, two slaves, and two repeaters, for instance *(Figure 1)*. Amplifying control signals and making sure that they're clearly received by the slaves is one task performed by the repeaters. Repeaters can also increase the number of slaves per cable segment, extending the control bus's reach. To ensure that signals travel through repeaters correctly in both master-to-slave and slave-to-master directions, though, the repeaters must be switched.

Controlling the switching can be a cumbersome task. One way to handle it is to generate a repeater-reversing signal at the slave location and carry it over a dedicated control line to the repeaters. The catch is that the repeater control line needs to be very long—the length of the cable segment, in fact. Handling direction control remotely introduces delays and increases the possibility of errors. Ideally, control of the repeater switching would occur locally, at the repeaters themselves. Designers can achieve this local control and get rid of repeater lines by building a smart, direction-sensing repeater.

CONTROLLING REPEATERS

To see the advantages of direction-sensing repeaters, look at a design that uses repeater control lines *(Figure 2)*. Based on the repeater control circuit used by the Intel Bitbus, this design is for twisted-pair cable. (Sometimes ribbon cable can be used instead). The differential line drivers and receivers are designed for multipoint applications and meet the EIA-485 standard.

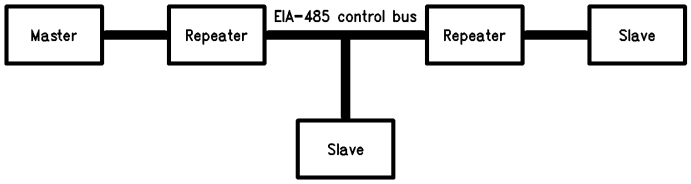

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FIGURE 1. Repeaters Extend the Length of the Twisted-Pair Bus by Transmitting the Signal on to the Next Cable Segment

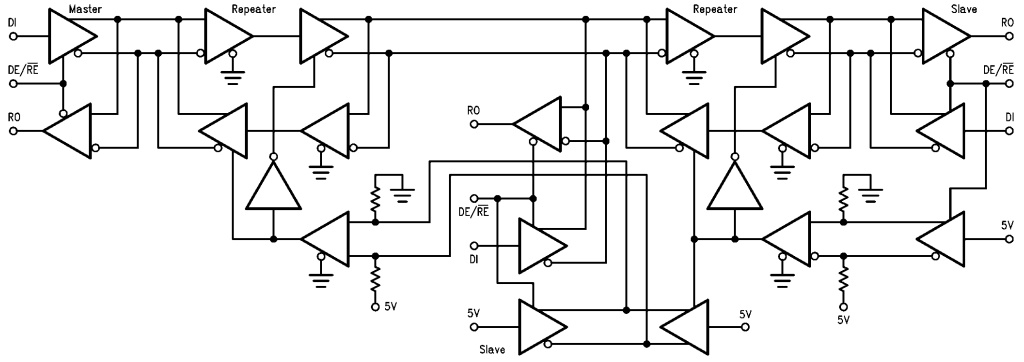

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FIGURE 2. Repeater Direction Can Be Switched from the Slave's End with a Biased Repeater-Control Line

Bias resistors on the control line typically enable the repeater in the direction away from the master. In this case, the master is the talker and the data flows in the master-to-slave direction. When a slave responds to a poll from the master, it drives its direction control line—DE/$\overline{RE}$—high. This drives the slave's repeater control line high, overriding the low state normally imposed by the bias resistors. The orientation of each repeater between the slave and the master is switched to the slave-to-master direction. All other repeaters stay enabled in the direction away from the master—letting slaves talk to any other slave, if the protocol allows it. The repeater control line is actively driven to only one state (high), so that if more than one slave tries to drive the control line at the same time, contention current is minimized.

Eliminating the repeater control line in the network greatly simplifies the circuit *(Figure 3)*. Here, a local data direction-sensing control circuit switches repeater direction. The circuit switches the repeater in the right direction by sensing which side of the data line is active first. If the master side is active first, the repeater is enabled in the master-to-slave direction, and vice versa. If the master and slave are active simultaneously, neither direction is enabled.

Two line-sense circuits work in the local control circuit. One monitors the master side of the data line, the other the slave side. The data line is active when driven to a differential high or low. The data line is inactive when all drivers connected to it are in TRI-STATE®. Resistors bias the sense circuit receiver inputs to produce high receiver outputs when the data line is inactive. When the data line is driven, the bias is overridden and the receivers respond to the signals on the data line. One output switches to the same state as the data line, and the other output switches to the complementary state. An active line sends complementary inputs to the AND gate and switches the sense circuit output low. An inactive data line produces high inputs to the AND gate (because of the resistor bias) and switches the output high. Data direction is determined by detecting which sense-circuit output (master or slave) goes low first.

The direction-sensing repeater design divides into six functional blocks *(Figure 4)*. The first block—block a—is a bidirectional repeater. Block b senses the state of the data line on each side of the repeater. It checks for either a driven state (active) or a high impedance state (inactive). Block c determines the enable signals according to the line states. Block d generates pulses used for masking, clocking, and error signals. Block e filters, generates a pulse, and detects a valid line state change. Block f latches in the most current line state information and generates the enable signals to the repeaters.

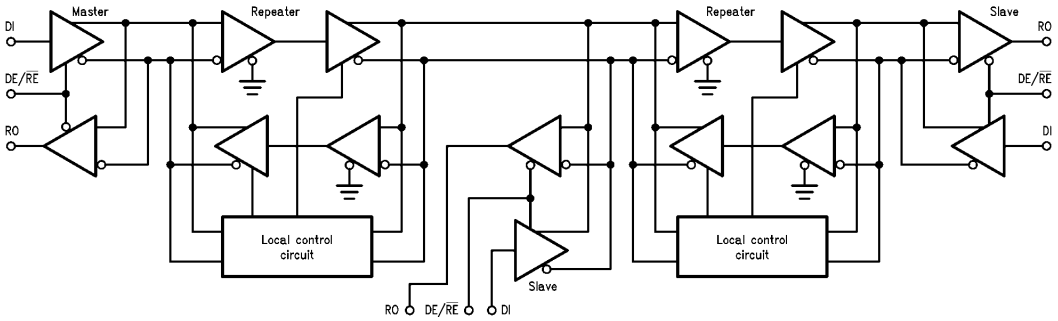

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FIGURE 3. Switching Repeater Direction Locally Avoids a Cumbersome and Costly Repeater Control Line

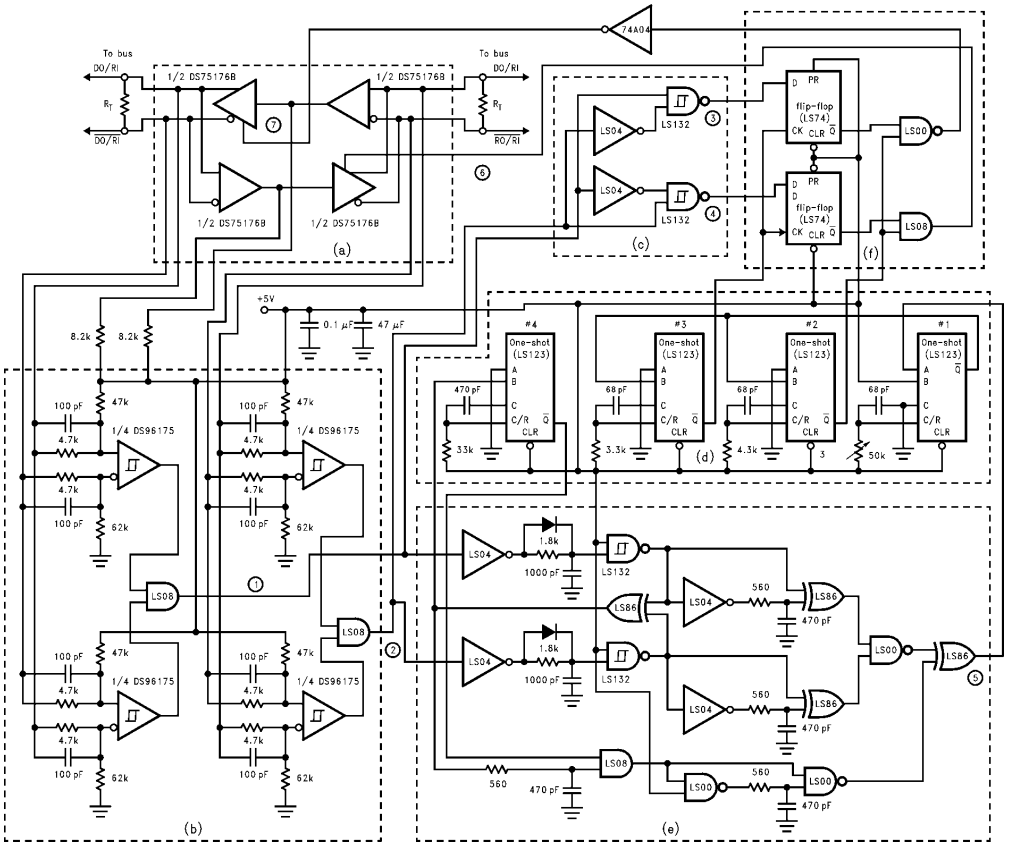

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FIGURE 4. Direction-Sensing Circuity Switches the Repeater in the Direction that Data Is Being Transmitted

The bidirectional repeater consists of two standard-pinout EIA-485 transceivers. The inverter inverts the enable line on one of the transceivers, so that two standard transceivers can be used. The ''active-low'' receiver enables are permanently enabled by hard-wiring them to ground. The driver enables are set by the output of the LS00 and LS08 gates. Data lines must be terminated on each side of the repeater to bias the line for the line-sense circuits. The termination resistor should be selected to match the transmission line's characteristic impedance—100Ω to 120Ω is typical for twisted pair.

In block b, an EIA-485 quad receiver senses the line to determine whether it's active or inactive. Each receiver pair monitors one side of the transmission line. The quad receiver's enable should be hard-wired ON. Resistors bias the receiver input to a positive differential voltage that produces a high ouptut when all drivers are in TRI-STATE mode. The receiver outputs are combined with an AND gate. A falling edge at the AND gate output indicates an active line, and a rising edge indicates a return to the Z line state.

The logic in block c—standard gates and the LS132 NAND gate—prevents the repeater from being enabled in case of collision. If both data lines become active at the same time, logic will disable transmission in both directions. In addition to the NAND function, the LS132 gate's inputs have hysteresis to increase noise immunity. This yields a jitter-free output from a slow input signal.

When drivers on each side of the repeater drive the line simultaneously, a collision occurs. To prevent this, the logic in block c keeps both repeater drivers off until the lines on both sides have returned to the inactive state. When a collision occurs, a low appears at signal locations 1 and 2. The logic sets the D flip-flop inputs high, however, so repeater disables—instead of enables—are generated.

When signals 1 and 2 are high, the D flip-flop inputs are high, and both repeater drivers are disabled. If either 1 or 2 is low while the other is high, an enable signal travels to one of the repeater drivers, depending upon which line is low. A valid line state change causes block d to generate a clock pulse that will latch the D flip-flops. After the repeater has turned on, signals 1 and 2 go low, since data is passing through the repeater. Because data transitions don't change the line state—it stays active—no new clock pulse is generated and the enables aren't updated.

TRIGGERING ONE-SHOTS

Block d includes four retriggerable LS123 one-shots for timing functions. The first one-shot is triggered when a valid line state change is detected. Its output trips the second and third one-shots on the same edge. The second one-shot's output is used as an enable mask, while the output of the third generates the clock pulse that latches in the latest enable bits. The fourth one-shot senses errors. It is activated when a collision occurs.

The one-shot's output pulse widths are set by external capacitors and resistors. Standard 74123 one-shots shouldn't be substituted for the LS123 devices, because the LS123 IC's clear pin is also a trigger. Also, the resistor and capacitor should be as close to the device pins as possible, to minimize stray capacitance and noise pickup. In this application, these can affect the one-shots' time constants.

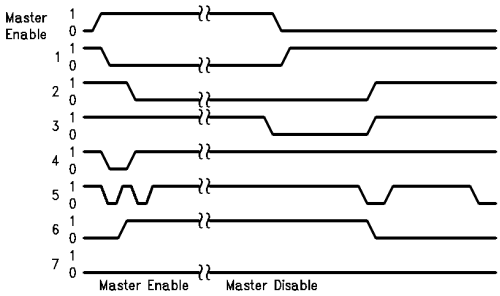
The first one-shot's resistor value is adjustable with a 50K trim pot to adjust the output pulse width. This one-shot is triggered on power-up, or by a valid line state change. Its output triggers the next two one-shots. The one-shot's output pulse is set wide enough to mask out the second pulse, caused when the data line on the other side of the repeater becomes active. When one side becomes active, a pulse is genered at point 5, triggering the first one-shot. When the repeater is enabled, the repeater drives the other side of the line. The newly active side of the line generates a second pulse, as it has changed from inactive to active. The second pulse at point 5 retriggers the first one-shot, preventing a new clock pulse. Consequently, the second and third one-shots aren't triggered.

The output of the second one-shot disables both repeater enable lines for about 200 ns. This disable inserts a minimum inactive state between every repeater direction switch, preventing it from toggling. After the minimum interval, however, the repeater can change direction. The third one-shot generates the D flip-flop clock pulse upon a valid line state change. The fourth one-shot sends an error signal to disable the repeater. The error occurs when the repeater isn't enabled between the time that one side of the transmission line becomes active and the time the other side becomes active. This scenario is also a collision, and is related to the propagation delay of the local control circuit. In this case, the enables to the repeater are kept off.

Block e filters and converts a valid line state change into a pulse, which triggers the first one-shot. The first low-pass filter cleans up spikes from the output of the line-sense circuits. Spikes appear from the difference in switching thresholds between receivers in the sense circuit. For a short time, receiver outputs are in the same state, causing a glitch at points 1 and 2 on every other signal transition. The width of the spikes depends on the data line signal transition time. For a short line, the data line capacitance is small, the signal transitions are fast, and the pulses out of the LS08 are very narrow. In most applications, though, the data line between repeaters is long, so transition time is much slower. In this case, the pulses at the LS08 output are wider. These pulses must be filtered out before they mislead the repeater into switching direction.

The first low-pass filter performs this function, with component values for a repeater linking two 1000-meter cable segments and a data rate of 200 kbaud. This filter also controls the length of time required to enable and disable the repeater. The difference between these two times is the delay of the low-pass filter. The enable time—375 ns from LS04 output to LS132 output—is shorter than the disable time—about 3.5 μs—because during enable, the capacitor charges through the diode *(Figure 5)*.

The final block masks the enable bits to the repeater when the second one-shot is triggered by the first. A latch holds the repeater direction enable bits when a valid line change has occurred. The enable lines are automatically masked for 200 ns, guaranteeing return to the inactive state and disabling the repeater when the D flip-flops are changing states.



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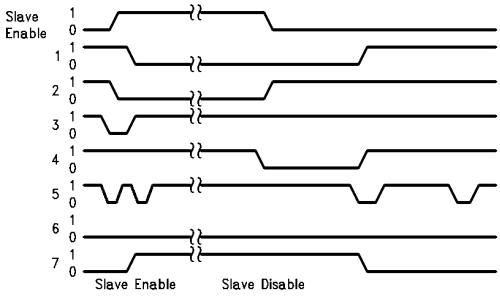

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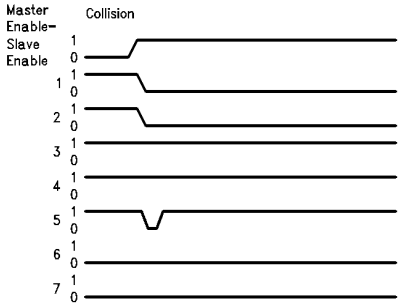

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FIGURE 5. Signals at different points in the circuit vary according to the data line conditions. There are five possible cases: Master Enable, Master Disable, Slave Enable, Slave Disable, and Collision (master and slave attempting to enable simultaneously).

To understand the timing in the master enable case, assume the master is located on the left side of the repeater and the slave on the right (*Figure 4,* again). First, both lines on either side of the repeater are inactive. The line-sense circuit outputs are high and Enables 6 and 7 are low. Next, the master drives the line high. The rising-edge line ME is the driving master's enable line. As soon as the master drives the line high, the sense circuit on the master side detects an active line state. The output of the LS08 gate pulls low, indicating the inactive-to-active state change. Lines 3 and 4 show the D flip-flop input signals. When 4 is low, the repeater is enabled in the master-to-slave direction.

On line 5, two pulses appear. The first occurs when the master side of the line changes from inactive to active. The first one-shot is triggered, generating a clock pulse. The D flip-flop latches its inputs and one repeater driver is enabled. Line 7 stays low, disabling the repeater in the direction towards the master. Line 6 becomes enabled, as a result of the master side becoming active first. The pulse created when the slave side becomes active is the second pulse on line 5. The second pulse doesn't generate a clock pulse; it retriggers the first one-shot. This one-shot can be adjusted so that the second pulse occurs within the output pulse of the first trigger. This guarantees that a new clock pulse won't be generated and keeps the repeater enabled in the same direction.

When the master has completed transmission, it is disabled and lets go of the line. The line-sense circuit detects the state change, data is latched into the D flip-flops, and enable lines 6 and 7 are pulled low.

In the slave enable case the same timing cycle takes place, with the roles of sense lines 1 and 2 and enable lines 6 and 7 reversed. When collision occurs, lines 3 and 4 stay high and neither direction is enabled. The line-sense circuits on both sides of the repeater detect a state change—from inactive to active—upon collision. The logic in block c, however, keeps the repeater disabled. The second pulse usually seen on line 5 doesn't occur, because the repeater is disabled in both directions. Both sides must return to the inactive state before the repeater can be enabled again in either direction.

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