Device Generated Noise Measurement Techniques

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ABSTRACT

In recent years the speed and drive capability of advanced digital integrated circuitry has increased significantly. However, along with the advantages of increased speed and drive has come the consequence of greater device generated noise. Noise is an important consideration when designing systems with todays advanced logic circuits. Device noise levels vary from test board to test board, load value and tolerance, temperature, V_{CC}, and to a larger degree from test board to system. Therefore, realistic measurement technique must be adhered to by those responsible for specifying device noise parameters. As is true with all device parameters, standard methodologies are necessary in order to provide the system designer with consistent data allowing for fair comparative analysis.

INTRODUCTION

Device noise is generated when a sharp increase in current or di/dt is needed to drive one or more outputs from one state to another. A voltage shift or bounce in the device power and ground reference is a manisfestation of this current requirement.

Device generated noise may be somewhat of a misnomer since most of the ''device'' noise originates from the package housing the chip. It is a combination of the bond wire and the leadframe inductance that causes the noise to appear on the internal device power references. The relationship is explained by the equation $V = L*di/dt$ where L is the package inductance. Conversely, if a device circuit has an ideal ground and V_{CC} current path, i.e., 0Ω and 0 inductance to an unlimited low impedance power supply, device noise will not occur.

Some advanced CMOS technologies exhibit output slew rates as great as 2.0V/ns into light loading. The current required to drive ACMOS outputs rail to rail, in so little time, through path inductances is the root of the device noise problem. This also explains why it is so important to properly bypass the device power terminal in a system.

Much work has been accomplished to reduce device generated noise. For instance, National Semiconductor has utilized innovative design approaches such as the split ground leadframe which provides for separate input and output circuit ground paths. Additionally, the Graduated Turn-on (GTO™) and the undershoot corrector (USC) circuits, available on the FACT Quiet Series™ of ACMOS devices, have been instituted to further reduce device noise. Although the problem still exists, significant advances have been made toward reducing device generated noise.

DEVICE NOISE TERMS AND DEFINITIONS

The device noise parameters have been divided into four basic categories for definition and ease of technical discussion. They are as follows:

V_{OLP} (Voltage output low peak): This is the ground bounce parameter. It refers to the positive bump which occurs coincident with the active outputs switching high to low. It is measured on a quiet output which is in a low state.

V_{OLV} (Voltage output low valley): An undershoot which occurs immediately after the V_{OLP} parameter. It is also measured by monitoring a quiet output conditioned to a low state.

V_{OHP} (Voltage output high peak): A measure of the positive excursion or overshoot which occurs as a result of multiple outputs switching from low to high. Measured while monitoring a quiet output conditioned to a high state.

V_{OHV} (Voltage output high valley): A measure of the droop or valley voltage occurring coincident with multiple active signals switching from low to high. This parameter is tested with a quiet output conditioned to a high logic state.

DYNAMIC THRESHOLD

Dynamic thresholds are threshold levels which have been moved due to internal chip reference shifting caused by device generated noise.

V_{ILD}: The shifted dynamic threshold low level.

V_{IHD}: The shifted dynamic threshold high level.

OTHER NOISE TERMS

Overshoot (O.S.): The amount a signal may extend above the V_{OH} level when a low to high transition occurs.

Undershoot (U.S.): The amount a signal may extend below the V_{OL} level when a high to low transition occurs.

Multiple Output Switching (M.O.S.): Used when discussing multiple output switching noise to indicate that more than one gate or driver is switching.

TEST EQUIPMENT

Device generated noise characteristics are dependent on many variables. Some of these include loading, test equipment and testboard layout. Although, there is a load standard, no such standard exists for a test vehicle. A test board for the industry has been suggested by an article written by EDN magazine in the March 2, 1989 issue, entitled ''EDN's Advanced CMOS Logic Ground-Bounce Tests''. The article published ground bounce[1] data taken on various vendors' ACMOS devices using the ESH Inc.[2] test board. This paper centers on use of the ESH testboard because it is believed that this is one of the best commercially available vehicles for device generated noise testing.

The most important test instrument is the oscilloscope. The oscilloscope bandwidth must be adequate for observing the true noise waveform.

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TEST BOARD DESCRIPTION

The ESH test board is a high quality multi-layer board with built-in simplicity and universality. The test board provides for connection to a device pin by two methods. Pin connection is either direct to the device or through a series resistor connection as shown in the single path circuit schematic of *Figure 2*. Sub-miniature coaxial connectors are arranged in two circles around the board as shown on *Figure 1a*. Both the inner and outer rings have pin connections that provide circuit traces of equal electrical length. The inner ring is normally configured with 450Ω series resistors between the connector and the device. This has a dual purpose. Not only does it provide for standard load connection but also a convenient 50Ω X10 scope monitoring point. By plugging a 50Ω sub-miniature terminator into the appropriate inner ring connector the standard resistive load is completed. the detail shown in *Figure 1b* shows how chip components are mounted to the back of the board.

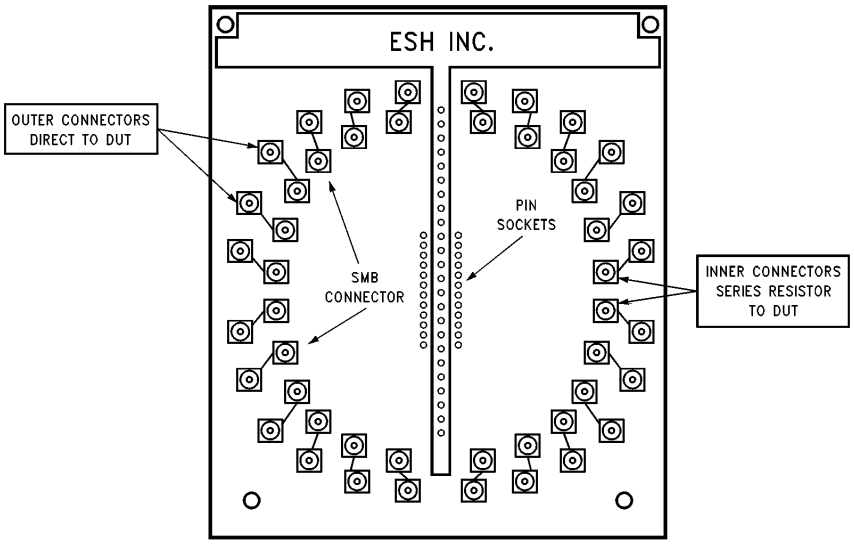

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FIGURE 1a. ESH Testboard Top View

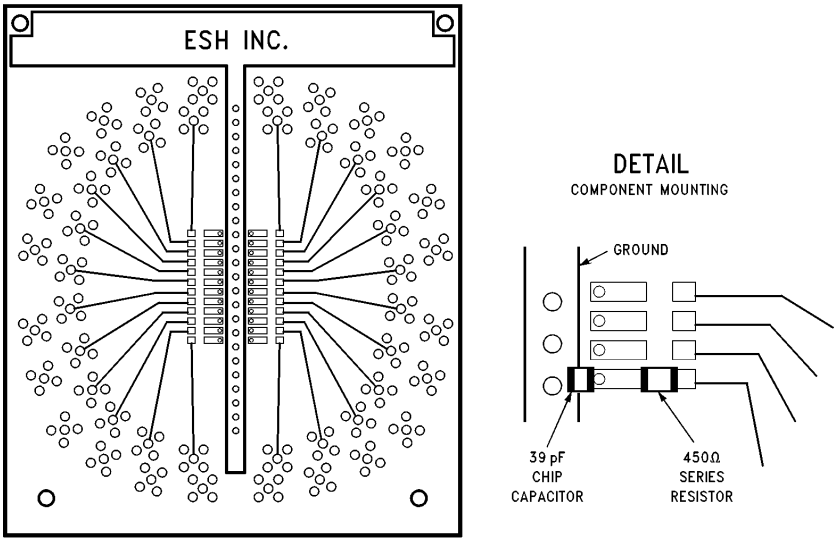

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FIGURE 1b. ESH Testboard Bottom View

TEST BOARD CONSTRUCTION

Low profile pin-sockets must be used for the DUT position on the board. Pin sockets[3] are mounted from the top-side of the board in locations shown on *Figure 1a*. Low profile DUT connection minimizes lead length effects which help assure accurate ''device only'' noise data.

SMB type connectors are soldered into the inner and outer positions from the top-side of the board also. These are male coaxial connectors available from most large electronic distributors[4].

Load capacitors are mounted at the appropriate device output pins. This is done on the bottom-side of the board directly from the pin-socket to the testboard ground strip as shown in *Figure 1b* detail. Each ESH test board circuit trace has capacitance of 12 to 15 pF. Therefore, a capacitor of 39 pF will give the specified standard load of 50 pF.

The fixture must be properly bypassed at the V_{CC} pin. This is done with a high quality RF capacitor of 0.1 μF. A larger value may be soldered in parallel with this for low frequency filtering.

450Ω chip resistors are soldered in at the series connection positions to complete the load/monitoring circuitry on the bottom-side of the board shown in *Figure 1b*.

OTHER TEST EQUIPMENT

A 1 MHz pulse generator or word generator capable of presenting the device with sufficient edge rates will be needed. Testing devices at 1 MHz is recommended since this is the frequency at which noise specification is set. Also, greater frequencies can cause increased heating of the DUT, thereby influencing noise amplitude.

A regulated 5V power supply capable of supplying 1A of current is the other required equipment. If device noise data is needed over temperature then temperature regulating equipment must be considered as well.

TEST METHODOLOGY

General

Octal buffer/drivers and registers are the most commonly used devices which may cause device noise problems in systems. However, the same principles apply to other devices, the only difference being test jig configuration and device pin conditioning.

To test for worst case multiple switching noise the quiet output gate or the path which is the noisiest must first be determined. This gate may differ depending on which noise parameter is to be measured. Usually, the gate with its output residing closest to V_{CC} will exhibit the worse V_{OLP}/V_{OLV} noise while the gate with its output nearest the ground pin will show worse case V_{OHP}/V_{OHV} noise.

Figure 3 is a block diagram depicting the basic device noise test system. Whereas *Figure 6* shows a more specific test system for measuring ground bounce or V_{OLP}/V_{OLV} noise on the 74XXX244 octal buffer/driver.

INPUT CONDITIONING

In order to view multiple output switching noise, seven inputs must be actively switched so that all output edges are coincident. The 8th gate is the quiet monitor which must have the correct input level conditioning. There are two acceptable methods by which the device may be actively switched.

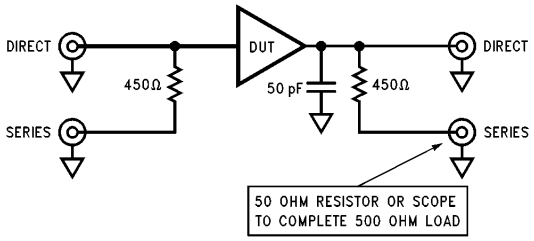

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FIGURE 2. ESH Testboard Basic Single Path Circuit Configuration

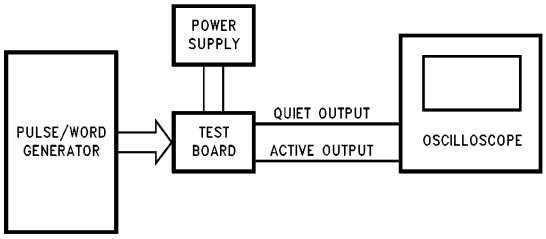

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FIGURE 3. Device Noise Test Set-Up Block Diagram

Word Generator Method

If a multiple output word generator is available each device input may be fed separately. The circuit for an octal device is shown in *Figure 4* using a word generator. As can be seen, each generator output must be terminated at the input to the DUT.

The generator must be de-skewed so that the output edges are as coincident as possible. Word generator outputs can usually be de-skewed to within 100 ps of each other. De-skewing is important because output current is maximum when output edge coincidence occurs. The word generator method of signal feed provides for minimum input waveform distortion. However, it involves a more critical set-up due to skew implications.

Pulse Generator Method

If a single output pulse generator is to be used, the 7 active inputs must be shorted together and fed with the single signal source. The schematic for this can be seen in *Figure 5*. The generator should be terminated in its characteristic impedance and can be connected at any one of the 7 shorted inputs. *Figure 6* shows a typical instrument connection for a V_{OLP}/V_{OLV} test using this method.

An advantage this method has over the word generator is that there is no de-skewing necessary. However, the generator must be capable of driving 7 inputs. The input should be checked to assure the waveform is not overly distorted when 7 inputs are fed together. Also, the V_{HIGH} level may need adjustment to bring it to the proper voltage due to loading effects.

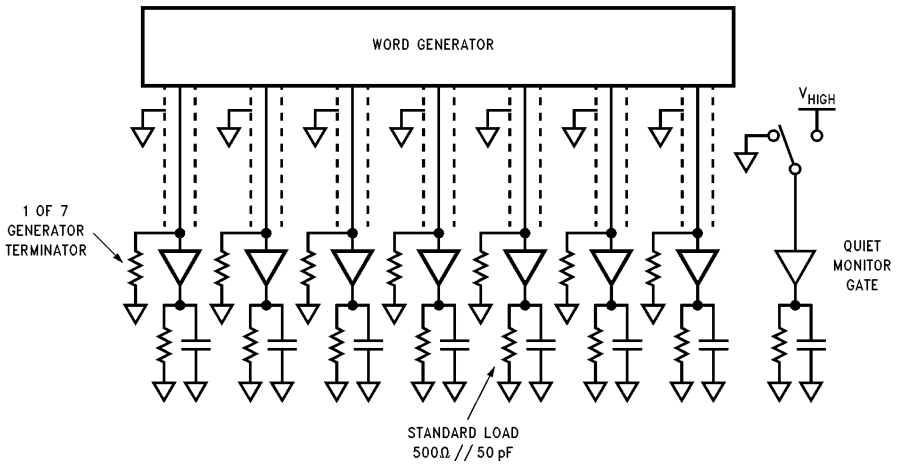

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FIGURE 4. Word Generator Circuit Configuration

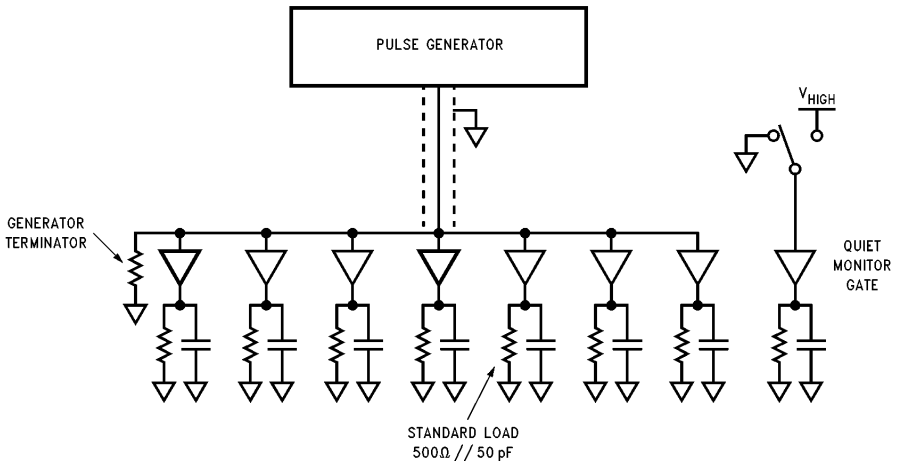

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FIGURE 5. Pulse Generator Circuit Configuration

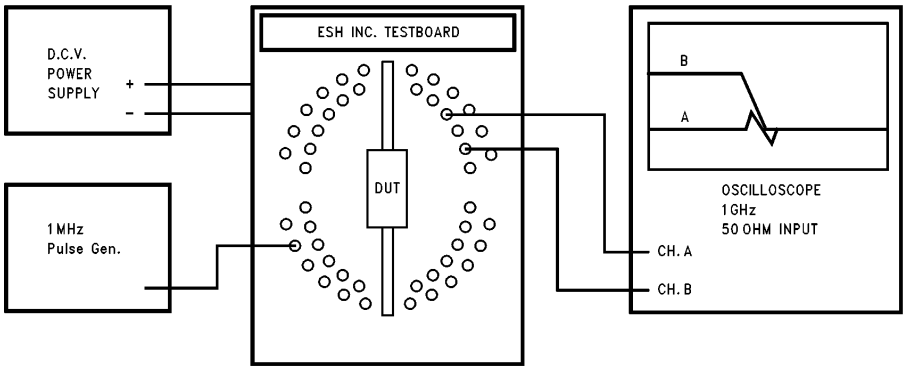

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FIGURE 6. 74X244 Test Set-Up

QUIET MONITOR GATE AND ENABLING

The quiet monitor gate input must be set for a high or low depending upon what device type is being tested and whether V_{OLP}/V_{OLV} or V_{OHP}/V_{OHV} is to be measured. Do this by either plugging in a 50Ω terminator resistor on the appropriate outer ring connector or directly grounding the input or by tying the input to a voltage supply for a high input level.

Any output enabling input pin can be conditioned in the same way as described above.

OUTPUT CONDITIONING

Output Loading

Vendor specifications are normally set using the industry standard load. Therefore, outputs must be presented with standard loads in order for test results to reflect the vendor specified values of device noise. This includes the actively switching outputs as well as the quiet output.

OSCILLOSCOPE

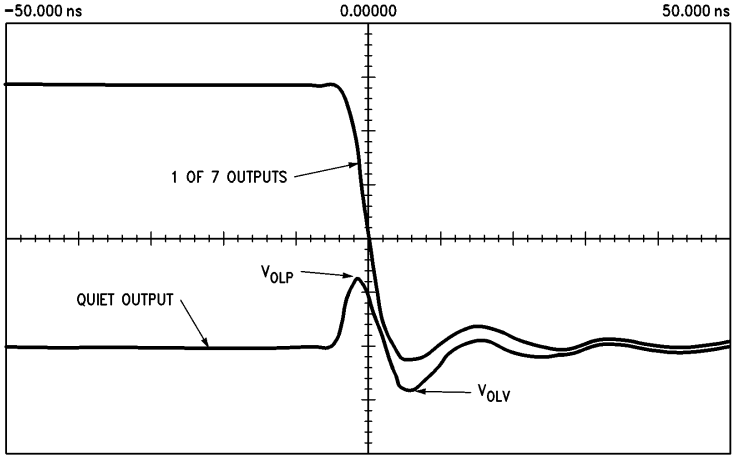
The oscilloscope must have at least a 300 MHz bandwidth. However, a 1 GHz bandwidth is highly recommended. This is because the edge rate and harmonics of advanced technologies can extend into the VHF and UHF range of frequencies. Because the output edge rate is what causes the device noise, it is imperative that the oscilloscope have adequate bandwidth to view the true character of the noise. The oscilloscope should have 50Ω inputs if it is to be used to complete the 500Ω load, otherwise a high impedance FET probe may be used such as the Tektronix model P6201. The probe must have adequate bandwidth and minimum capacitive loading.

Although standard loading is used for setting device specifications, a device may be tested at any load desired. Testing with non-standard loads may be a worthwhile design consideration if the system circuit loading of the device is known. However, system loads are usually distributed while test board loads are lumped. A test board load requires that a greater amount of current be supplied in a shorter time (a larger di/dt) to charge the output load capacitor. This is because of the lumped nature of the load capacitor and the lack of a distributed circuit trace. Therefore, test board noise is worse case.

OSCILLOSCOPE MONITORING

The oscilloscope should have 50Ω inputs and may be used to complete the 500Ω load on two of the device monitored outputs. One channel is connected to a switching output in order to provide a trigger and to monitor one of the 7 actively switching outputs. The other channel is used to measure the device noise at the quiet gate output. If the ESH test board is being used, the inside ring should be used for completing the load and monitoring signals. See *Figure 6* for oscilloscope connection when testing the 74XXX240, 241 or 244 device for ground bounce.

Oscillographs showing the typical waveshapes for V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} are shown in *Figures 7a* and *7b* respectively.



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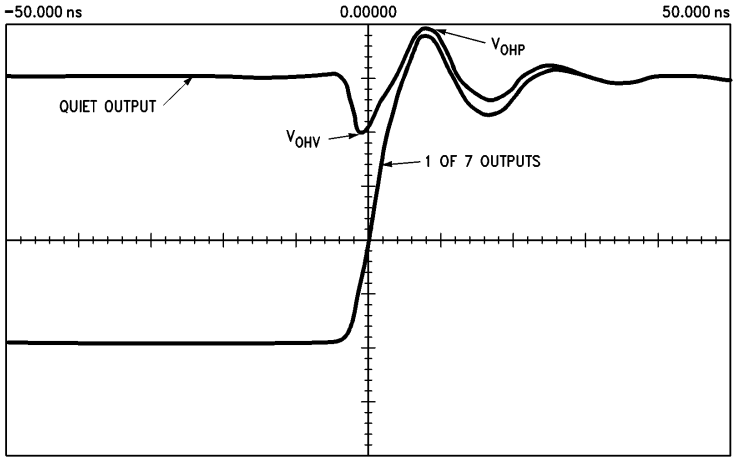
Ch. 1 = 1.000 V/div Offset = 2.080V
Ch. 2 = 1.000 V/div Offset = 2.000V
Timebase = 10.0 ns/div Delay = 0.00000 sec

FIGURE 7a



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Ch. 1 = 1.000 V/div Offset = 2.080V
Ch. 2 = 1.000 V/div Offset = 2.000V
Timebase = 10.0 ns/div Delay = 0.00000 sec

FIGURE 7b

DYNAMIC THRESHOLD

Unlike static threshold the dynamic thresholds of a device are those found under worse case multiple output switching conditions. Dynamic threshold measurement, like device generated noise, is very sensitive to the test environment. All the standards used for testing device generated noise should be adhered to when testing dynamic thresholds.

An accepted method of testing dynamic thresholds utilizes a set-up identical to that for testing device generated noise. The difference is that a variable DC voltage supply is connected to the quiet monitor gate input. The DC voltage at the input is varied while the quiet gate output is monitored for the accepted threshold criterion.

The dynamic threshold low is tested while triggering on 1 of 7 high to low active edges. The DC input voltage is raised or lowered, depending on whether the gate is inverting or not, while monitoring for failure criteria. Dynamic threshold high is checked while triggering on 1 of 7 low to high edges and lowering the DC voltage from V_{OH}, in the case of a non-inverting gate, until the threshold high criteria is met.

The criterion may be the guaranteed TTL static threshold levels of 0.8V for a low and 2.0V for a high. The levels may occur in the form of glitches when testing buffers and gates or oscillation when testing clocked devices.

For a more detailed explanation of the dynamic threshold phenomenon and testing techniques please refer to National Semiconductor applications note AN-680, ''Dynamic Threshold for Advanced CMOS Logic''.[5]

SUMMARY

The importance of using standard methodology and proper equipment cannot be over-emphasized when considering a system for measuring device generated noise. There are many variables which can affect the characteristic of the noise pulse. Some of these are test jig, oscilloscope bandwidth and impedance, loading, power supply voltage, and temperature.

This paper has been written in order to describe standard methodology which should be adhered to when testing for device generated noise. It is our desire that it provide specific technical insight and guidelines to assist designers using advanced technologies.

REFERENCES

1. For further explanation see National Semiconductor application note AN-640, ''Understanding and Minimizing Ground Bounce''.

2. ESH Inc., 3020 So. Park Drive, P.O. Box 26471, Tempe, AZ, Part #: LAB-300-24 REV C; PH: 602-438-1112.

3. Sterling Electronics, P.O. Box 4041, 15D Constitution Wy., Woburn, MA, pin socket Part #:SLSG-1 D68-1; PH: 617-938-6200.

4. Digi-Key Corp., 701 Brooks Ave. South, P.O. Box 677, Thief River Falls, MN, sub-miniature connector Part #:J467.

5. For detailed discussion see National Semiconductor application note AN-680, ''Dynamic Threshold for Advanced CMOS Logic''.

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