Using Logic Devices with 25Ω Series Resistors in the Outputs

National Semiconductor
Application Note 754
John Davis
February 1991

The 25Ω Series Damped Devices in National Semiconductor's FAST®, FASTr™, and BCT logic families are useful in any high-speed drive application where control of undershoot and ringing is a concern. They are ideal for noise control in applications where reflected wave switching is permitted, and where use of conventional parallel or Thevenin termination is undesirable.

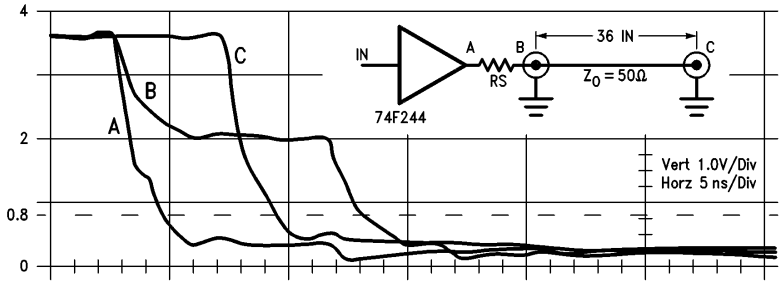
These devices are particularly useful for driving the arrays of capacitive inputs of DRAM devices where undershoot below −1V may corrupt or damage the memory. They are also ideal for driving the inputs of some programmable devices (PLDs) where excessive and repetitive undershoot may alter the device's programmed pattern.

DAMPING DISCUSSION

The placement of an external damping resistor in series with, and immediate to, a low impedance driver's output is a commonly recommended method for reducing under/overshoot when driving unterminated transmission lines and other networks. (Refer to Section 3 ''Design Considerations'' in the FAST Advanced Schottky TTL Logic Databook for a discussion of transmission line concepts and termination techniques.) The damping resistor raises the effective-driver impedance to approximate a series termination for the driver relative to the effective-line impedance. When the effective-driver impedance matches the effective-line impedance, the line is ''series terminated''. This results in 50% reduction of the driver's voltage step presented as the incident wave into the line. Upon reaching the unterminated end of the line, the incident voltage wave is doubled by the first reflection to the desired logic swing and will have minimal undershoot. The first reflection proceeds back toward the driver where it is terminated by the close match of equivalent damped-driver impedance to the line's effective impedance, minimizing second reflections. *Figure 1a* illustrates the effects of series damping which approximate a series termination.

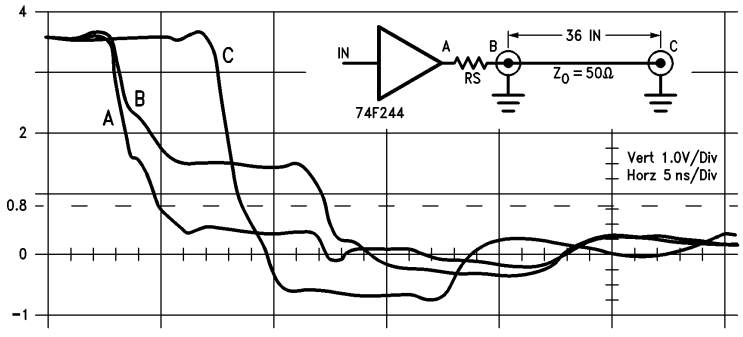
''Critical Damping'' *(Figure 1a)* occurs when the effective-driver impedance closely matches the effective-line impedance and results in a near ideal series termination. This results in optimum transition times and control of undershoot and ringing with full logic transition accomplished on the first reflection.

The effective-line impedance is application specific and may not closely match the chosen damped-driver impedance. When the line impedance is greater than the driver impedance, the line response is ''under damped'' and some degree of undershoot and ringing will be present.(*Figure 1b*)



TL/F/10906–1

FIGURE 1a. Critical Damping; RS = 51Ω



TL/F/10906–2

FIGURE 1b. Under Damping; RS = 25Ω

FAST® is a registered trademark of National Semiconductor Corporation.
FASTr™ is a trademark of National Semiconductor Corporation.

 TL/F/10906

RRD-B30M75/Printed in U. S. A.

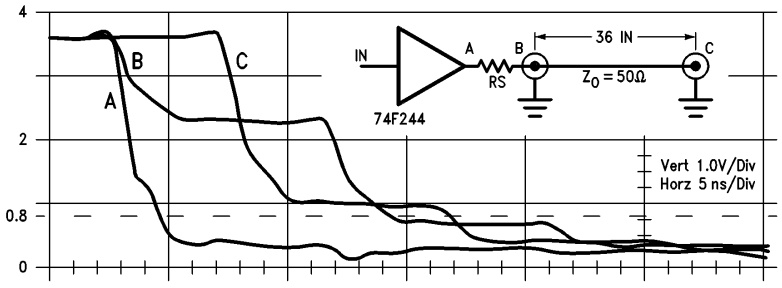
When the effective-driver impedance is greater than effective-line impedance, an ''overdamping'' condition exists. Here the incident voltage step into the line will be less than half of the desired logic swing. This can result in excessive transition/delay times as multiple reflections may be required to complete the logic transition. The three damping conditions are summarized graphically in *Figures 1a, b,* and *c* in contrast to no damping in *Figure 1d.*

Note that some propagation delay penalties are to be expected when using damped- or series-terminated drivers with distributed loads. Depending on the degree of damping, the loads close to the driver must typically wait for the first reflection to arrive from the open end of the line to see full logic swing at their input. These loads closest to the driver cannot be guaranteed to receive their valid input logic stimulus until twice the one-way delay of the line. This is called reflected wave switching. Also, the effective line delay is modified by capacitive loading differently for series-terminated lines than for parallel-terminated lines. In general, series-terminated lines are slower than equivalent lines with parallel terminations. For equivalent loading, the delay modifier for the series-terminated line will be about twice that of the same line with parallel termination. The effective line delay modifiers for the series-damped condition will best be determined empirically in the application.

Note also that static I_{IL} and I_{IH} fan-in load currents will cause voltage drop across the damping resistor, thereby reducing static noise immunity when driving TTL logic.

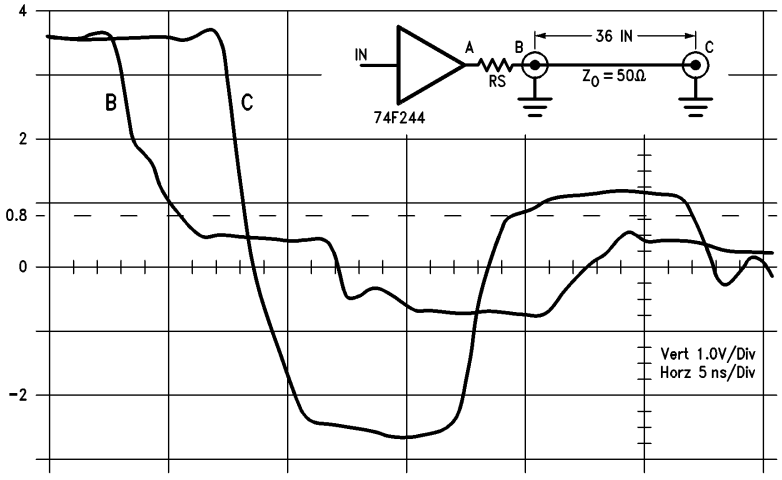
DAMPING VS PARALLEL TERMINATIONS

The system designer will choose the form of application termination based on performance demands and personal preference. Both parallel and damped/series-termination forms are effective in waveform control. The parallel-termination form permits maximum speed since incident wave switching for distributed loads is achieved, this scheme has the lowest modified line delays. The damped- and series-terminated forms are inherently slower due to their reflected wave mode of operation; however, they do offer some advantages over parallel forms of termination. The reduced energy of the incident wave in a damped- or series-terminated line translates to reduced crosstalk and radiated EMI. Static power dissipation in the termination is significantly reduced with damped/series-terminated lines versus parallel terminations. The damping/series resistor limits the transient load current into the driver to reduce ground bounce and V_{CC} droop effects during multiple output switching.



TL/F/10906–3

FIGURE 1c. Over Damping; RS = 75Ω



TL/F/10906–4

FIGURE 1d. No Damping/Unterminated; RS = 0Ω

NATIONAL'S DEVICES WITH INTERNAL DAMPING

Standard high-speed and high-drive buffer devices, such as the 74F244, are frequently chosen to drive distributed loads and low impedance networks. The low impedance (3Ω), high current sink (64 mA) characteristics of these devices are useful for driving high TTL fanout and heavy loads with a full 3V negative-going swing. (See 74F244 output drive characteristics in *Figure 3.*) When this device is used for memory driving without some form of parallel or Thevenin termination, it becomes a candidate for use with external-series damping if undershoot is to be controlled. These types of popular Buffer/Line Driver and Transceiver devices were chosen by National to be offered with a manufacturing option of internal 25Ω series damping.

TABLE I. FAST, FASTr, and BCT Devices with 25Ω Series Damping Resistors in the Pull-Down Stage

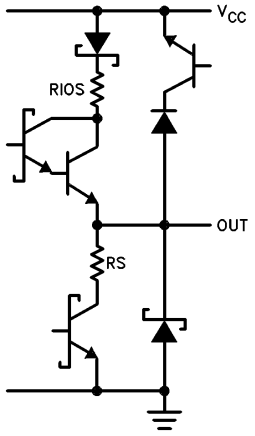
Series Damped Device	Function
74F2240	Octal Buffer/Line Driver; Inverting
74F2241	Octal Buffer/Line Driver
74F2243	Quad Bus Transceiver
74F2244	Octal Buffer/Line Driver
74F2620	Octal Bus Transceiver; Inverting
74F2623	Octal Bus Transceiver
74F2640	Octal Bus Transceiver; Inverting
74F2643	Octal Bus Transceiver; Inverting B
74F2645	Octal Bus Transceiver
74FR2240	Octal Buffer/Line Driver; Inverting
74FR2241	Octal Buffer/Line Driver
74FR2244	Octal Buffer/Line Driver
74BCT2240	Octal Buffer/Line Driver; Inverting
74BCT2241	Octal Buffer/Line Driver
74BCT2244	Octal Buffer/Line Driver
74BCT2827A	10-Bit Buffer/Line Driver
74BCT2828A	10-Bit Buffer/Line Driver; Inverting

Note 1: 74F2645 and 74F645 are lower power logic equivalents of the 74F245.

Note 2: Contact your local NSC Sales Office for additional product announcements and availability.

INTERNAL PULL-DOWN DAMPING

Figure 2 shows placement of the internal RS Damping Resistor in series with the pull-down transistor of these series-damped devices. This placement accomplishes the desired damping effect to the high-to-low (HL) transition without altering the inherent damping by the pull-up stage's RIOS register on the low-to-high (LH) transition.



TL/F/10906–5

FIGURE 2. Circuit Placement of RS Series Damping Resistor

Table II summarizes the output drive specifications of the typical damped device in contrast to the undamped master device. The damping resistor radically alters the sink capability of the pull-down stage but leaves the pull-up stage's source drive unchanged. The equivalent series resistance of the damped pull-down stage now closely matches that of the inherently-damped pull-up stage (illustrated in *Figure 3*). This balancing of the output's source/sink impedance moves the device toward an idealized constant impedance driver. This facilitates its use as a series-terminated or back-matced driver in point-to-point drive applications. The constant impedance load lines drawn onto the output drive characteristics in *Figure 3* further demonstrates the drive reduction of the damped pull-down stage. Note that the undamped 74F244 sink characteristics indicate incident wave switching from full V_{OH} to a V_{OL} point safely below the 0.8V logic threshold into line impedances as low as 30Ωs. In contrast, the damped 74F2244 is incapable of achieving incident swing to a V_{OL} point below V_{IL} into impedances as high as 100Ω.

TABLE II. DC Specification Comparison

74X 10% V_{CC} Data Sheet Parameter	Series Damped Device	Un-Damped Device
V_{OL} @ I_{OL}	<0.5V @ 1 mA	
V_{OL} @ I_{OL}	<0.75V @ 12 mA	<0.55V @ 64 mA
V_{OH} @ I_{OH}	>2.4V @ −3 mA	>2.4V @ −3 mA
V_{OH} @ I_{OH}	>2.0V @ −15 mA	>2.0V @ − 15 mA
I_{OS} (5.5V)	> −100 mA	> −100 mA
I_{OS} (5.5V)	< −225 mA	< −225 mA

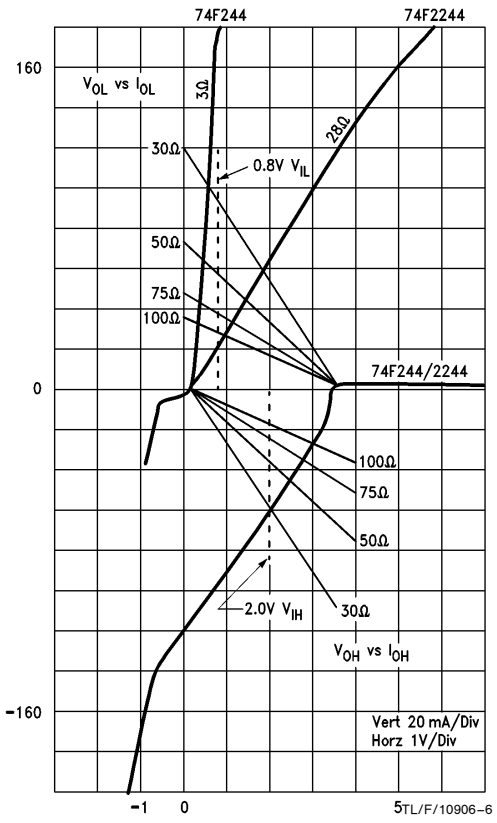


FIGURE 3. DC Output Drive Characteristics V_{CC} = 5V, T_A = 25°C

An additional benefit to placing the damping resistor in series with the pull-down stage improved noise control. The damping resistor limits any simultaneous switching currents shared in the totem pole output stage as well as limits the peak in-rush load current during the HL transitions. These factors contribute to lower peak ground currents which reduces both ground bounce and dynamic threshold erosion.

WHY 25Ω?

The 25Ω RS damping resistor was chosen as a nominal value for effectively controlling undershoot to less than 1V below ground. This would be the case for a memory drive application where the effective loaded line impedance is less than 50Ω. For example, a small DRAM array of nine devices distributed uniformly on a five-inch section of 75Ω microstrip will lower the effective line impedance to approximately 30Ω, assuming 5 pF input capacitance of a DRAM. The addition of the damping resistor raises the effective pull-down stage on impedance to a nominal 28Ω as shown for the 74F2244 in *Figure 3*. The 74F2244's series impedance closely matches the effective line impedance creating a critically damped condition.

INTERNAL DAMPING PERFORMANCE COMPARISON IN LINE DRIVE APPLICATION

Figure 4a illustrates a simulated application for point-to-point driving of a light capacitive load (MOS device) over a 36-inch length of unterminated 50Ω coaxial transmission line.

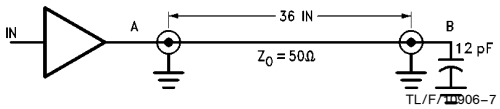
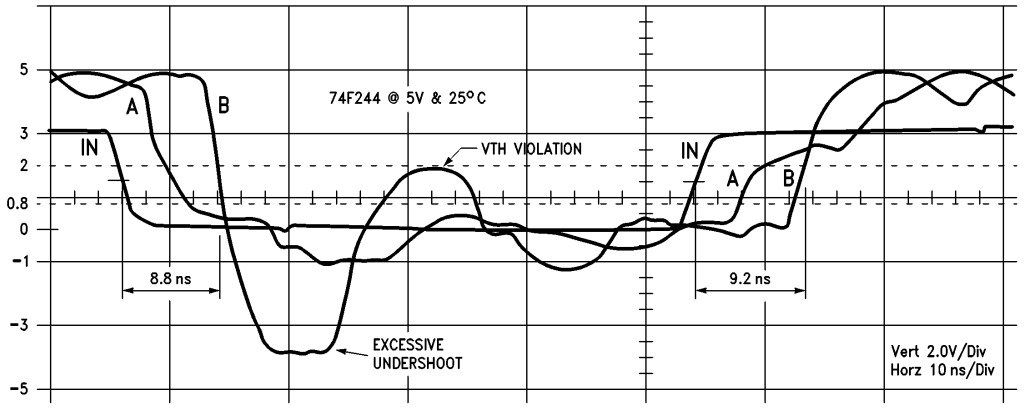


FIGURE 4a. 74F2244/244 Line Drive Demo Fixture

Figure 4b shows the effect at points A and B when this circuit is driven by the undamped 74F244. The 50Ω load line of *Figure 3* indicates the 74F244 is capable of a nearly full HL swing into 50Ω. The incident step seen at point A supports this. The incident LH voltage at point B is nearly doubled, causing severe undershoot which lasts until the partially re-reflected wave returns a full round trip line delay later. The second reflection is then doubled at the open end of the line to cause severe ringing which violates the logic low threshold to the load. The incident LH voltage step at point A shows the inherent damping of the RIOS resistor in the pull-up stage dropping a portion of the drivers internal voltage swing with the doubling effect seen at point B. As predicted by *Figure 3,* the incident LH wave is sufficient to traverse the TTL logic threshold region. The LH wave reflections tend to reverberate since, in the absence of any pull-down resistor in this circuit, the reflection coefficients are unity at both ends of the line when the reflected wave reverse biases the driver pull-up stage. Lowering the test pulse frequency significantly allows the ringing to damp out naturally. Alternatively, a 1 kΩ shunt resistor placed at either end of the line quenches the logic high ringing and quickly restores a nominal V_{OH} level to the line.



TL/F/10906–8

FIGURE 4b. 74F244 Line Drive Demo Fixture

Figure 4c shows the effects of driving the circuit with the internally-damped 74F2244. As predicted by *Figure 3,* the 74F2244 cannot provide full HL voltage swing into 50Ω as evidenced by the reduced incident voltage step at point A due to voltage drop across the internal RS damping resistor. The voltage doubling at B is evident but is proportional to the smaller incident wave. The result is significantly less undershoot and controlled ringing on the second reflection. This is due to better absorption of reflected voltage at the driver as its damped impedance more closely matches the line. Undershoot at B goes slightly below 1V. The higher-than-normal starting V_{OH} value contributes to a larger incident voltage step and therefore a larger first reflection. The shunting of the line with a 1 kΩ resistor, as mentioned earlier, normalizes the starting V_{OH} and reduces the incident swing and associated reflections. The line behavior then closely resembles that of *Figure 1b* where undershoot is well above −1V.

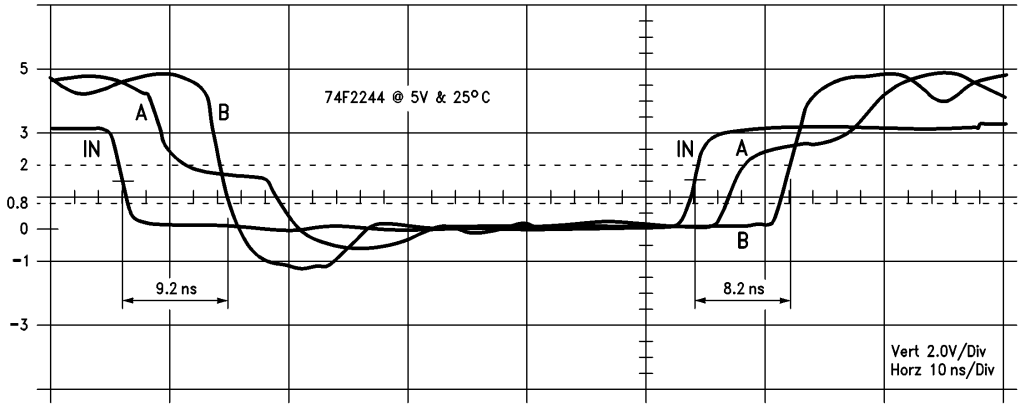
Note that propagation time to the initial logic low on the HL transition at B is slightly slower with the damped service. This is due to the higher driving point impedance which slows the edges and kicks the line with less energy on the incident step. This is the performance tradeoff for series damping in consideration of the improved HL waveforms seen at B. Again note that the 74F2244 does not permit incident wave switching at point A or along the line.

Propagation time to initial logic high on the LH transition should theoretically be equal for both devices since pull-up stages are identical. The 74F2244 appears faster, possibly as the HL reflection effects on the 74F244 driver have not settled out due to the short duty cycle used.

The undershoot still seen at point B when driving with the 74F2244 is evidence that the circuit is ''underdamped''. An additional external damping resistor (10Ω–20Ω) may be used to further reduce undershoot as optimum or ''critical'' damping is approached. Addition of the external resistor affects damping of both the pull-down and pull-up stages.

INTERNAL DAMPING PERFORMANCE COMPARISON IN DISTRIBUTED LOAD APPLICATION

Figure 5a illustrates a simulated application for driving the distributed capacitive load seen in a dense MOS memory array over a four-inch length of unterminated 75Ω microstrip



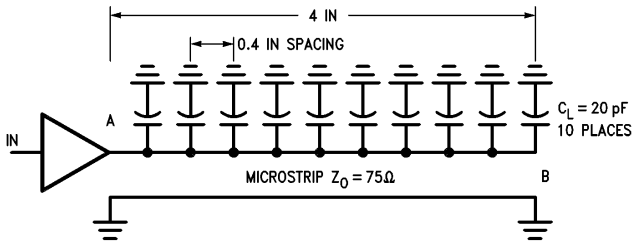
TL/F/10906–9

FIGURE 4c. 74F2244 Line Drive Demo Fixture

transmission line. The uniform distributed capacitive loading of the line significantly lowers the impedance seen by the driver during transition. In this example, effective impedance has been lowered from 75Ω to approximately 15Ω.

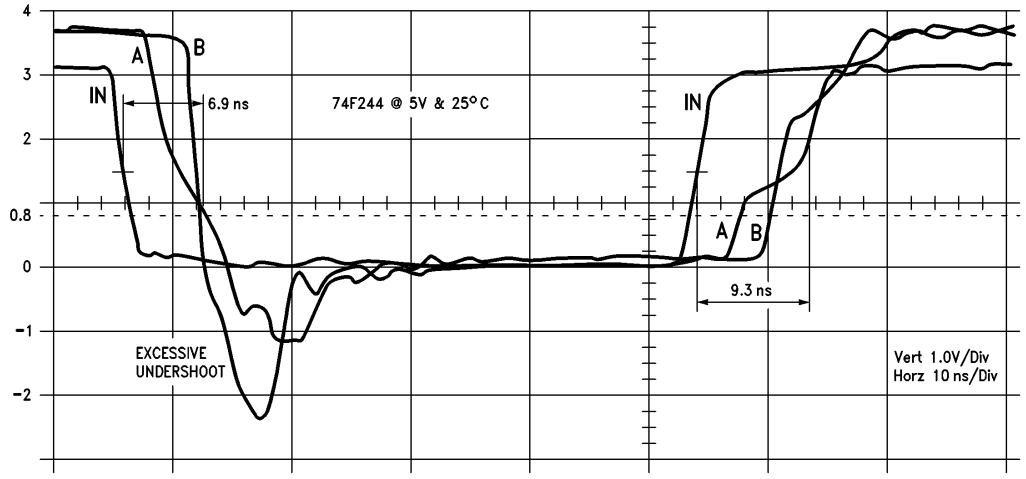
As seen in *Figure 5b,* the 74F244's LH incident step at point A barely reaches 1V, indicating an over-damped condition with the effective load impedance significantly less than the driver (pull-up) source impedance. The 74F244's HL transition shows significant undershoot, indicating an under-damped condition. The severity of loading to the driver is evident as propagation-to-threshold logic low/high is reached sooner at the far (B) end of the network than at the driven (A) end due to reflective effects.

In *Figure 5c,* the 74F2244's damping is very effective in eliminating the HL undershoot at some penalty in network propagation delay. The stepped response at B and two-step response at A is evidence of over-damping. A 10Ω internal pull-down damper would have been optimum for this particular application and an improved HL delay characteristic would then be realized. The slightly faster LH delay seen with the 74F2244 vs 74F244 is probably due to variation in the RIOS resistors of the devices chosen for the demonstration. The device with the lowest RIOS is less damped and will drive the load fastest.



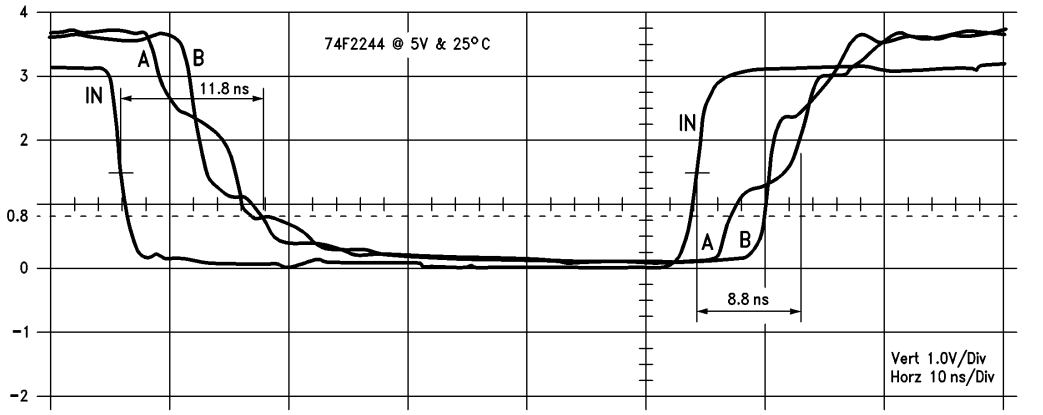
TL/F/10906–10

FIGURE 5a. 74F2244 Distributed Load Demo Fixture



TL/F/10906–11

FIGURE 5b. 74F244 Distributed Load Demo Fixture



TL/F/10906–12

FIGURE 5c. 74F2244 Distributed Load Demo Fixture

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998