Operating ECL from a Single Positive Supply

National Semiconductor
Application Note 780
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May 1991

INTRODUCTION

ECL is normally specified for operation with a negative V_{EE} power source and a negative V_{TT} termination supply. This is the optimum operating configuration for ECL but not the only one. Operating ECL from a positive V_{CC} supply is a practical alternative that is gaining in popularity. Positive referenced ECL, or PECL as it is referred to, has been implemented in various mixed signal ASIC for use in the Video Graphics and Communications fields and is used in clock distribution as well. New single supply translator chips are becoming available to facilitate the interface of PECL logic levels to TTL and back again. Logic designers who strive for maximum speed in a system, now can easily replace sections of TTL logic with ECL and operate in PECL fashion from the common TTL V_{CC} supply.

STANDARD NEGATIVE SUPPLY ECL OPERATION AND WHY

Figure 1 shows F100K logic elements operating in standard negative supply ECL configuration. The most positive potential is the primary voltage reference for ECL operation. Standard ECL input and output levels are therefore negative potentials referenced to the stable passive Ground (0V). The inherent F100K voltage compensation permits stable input and output levels over a broad range of V_{EE}'s; i.e., −4.2 to −5.7 VDC for 300 Series F100K. Thus ECL logic operating from a −4.2V V_{EE} is compatible to logic operating from a −5.7V supply assuming both are referenced to a common 0V Ground.

Since ECL logic outputs only source currents that originate from the potential applied to its V_{CC}/V_{CCA} pins, the use of a 0V low impedance and low inductance ground potential is the optimum choice for operation. The use of a continuous copper ground plane as the primary ECL reference is the ideal source for the high frequency transient currents demanded by the logic during switching. Note that despite the ideal nature of a ground plane as the primary ECL reference, when mixing TTL (or other noisy circuitry) into ECL systems, the recommendation is to reference the TTL to a separate ground plane. This is to keep the high transient TTL switching energy out of the primary ECL reference and preserve ECL noise margins.

When F100K ECL output signal interconnection lengths are direct and short enough, transmission line effects may be ignored and then only a RE output biasing resistor is required for logic operation. Please refer to section seven of the "F100K ECL Logic Databook and Design Guide" for a more detailed explanation of transmission line effects and ECL termination techniques. The RE resistor provides bias to keep the ECL emitter follower output transistor on for both high and low logic states. The RE resistor is normally connected between the ECL output and the most negative potential (V_{EE}) thus permitting "single" supply operation.

The V_{EE} potential will ideally be distributed to the ECL logic from a power plane or bus which has low DC series resistance and low AC impedance. The low AC impedance is essential to supply the transient energy needed during switching. Although the inherent nature of ECL by design is to maintain essentially constant I_{EE} current even during switching, the charging and discharging of internal and external capacitances and the switching currents in the RE resistors place transient demands on V_{EE}. The degree to which the user can maintain complementary balance of ECL output loading will greatly influence the nature of the transient I_{EE} demands.

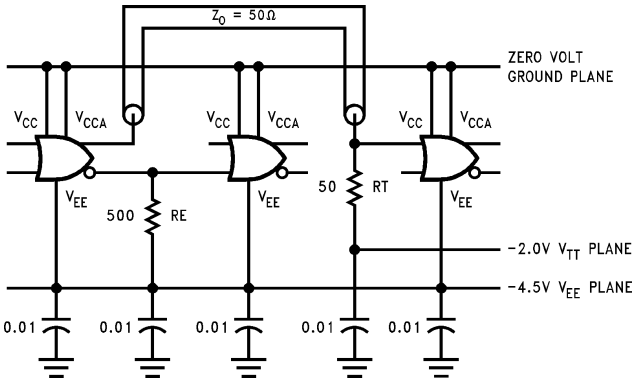

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FIGURE 1. ECL Standard Operation from a Negative V_{EE} Supply

F100K 300 Series Voltage Levels Specified for Standard Negative V_{EE} Supply Operation

Level	Min	Typ	Max	Units
V_{OH}	−1.025	−0.955	−0.87	VDC
V_{IH}	−1.165		−0.87	VDC
V_{BB}		−1.320		VDC
V_{IL}	−1.83		−1.475	VDC
V_{OL}	−1.83	−1.705	−1.62	VDC

Conditions: V_{CC}/V_{CCA} = 0.0 VDC Ground
V_{EE} = −4.2 to −5.7 VDC
RT = 50Ω; V_{TT} = −2.0 VDC
All Levels W.R.T. Ground

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The usual recommendation for the V_{EE} plane is to bypass every ECL device at its V_{EE} pin with a good RF quality ceramic capacitor. The point at which the RE resistors return to the V_{EE} plane should also be bypassed particularly if it is a single return from a multiple resistor R-PAK. Values from 0.01 μF to 0.10 μF of the "High K Class II Dielectric" ceramic Z5U grade capacitor are recommended for commercial applications. The lower series inductance inherent in the leadless chip style capacitor is preferred over leaded types for highest frequency performance. The "Mid K Class II Dielectric" ceramic X7R grade capacitor offers acceptable bypass operating characteristics over the broader temperature range of $-55°C$ to $+125°C$.

Bulk bypassing of the V_{EE} plane with a 1 μF to 10 μF is recommended at the point where the V_{EE} supply connects to the plane. Aluminum or Tantalum Electrolytic capacitors are usually used for bulk bypassing. Miniaturized surface mount Electrolytic capacitors are available for use in high density component applications.

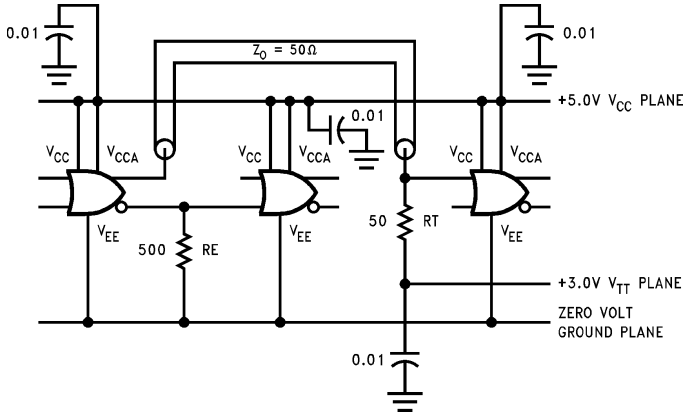
In typical ECL system designs, some inter-connection lengths will exceed the critical values and force the consideration of transmission line effects. The most common high performance and power efficient termination scheme requires the use of a negative 2.0V V_{TT} termination supply. A single RT resistor in conjunction with the V_{TT} supply will terminate each output's transmission line in its characteristic impedance and will also provide optimum bias to the ECL output transistor.

The V_{TT} potential will ideally be distributed to the RT terminators from a power plane which has low DC series resistance and low AC impedance. The low AC impedance is essential to supply the transient energy in the termination resistors during switching. Bypassing V_{TT} wherever RT resistors return to the V_{TT} plane is essential to maintaining the low AC impedance of the plane. Capacitor recommendations for bypassing V_{TT} are the same as for V_{EE} above.

The regulation of the V_{TT} supply is not critical. A variation of $\pm 5\%$ from nominal causes typically only ± 12 mV variation in output levels for 50Ω terminations or ± 7 mV variation for 100Ω terminations. Note that in standard ECL configuration, the V_{TT} supply need only sink current into its negative terminal (single ended V_{TT} operation with positive terminal grounded). V_{TT} here will typically be a simple series regulated supply. If the need for single negative supply operation is paramount, a less power efficient Thevenin termination scheme can be used between the V_{CC}/V_{CCA} and V_{EE} planes and selective use of series damping in conjunction with RE resistors may also be implemented.

THE PECL TRANSFORMATION

Transforming ECL from negative supply to positive supply operations is conceptually quite easy. Just offset all standard ECL operating potentials by a positive amount equal to an absolute value within the normal V_{EE} operating range. For F100K 300 Series the normal V_{EE} range is -4.5 to -5.7 VDC. A 5V offset fits nicely within the range and happens to match the nominal potential for TTL systems. Thus V_{EE} becomes the 0V ground with V_{CC}/V_{CCA} offset to $+5$V and V_{TT} (if required) offset to $+3$ VDC. *Figure 2* illustrates the transformation (from *Figure 1*).



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F100K 300 Series Voltage Levels Specified for Positive V_{CC} Supply [PECL] Operation

Level	Min	Typ	Max	Units
V_{OH}	$V_{CC} - 1.025$	$V_{CC} - 0.955$	$V_{CC} - 0.87$	VDC
V_{IH}	$V_{CC} - 1.165$		$V_{CC} - 0.87$	VDC
V_{BB}		$V_{CC} - 1.320$		VDC
V_{IL}	$V_{CC} - 1.83$		$V_{CC} - 1.475$	VDC
V_{OL}	$V_{CC} - 1.83$	$V_{CC} - 1.705$	$V_{CC} - 1.62$	VDC

Conditions: $V_{CC}/V_{CCA} = 4.2$ to 5.7 VDC
$V_{EE} = 0.0$V to Ground
RT = 50Ω; $V_{TT} = V_{CC} - 2.0$ VDC
All Levels W.R.T. Ground

FIGURE 2. ECL Operation from a Positive V_{CC} Supply [PECL]

CONSIDERATIONS FOR PECL OPERATION

All the considerations previously discussed for standard operation still apply; i.e., solid isolated and well bypassed reference planes, etc. Some additional considerations apply for PECL operation.

PECL input and output levels are referenced to the active positive V_{CC} rail that is variable and subject to line and load regulation. PECL level compatibility between sub-systems or systems can be difficult if precise V_{CC} distribution and accuracy are not maintained throughout. Differential PECL signal transmission and reception between systems may be necessary to ease the V_{CC} accuracy burden.

This active positive V_{CC} potential is the primary reference for PECL levels and the source of PECL switching currents. The distribution of V_{CC} to PECL logic is just as important as is the ground distribution to the standard ECL configuration. V_{CC} should be delivered from a continuous copper plane with liberal use of high frequency decoupling capacitors at each PECL device's V_{CC}/V_{CCA} pins.

If TTL or other noisy circuitry is to share the V_{CC}, a separate powerplane should be provided. TTL switching transients should be isolated from the PECL V_{CC} plane to preserve PECL noise immunity. Again, differential PECL operation may be warranted for situations where noise control is limited and good common mode noise rejection is required.

The various requirements for output termination and bias previously discussed for standard ECL applies directly to PECL operation. Note that the nominal $+3V$ V_{TT} supply in PECL mode is required to sink current into its positive terminal (single ended V_{TT} operation with negative terminal grounded) from the emitter follower outputs throught the RT resistors. A current sinking V_{TT} supply will be necessary if operated single ended to ground. The V_{TT} supply should track the V_{CC} supply keeping a nominal 2V offset to assure optimum biasing of the outputs.

The V_{EE} for PECL operation is 0V or ground potential and should be distributed from a continuous copper plane in consideration of handling the transients switching currents from the RE bias resistors. Although the PECL V_{EE} plane will be somewhat tolerant of TTL noise, the recommendation is to isolate TTL transient switching energy in a separate TTL ground plane.

POWERPLANES

The dedication and organization of powerplanes is essential to successful ECL system design.

Figure 3 illustrates an optimum powerplane implementation for Standard ECL operation on a printed circuit mother board in conjunction with TTL circuitry. *Figure 4* shows an optimum powerplane configuration for PECL operation. Note that the dedication and positioning of separate ECL and TTL powerplanes is intended to preserve ECL noise immunity when operating in a mixed signal environment.

Copper Plane 1	Signal
2	TTL 0V Ground
3	TTL $+5V$ V_{CC}
4	Auxillary GND/Power/Thermal
5	ECL $-$ 2V V_{TT}
6	ECL $-$ 4.5V V_{EE}
7	ECL 0V Ground
8	Signal

FIGURE 3. Powerplane Layup for Standard ECL Operation

Copper Plane 1	Signal
2	TTL 0V Ground
3	TTL $+5V$ V_{CC}
4	Auxillary GND/Power/Thermal
5	ECL $+$ 3V V_{TT}
6	ECL 0V V_{EE}/Ground
7	ECL $+$ 5V V_{CC}
8	Signal

FIGURE 4. Powerplane Layup for Positive Referenced ECL

The optimum multiple powerplane approach may not be feasible for some designs. Logic and powerplane partitioning (islands) can be used to control noise when ECL and TTL must share the same powerplane. *Figure 5* illustrates the basic concept where areas of a system board are organized by logic type and share the same horizontal powerplane. Low pass filters are usually used to help isolate high frequency signals in sections of the shared plane.

POWER SUPPLY SEQUENCING CONSIDERATIONS

In logic systems where multiple independent power supplies are used, or where two independently powered systems are connected logically, some consideration must be given to supply sequencing. This is particularly true for ECL/PECL logic due to placement of ESD (Electrostatic Discharge) protection diodes on the inputs and outputs. *Figure 6* shows the typical ESD diode placement in a F100K 300 Series device. *Figures 7a* and *7b* illustrate independently powered ECL driver and receiver operating with an independent ground referenced V_{TT} termination supply.

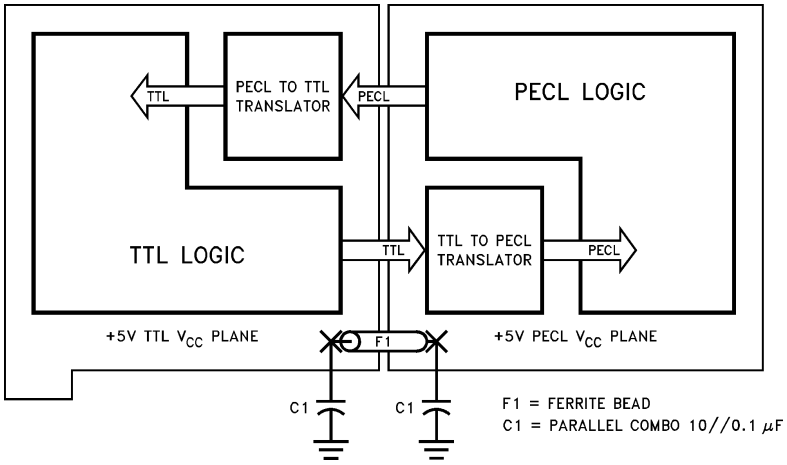

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FIGURE 5. Powerplane and Logic Partitioning

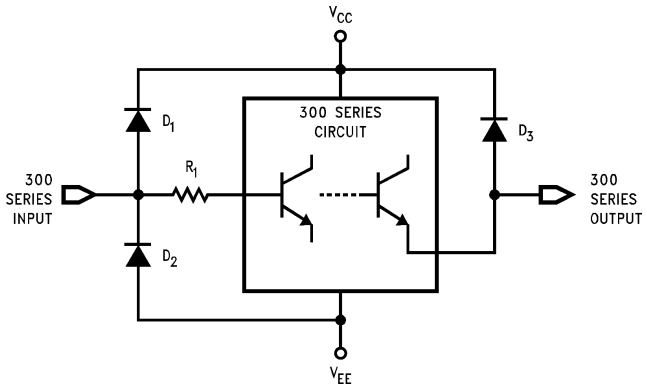

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FIGURE 6. F100K 300 Series ESD Diode Circuit Placement

When the devices (*Figure 7a*) are operated in Standard ECL fashion, V_{EE1} may be off while V_{EE2} and V_{TT} remain on without causing a forward bias potential on any of the ESD diodes. Note that both the true and complement outputs of the ECL1 driver will source logic one current simultaneously to the V_{TT} supply when V_{EE1} is off while V_{TT} remains on. Emitter follower transistors of ECL1 are biased on to a logic high level by the V_{TT}/RT even in absence of V_{EE1}. The potential for V_{TT} current overload exists under these circumstances.

When V_{EE2} is powered off and V_{TT} remains on, the low rail input ESD diode of ECL2 (connected to V_{EE2}) will forward bias and conduct heavily as V_{TT} tries to re-power the V_{EE2} rail. The diode conduction will be limited by the RT resistor and the impedance of the off V_{EE2} supply in parallel with the ECL2 logic impedance. Although the ESD diode current density rating will typically support this current overstress, the recommendation is to avoid this by insuring that V_{EE2} and V_{TT} are ramped together and that V_{EE2} is never more positive than V_{TT} by 0.5V.

When the devices (*Figure 7b*) are operated in PECL fashion, there is a very clear forward bias hazard to ESD diodes when supplies are sequenced. If V_{CC2} is dropped before V_{CC1}, the positive referenced emitter followers of ECL1 will attempt to re-power up ECL2 through its high rail input ESD diode (connected to V_{CC}). The ECL emitter follower outputs are low impedance voltage sources (6Ω typical) and can source an incredible amount of current (greater than 200 mA each output). Thus V_{CC2} must never be more negative than V_{CC1} by 1.0V to avoid current overstress.

When V_{CC1} is powered off and V_{TT} and V_{EE2} remain on, the output ESD diode of ECL1 (connected to V_{CC1}) will forward bias and conduct heavily as V_{TT} tries to re-power the V_{CC1} rail. The diode conduction will be current limited by the RT resistor and the impedance of the off V_{CC1} supply in parallel with the ECL1 impedance. Although the ESD diode current density rating will typically support this current overstress, the recommendation is to avoid this by insuring that V_{TT} is never more positive than V_{CC1} by 0.5V.

If V_{CC1} and V_{CC2} are dropped while V_{TT} remains on, then V_{TT} tries to re-power both V_{CC} rails through the output ESD diode of ECL1 and the high rail input ESD diode of ECL2. The forward bias current is limited by the RT resistor and the V_{CC1}/V_{CC2} supply impedance in parallel with the collective logic impedance. This diode overstress is undesirable and should be avoided by insuring that V_{TT} is never more positive than V_{CC1} or V_{CC2} by more than 0.5V.

If V_{TT} is dropped before V_{CC1}, then increased load current can flow through the RT resistor from the emitter follower output of ECL1. Therefore V_{TT} ramping should be timed with V_{CC1} and V_{CC2}.

From the previous discussion, the most critical concern is that no PECL receiver should be powered down if driven directly by a powered up PECL driver without some form of current limiting. The inputs to the receiver must be current limited with external resistors of 100Ω or greater to be able to survive the overstress caused if V_{CC1} is ever permitted to be more positive than V_{CC2} by more than 1.0V. Although the use of current limiting resistors will alter the effective input edge rates and device propagation delays slightly, careful selection and placement of resistors will minimize device performance degradation. Use of surface mounted chip resistors located close to the input is recommended.

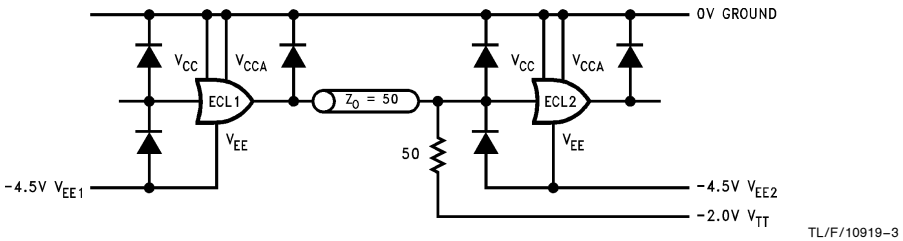

FIGURE 7a. ESD Diodes in Standard ECL Operation

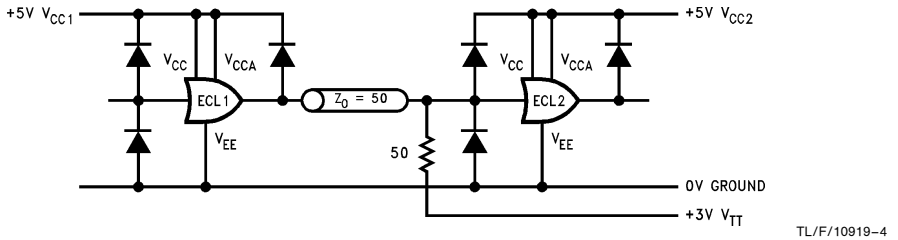

FIGURE 7b. ESD Diodes in PECL Operation

DUAL SUPPLY TRANSLATORS—THE CONVENTIONAL APPROACH

Dual supply ECL-to-TTL and TTL-to-ECL IC translators have been in general use for several years. These devices perform the logic level translations between ECL operating from a negative V_{EE} supply and TTL operating from a positive V_{CC} supply. This approach naturally allows each logic family to operate in their conventional and Data Book specified manner. System designers typically are most comfortable with the dual supply aproach. This conventional method permits the use of the most familiar design practice for ECL and should easily yield reliable mixed signal system operation. The growing list of F100K 300 Series Dual Supply Translators, as shown in *Figure 8*, is testimony to the continued popularity and versatility of this approach.

Features	100324	100325	100328	100329	100393	100395	100397	100398
Data Bits	6	6	8	8	9	9	4	4
ECL-to-TTL		X	X	X	X	X	X	X
TTL-to-ECL	X		X	X			X	X
Flow-Thru	X	X						
Latched			X		X		X	X
Registered				X		X		
ECL Differential Input		X[1]					X	X
ECL Differential Output	X						X	X
ECL Output Drive (Ω)	50		50	50			25	25
ECL Cutoff (Hi Z)			X	X			X	X
TTL Output Drive (mA) (I_{OL}/I_{OH})		20/−2	23/−3	24/−3	64/−15	64/−15	64/−15	64/−15
TTL TRI-STATE®			X	X	X	X	X	X
ECL Control Pins			X	X	X	X	X	
TTL Control Pins	X				X			X
TPD E to T (ns Max)		4.8	5.9	7.7	5.3	6.4	5.8	5.8
TPD T to E (ns Max)	3.0		3.8	3.9			2.4	2.2
I_{EE} (mA Max)	−70	−37	−169	−199	−39	−67	−99	−99
I_{EE} (mA Max) (Cutoff)			−169	−199			−159	−159
I_{CC} (mA Max)	38	65	74	74	65	65	36	45

[1] V_{BB} provided for Single-ended Operation

FIGURE 8. Table of F100K 300 Series Dual Supply Translators

SINGLE SUPPLY TRANSLATORS—THE NEW WAVE APPROACH

Single Supply Translators that allow PECL-to-TTL or TTL-to-PECL interfaces are a recent addition to the F100K 300 Series ECL family. Development of these devices is motivated by the need for a convenient technique by which higher performance ECL logic can be integrated into existing TTL systems containing a single positive supply. These devices should also provide a vehicle for new lower cost designs of mixed signal single supply systems.

Figure 9 describes three such devices being offered in the F100K 300 Series family. The popularity of PECL operation is expected to grow significantly as designers become more familiar with the technique. As interest and usage of Single Supply Translators increase, the family of this type of device can be expected to expand.

A simple illustration of the ease with which the Single Supply Translator can accomplish the interface from TTL to PECL and back to TTL is shown in *Figure 10*. Note that the translator devices have on chip V_{CC} partitions that facilitate the use of dual powerplanes for the preservation of ECL noise immunity. Differential operation on the PECL side of the translator is recommended to be used to maximize noise immunity. A V_{BB} reference voltage output is provided on the 100390 device to facilitate single ended operation.

Features	100390	100391	100392	100389
Data Bits	6	6	5	6
ECL-to-TTL	X			
TTL-to-ECL		X		
CMOS-to-ECL			X	X
ECL Differential Input	X[2]			
ECL Differential Output		X	X	X
ECL Output Drive (Ω)		50	25	50
ECL Cutoff (Hi Z)			X	
TTL Output Drive (mA) (I_{OL}/I_{OH})	24/−3			
TTL TRI-STATE	X			
TTL Control Pins	X	X		
CMOS Control Pins			X	X
TPD E to T (ns Max)	6.4			
TPD T to E (ns Max)		1.7		
TPD C to E (ns Max)			TBD	TBD
I_{EE} (mA Max) (Cutoff)			TBD	
I_{CC} (mA Max)	48	60	TBD	TBD

[2] V_{BB} provided for Single-ended Operation

FIGURE 9. Table of F100K 300 Series Single Supply Translators

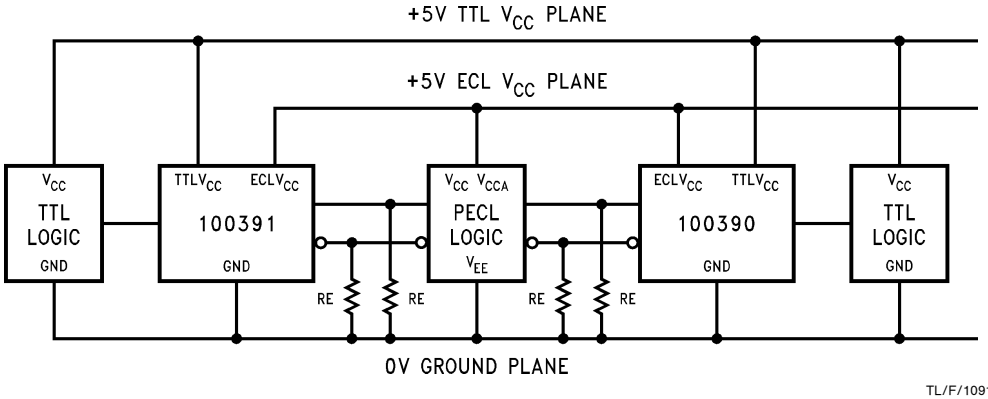

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FIGURE 10. Use of Single Supply Translators

Lit. # 100780

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