The Differences between BiCMOS III and BiCMOS IV

National Semiconductor
Application Note 705
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INTRODUCTION

National Semiconductor's proprietary one micron BiCMOS III process is used to produce our 64K and 256K density asynchronous SRAMs and our 2Kx9 Advanced Self-Timed (AST) SRAM. However, to produce the next generation of high performance, high density SRAMs, like our 1 M-bit density ECL I/O SRAM, National had to develop a new BiCMOS process. This new process, BiCMOS IV, features a minimum design rule of 0.8 microns and a minimum effective channel length of 0.55 microns.

NATIONAL'S BiCMOS ADVANTAGE

National's BiCMOS IV process is much more than a simple ''shrink'' of our BiCMOS III process. BiCMOS IV is the highly optimized result of years of bipolar and BiCMOS experience combined with the latest advances in semiconductor processing technology. We've taken advantage of the experience we've gained from working with BiCMOS since the early 80's. We've also applied the knowledge and learning that we've gained from working with our production BiCMOS III process. Plus, we've implemented some of the latest developments in semiconductor processing. And, we've taken advantage of techniques used in our performance leading ASPECT II bipolar process technology. As a result, National's new BiCMOS IV process has enabled our circuit designers to produce the fastest, densest and highest performance SRAMs available in the world.

Several key technological differences have enabled us to produce SRAMs that are not only denser, but feature higher performance transistors, improved interconnects, and enhanced reliability. Several key process differences are responsible for this improved performance, reliability and packing density. We've made changes in the buried layer formation, switched the oxide isolation to an advanced zero encroachment recessed oxide, changed to a silicided second polysilicon layer and switched to an all tungsten Metal-1 layer.

A simple design rule shrink would not have enabled us to get the degree of performance that we have demonstrated with BiCMOS III. The most important performance differences is that the BiCMOS IV process yields bipolar devices that demonstrate significant improvement over BiCMOS III. BiCMOS III bipolar transistors have a F_t of 8 GHz and BiCMOS IV bipolar devices have a F_t of 16 GHz. (See *Figure 1* .) These higher performance BiCMOS IV bipolar transistors have a minimum size that is one-fourth of the area of a minimum size BiCMOS III bipolar device.

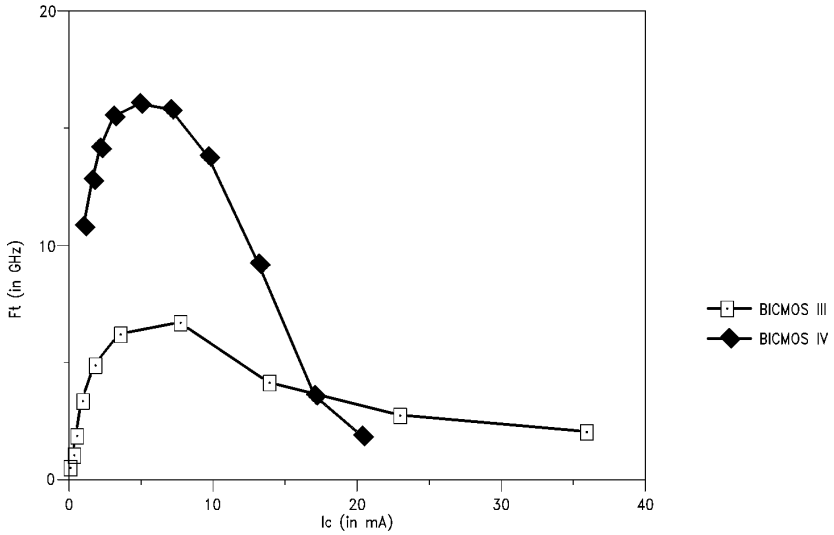

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FIGURE 1. F_t vs I_C for BiCMOS III and IV

  RRD-B30M75/Printed in U. S. A.

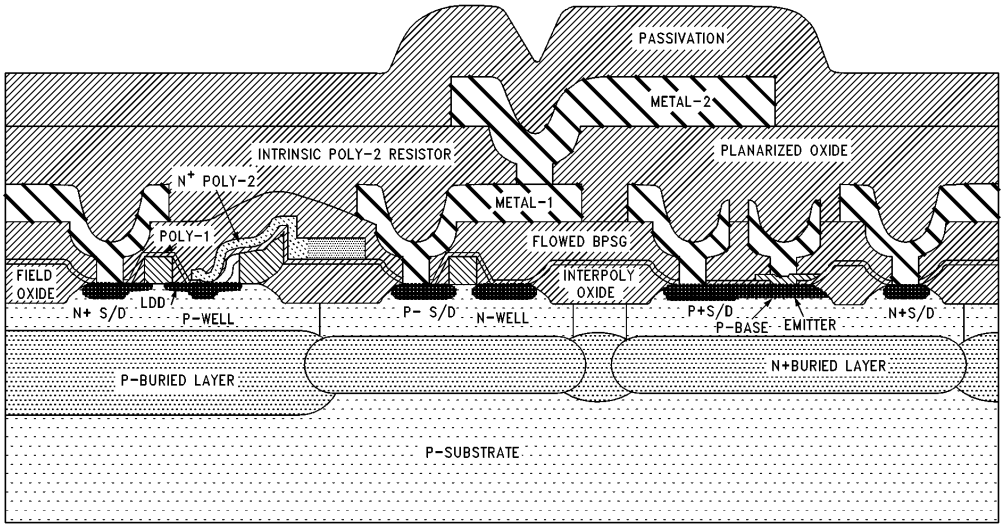
IMPROVED BURIED LAYER FORMATION

By making changes in our buried layer formation, we've been able to simplify the process flow, enhance reliability, and improve our device performance. We've changed the buried layer by increasing the doping levels and by laterally separating the buried layer regions.

We've enhanced the performance and reliability of the devices by increasing the doping levels in the buried layer. The p-type doping level in BiCMOS IV buried layer is five times that used in BiCMOS III. The n-type doping levels in BiCMOS IV buried layer represent a 40% increase over the BiCMOS III levels. By increasing the buried layer doping levels, we can improve latch-up immunity and lower the soft error rate.

A close-up of the buried layers is shown in *Figure 2*. You'll notice that the buried layers in the BiCMOS IV cross section are completely separated. In the BiCMOS III cross section, the two buried layers overlap. By separating these buried layers, we reduce the sidewall capacitances and as a result, improve performance. In BiCMOS processes, sidewall capacitance is a major performance limiting factor. These parasitic capacitances are further aggravated by having two overlapping heavily doped regions in the buried layer region. The junction capacitance created by this overlap is a small signal capacitance that degrades device switching time.

BiCMOS III



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BiCMOS IV

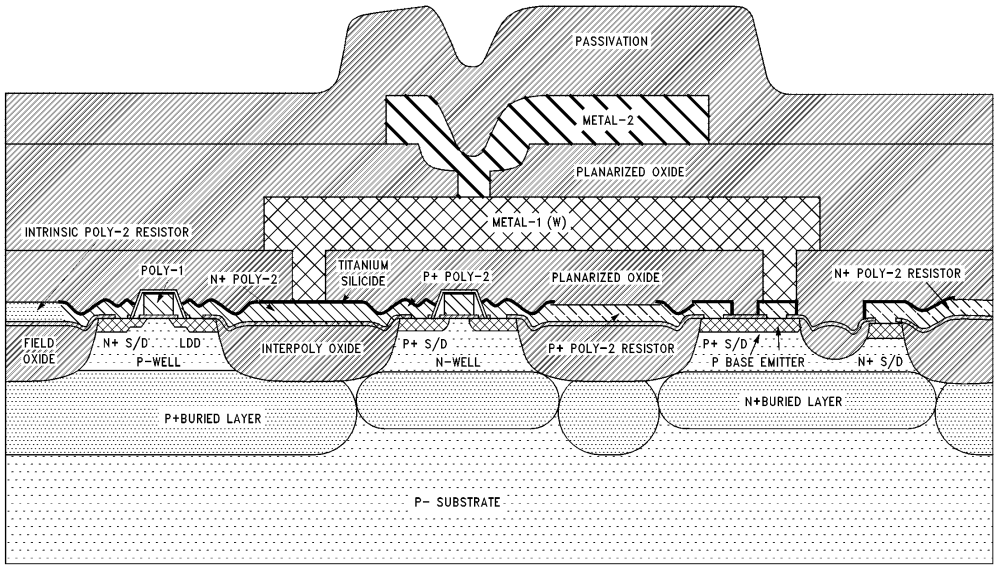

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FIGURE 2. Process Cross Section

ADVANCED OXIDE ISOLATION

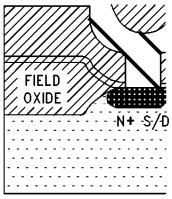
Figure 2 graphically shows the changes in the oxide isolation. Switching from a reduced bird's beak LOCOS (LOCal Oxidation of Silicon) to an advanced zero encroachment recessed oxide results in a highly planar process and also yields improved isolation, reliability, and packing density while significantly reducing sidewall capacitances.

From *Figure 2*, it's clear BiCMOS IV is a much more planar process than BiCMOS III. A major reason behind this improved planarity is the use of an advanced zero encroachment recessed oxide in BiCMOS IV. This new recessed oxide also improves our device isolation and extends the oxide isolation all the way down to the buried layer *(Figure 2)*. As a result, we've increased the field threshold for the parasitic transitors that are inherent in BiCMOS processes and thus, we've improved reliability.

Through the use of this recessed oxide we've been able to improve our overall packing density. In fact, our minimum size BiCMOS IV bipolar device takes up one-fourth of the area of the minimum size bipolar device in BiCMOS III. We can achieve this enhanced packing density in part because the advanced recessed oxide gives us an oxide isolated bipolar transistor and as a result the enclosure groundrules are reduced.

A major performance benefit from the use of a recessed oxide is a reduction of parasitic capacitances in the periphery of the devices. If you'll look carefully at the close-up view of the BiCMOS IV cross section shown in *Figure 3*, you'll notice that the field oxide regions are now directly adjacent to the N+ and P− regions. In the BiCMOS III cross section close-up view, you'll notice that there's a p-type silicon layer sandwiched between the isolation field oxide and the N+ area. A similar situation exists near the P+ source/drain areas. In BiCMOS III, this extra pn junction contributes a parasitic sidewall capacitance. In BiCMOS IV, this junction capacitance has been eliminated. As a result, sidewall capacitance has been reduced by a factor of 4, with the only capacitance coming from an oxide capacitance. Oxide capacitances are inherently much smaller than these junction capacitances.

BiCMOS III



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BiCMOS IV

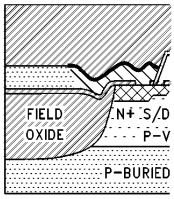

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FIGURE 3. Process Cross Section Closeup of Oxide Isolation

NEW SILICIDED POLYSILICON INTERCONNECT LAYER

BiCMOS IV uses the second polysilicon layer as an interconnect layer to improve packing density and reliability. This heavily doped poly layer is augmented by a titanium silicide layer on top of the interconnect areas. By using this silicided poly layer, we've improved packing density by having another interconnect layer (for short routing runs only). More importantly, we've enhanced reliability by eliminating metal contacts to all shallow junctions. By using this silicide poly to form contacts to active regions, we've reduced reliability problems like electromigration, metal-1 thermal stress at contacts, junction spiking, and other metal contact degradations.

The silicided poly is also used to reduce the number of contacts to Metal-1 by forming a short interconnect path between the contact region and the Metal-1 layer. Silicided poly can also be used to reduce the number of contacts to the Metal-1 layer. For example, without a silicided poly layer, connecting a CMOS inverter to an npn base would require two contacts and metal to connect the p-type poly to the n-type poly. A direct n-type poly to p-type poly connection would yield a poor quality diode. However, with a silicided poly layer, we're able to short the poly connection with a silicide and form good ohmic contacts.

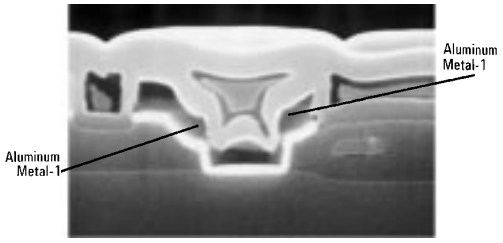
ENHANCED METAL-1 STEP COVERAGE

We've switched to an all tungsten Metal-1 layer to further enhance reliability and extend the product lifetime. The use of tungsten instead of aluminum dramatically improves step coverage. In *Figure 4*, you'll notice that the tungsten layer used results in a Metal-1 layer that has better uniformity throughout the layer. As a result, with an all tungsten layer, step coverage problems like thinning and cracking in nonplanar regions have been greatly reduced. Also, the all tungsten Metal-1 layer has greatly improved electromigration resistance. The close-up view of an aluminum Metal-1 layer in *Figure 4* shows great variation in thickness and high susceptibility to cracking and electromigration problems. This enhanced step coverage is also a result of the improved planarity in BiCMOS IV, which reduces step height and aspect ratio problems.

SUMMARY

National's new BiCMOS IV process is not a simple shrink down of our production proven BiCMOS III process. It's a highly optimized process that is a result of our extensive process learning with BiCMOS III combined with the latest developments in semiconductor processing technology. BiCMOS IV features improved buried layer formation, the use of an advanced zero encroachment recessed oxide, a silicided poly interconnect layer, and an all tungsten metal-1 layer. The changes we've made have resulted in a BiCMOS process with higher performance devices, improved packing density and enhanced reliability.

An Example of Poor Step Coverage Using an Aluminum Metal-1



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An Example Showing Enhanced Step Coverage Using a Tungsten Metal-1

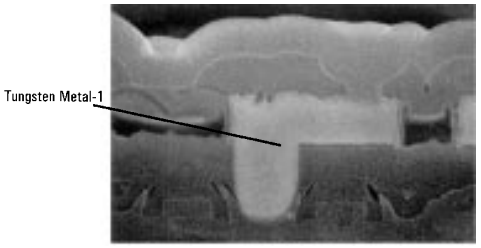

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FIGURE 4. Step Coverage Examples

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