Hot Carrier and Gate Oxide Reliability Characterization of National Semiconductor's BiCMOS IV Technology

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INTRODUCTION

In determining the reliability of a MOS process, it's important to consider two prime factors: gate oxide quality and the susceptibility of MOSFETs to hot carrier degradation. It's critical to have the ability to detect any weak devices that can lead to field reliability failures or parametric instability. Thus, National has placed major emphasis on in-line and end of line monitors, and on identifying processing steps which can improve the reliability of the BiCMOS IV process.

HOT CARRIER DEGRADATION

Today's MOS technology continues to advance to new levels, typified by National's BiCMOS IV 0.8 micron technology and 1 Megabit density SRAMs. However, as MOSFET channel lengths decrease to submicron levels, localized fields at the drain region increase. These strong localized fields can result in highly accelerated electrons. The high energy electrons may collide with the silicon lattice and create electron hole pairs (called ''impact ionization''). Some of the ''hot'' carriers that result from impact ionization can become trapped in the gate oxide or at the oxide interface. Many device parameters, such as threshold voltage and transconductance, are directly related to the amount of trapped charge. Over time, these hot carriers, as well as any charge generation from these injected carriers, can lead to parametric shifts. As a result, these parametric shifts can lead to decreased performance and even system nonfunctionality.

Device degradation is often measured in terms of percent shift in transconductance, G_m. G_m is the change in drain current with respect to the change in gate voltage at a constant drain voltage. In the BiCMOS IV technology, National has characterized G_m degradation through accelerated DC and AC testing of both p and n-channel MOSFETs. In DC stressing, the drain is held above 5.5V and the gate voltage is set to achieve maximum impact ionization current, which is measured using the substrate hole current. The time for 10% G_m degradation serves as a standard benchmark to show process stability and to study process effects on degradation.

For DC stressing, we're able to extract lifetime data by extrapolating back to a drain voltage of 5.0V or 5.5V to give the life under normal operating conditions. For DC stressing, we're able to form some qualitative comparisons on the process through a similar extrapolation. However, this qualitative comparison does not correlate directly to circuit lifetime. *Figure 1*, shown below, shows the stress testing data in terms of relative lifetimes.

For AC stressing, we use several test modes to simulate different circuit conditions. Inverter and SRAM pass gate circuits are the two most used stress conditions in simulating BiCMOS IV. The devices are stressed using a pulse generator with AC frequencies up to 10 MHz and with rise and fall times ranging from 100 ns down to 4.5 ns. AC testing shows degradation mechanisms that we can't see with DC

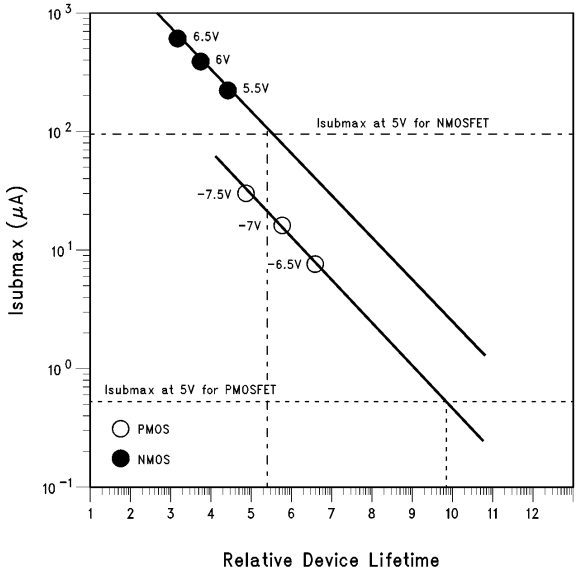

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FIGURE 1. BiCMOS IV P and N Channel Device Hot Electron Degradation Due to Accelerated DC Stressing Extrapolated to Determine Lifetime under Normal Operating Conditions

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stressing, and is therefore useful in understanding circuit lifetime.

In performing reliability characterization of BiCMOS III, National initially calculated lifetimes based on a 1% duty cycle determined through CMOS ring oscillator simulations. We later found that this calculation underestimated the actual lifetimes. With BiCMOS IV, we've done extensive characterization work through stressing ring oscillators and independently testing p-channel transistors. Through these ring oscillator tests, we're able to show more accurate lifetimes and develop a more comprehensive understanding of inverter operation and reliability.

Certain processing steps may further aggravate susceptability to hot electron degradation. During processing, hydrogen ions are introduced that may form weak Si-H bonds at the oxide surface. These ''loose'' bonds can be easily broken by hot carrier injection. In addition, plasma radiation can enhance this process. In BiCMOS IV processing, hydrogen can be introduced during the Silicon Nitride plasma deposition for the second passivation, through plasma bond etching, and through the final forming gas anneal.

To better understand total circuit effects, National is characterizing access time degradation on the 1 Megabit density devices through both static and dynamic burn-in at $-55°C$ and $V_{EE} = -6V$. For BiCMOS III and our 256K density devices, results from similar testing displayed no parametric shifts through 1000 hours of static burn-in. This result was expected, as it agreed with the preliminary AC hot electron data. Static and dynamic burn-in for BiCMOS IV is currently under way.

GATE OXIDE INTEGRITY

National uses Wafer Level Reliability (WLR) monitors in the BiCMOS IV process to identify possibly unreliable lots. Two gate oxide reliability monitors used are: Charge to Breakdown (Q_{bd}) measurements to monitor gate oxide integrity and possible susceptability to hot carrier degradation, and Fowler-Nordheim tunneling calculations to determine oxide thickness. These measurements are taken on test structures that lie in the scribe line in between the 1 Megabit die. National uses poly edge intensive capacitors with N+ junction regions and area intensive capacitors as the test structures because they best simulate actual transistors gates. The WLR reliability monitors have been very successful in detecting problems which result in both yield failures and decreased reliability.

The Fowler-Nordheim minimum oxide thickness is determined from current measurements taken during V-ramp testing. This test provides the oxide thickness at the thinnest, or weakest, point in the structure, unlike capacitive measurements which give an average thickness of the gate oxide. This measurement is particularly useful in detecting point defects or oxide thinning at the field edges, where localized high field regions can be created. In addition, this measurement helps detect unacceptably high bulk oxide charge levels.

In the Charge-to-Breakdown measurements, a constant current density is forced while the gate voltage is monitored for the onset of avalanche breakdown. Avalanche breakdown is defined as a 50% reduction in the gate voltage within a one second interval. Q_{bd} is calculated as being J $\times$ (time to avalanche) in units of Coulombs/cm^2. Q_{bd}, along with substrate current, has been found to correlate well with hot electron degradation for certain mechanisms in the BiCMOS IV process. Extensive evaluations, however, show that this correlation does not apply to all causes of low Q_{bd}.

SUMMARY

With reliability monitors and continued development, National is able to minimize and control the effects of hot carrier and gate oxide degradation. National's BiCMOS IV process also incorporates in-line and end-of-line WLR monitors to ensure high reliability. Fowler-Nordheim thickness and Q_{bd} measurements are two good indicators of weak gate oxides that may have possible susceptibility to hot carrier degradation. All of these enhancements and WLR monitors help to provide excellent process stability in BiCMOS IV.

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