JEDEC's "Revolutionary" SRAM Pinout Standard Helps Combat Noise in High Speed TTL I/O Systems

National Semiconductor
Application Note 709
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June 1990

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INTRODUCTION

In today's high-performance TTL I/O systems, SRAM speed is a critical issue. More often than not, the system speed is limited by the fastest SRAM cycle time available.

Using TTL I/O SRAMs at very high speeds introduces a critical design issue: how to avoid noise in the system. Noise is defined as any electrical signal present in a circuit other than the desired signal. Serious design considerations both from the system designer and the semiconductor manufacturer must be given to reducing system noise.

System designers must be well aware of the noise problems created by improper transmission line termination and inadequate power supply decoupling. On the component level, semiconductor designers can help reduce system noise by minimizing the power and ground lead inductance of their SRAM packages and by controlling the rate of change of the output current. Specifically, SRAM manufacturers can offer system designers higher speed and reduced noise devices by providing devices that adhere to the new JEDEC "Revolutionary" pinout standards.

National Semiconductor's 1 Megabit BiCMOS TTL I/O SRAM customers can gain the best speed and noise performance available because of National's use of the JEDEC "Revolutionary" pinout standard and because of other design features that manage noise.

SYSTEM NOISE SOURCES

With very fast TTL I/O SRAMS (15 ns to 20 ns for 1 Megabit densities), the key system design factors to controlling noise are the use of decoupling capacitors and matching termination impedance. These are especially important due to the very short rise and fall times associated with fast TTL I/O SRAMS.

Current spikes from outputs switching are a major cause of noise on power and ground. Supply decoupling is influenced by many factors, including printed circuit board power supply layout. The types and values of decoupling capacitor best for any given application may be determined experimentally, by observing supply noise in operation. As a general guideline, a systems designer should plan for decoupling capacitors of 0.02 μF to 0.1 μF distributed among the memories. Circuit board space for at least one capacitor per SRAM should be allowed. Subsequent experimentation may indicate that all capacitor sites need not be populated for adequate supply noise suppression. The capacitors chosen should be selected for low impedance at high frequencies; across the 20 MHz to 200 MHz range. For the most effective decoupling, the inductance from the SRAM device power supply leads to the decoupling capacitors should be kept at a minimum. Ideally, the capacitors could be placed next to the supply pins of the memory package, or possibly underneath the memory package between the supply pins. Decoupling capacitors may also be placed on the back side of the circuit board, directly behind each memory package.

A high impedance unterminated bus line acts like an antenna; it can radiate and receive electromagnetic interference (EMI). This can result in bus ringing, crosstalk and various other noise associated problems. The more transmission lines a bus has, the more antennas it has to pick up and radiate noise. The best way to reduce EMI is to ensure that the bus is properly terminated into a low-impedance load. Ideally, the termination resistor should be equal to the characteristic impedance of the bus line. This will provide the best incident wave switching and the least amount of signal reflection on the bus.

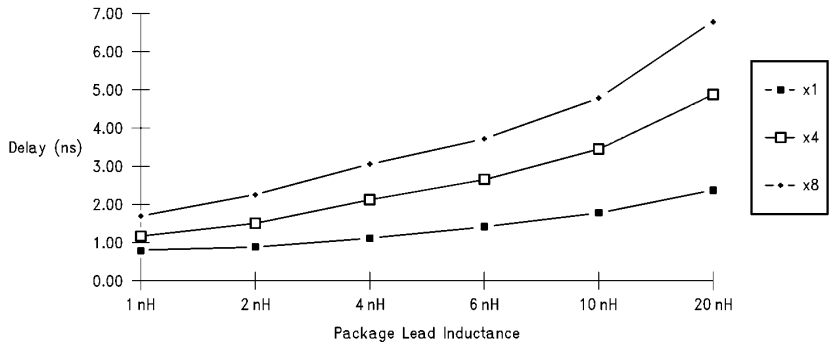

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FIGURE 1. TTL I/O SRAM Practical Output Delays vs. Package Lead Inductance (C_L = 30 pF, V_{OUT} = 1.5V and V_{GND} = 300 mV)

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When a reflected voltage arrives back at the driving transistor (due to an unmatched or improperly terminated line), the impedance of the transistor will determine the response. If neither the load termination or the source impedance matches the characteristic impedance of the transmission line, multiple reflections or ringing will occur until the voltage reflections are damped out. A more detailed discussion of transmission line theory can be found in National's *F100K ECL Logic Data Book and Design Guide.* The information contained in this publication is equally applicable to high speed TTL systems.

GROUND BOUNCE

Very fast TTL I/O SRAMs with wide data busses (4 to 8 bits or more) further complicate the noise issue. Having many data outputs leaves open the possibility that many or all of the output drivers can switch at the same time,. If a 128K x 8 TTL I/O SRAM's 8 outputs all switched from ''1's'' to ''0's'' at the same time, the output drivers would place a large demand for current on the single ground conductor (the lead frame of the chip and the bond wire) that brings ground on and off the chip. Such an abrupt transition could temporarily raise the ground potential of the chip, causing what is commonly referred to as ground bounce.

This change in ground voltage (or supply voltage if all outputs switched from ''0's'' to ''1's'') is mainly due to a voltage drop (ΔV_{GND}) over the package lead and bondwire inductance L. This voltage drop is given by:

$$\Delta V_{GND} = L \frac{\Delta i}{\Delta t} \quad (1)$$

where i = total current through the output drivers. In most cases, this is equal to the total output load charging or discharging current. Theoretically, the charge necessary to switch the output current is given by:

$$q = C_L \Delta V_{OUT} = \frac{\Delta i \Delta t}{2} \quad (2)$$

Where ΔV_{OUT} is the voltage swing at the output. To maximize the output switching speed, a static RAM should utilize an output buffer that ramps current up at a constant $\Delta i/\Delta t$ (equal to the tolerable $\Delta V_{GND}/L$) to a maximum i, then ramp down at the same constant $\Delta i/\Delta t$. Combining equations (1) and (2) yields the relationship between the discharging or charging time (Δt) of an output capacitive load and the voltage drop ΔV_{GND}:

$$\Delta t = \sqrt{\frac{2C_L \Delta V_{OUT} L}{\Delta V_{GND}}} \quad (3)$$

where Δt is the theoretical minimum output switching time that can be achieved. Assuming certain values for ΔV_{OUT}, C_L and ΔV_{GND}, *Figure 1* shows the speed gains that can be achieved by minimizing ground inductance of the SRAM package. Note that the x8 configuration is inherently slower due to the 8x capacitive load (C_L).

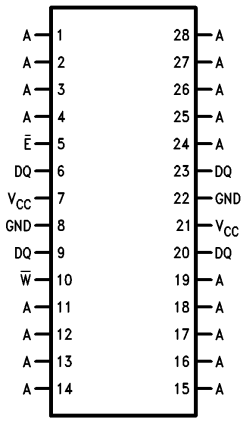
High speed TTL I/O SRAM manufacturers can provide their customers with higher speed, reduced noise devices by careful circuit design and by minimizing the power and ground lead inductance of their SRAM packages.

THE ''REVOLUTIONARY'' PINOUT SOLUTION

JEDEC (Joint Electron Device Engineering Council— the industry standard setting body) has adopted a new pinout standard for very fast TTL I/O SRAMs (20 ns and below at 1 Megabit density) known as the ''Revolutionary'' pinout standard.

The Revolutionary pinout standard features dual power and ground pins in the center of each sides of the IC package. For slower TTL I/O SRAMs (access times greater than 20 ns), JEDEC supports the ''Evolutionary'' pinout standard, featuring a traditional single corner power and ground pinout. The JEDEC Revolutionary and Evolutionary pinouts are shown in *Figure 2* for 256K x 4 TTL I/O SRAMs.

JEDEC Standard Revolutionary Pinout
Center Power and Ground



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JEDEC Standard Evolutionary Pinout
Corner Power and Ground

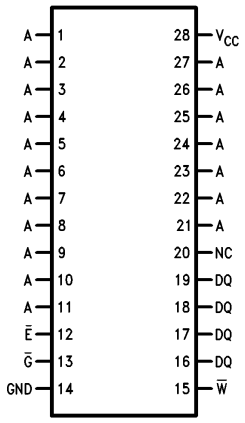

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FIGURE 2. JEDEC Revolutionary and Evolutionary Standard Pinouts for 256K x 4 TTL I/O SRAMs

The Revolutionary pinout reduces lead inductance in the supply leads in several ways. First, as shown in *Figure 3*, the Revolutionary pinout has a much shorter leadframe than is possible with an Evolutionary pinout package. The lead inductance for the Revolutionary pinout can be approximately 2–4 nH, when compared to that of the Evolutionary pinout's approximate 6–10 nH, realizing an immediate increase in switching speed (shown in *Figure 1*). Second, having two power and ground inductors creates an inductance that combines in parallel to reduce the inductance from between 2 nH–4 nH to 1 nH–2 nH, further improving the speed-noise tradeoff. Third, a mutual coupling between power and ground is created, reducing the effective series inductance. Finally, by double bonding each power and ground pad, semiconductor manufacturers can reduce the effective bondwire inductance even further.

To achieve sub-20 ns speed for the next generation of 1 Megabit TTL I/O SRAMs, it is simply not efficient for semiconductor manufacturers to design their devices with the Evolutionary pinout. Excessive inductance would cause the very fast Evolutionary-style devices to be extremely noisy.

ADDITIONAL SYSTEM BENEFITS OF JEDEC's "REVOLUTIONARY" PINOUT STANDARD

In addition to minimizing switching noise, the Revolutionary pinout standards carry two additional system design-in benefits. First, power, data and control pins remain fixed as pinous migrate upward in density from 1 Megabit to 16 Megabit density SRAMs. Shown in *Figure 4* are the 1M to 16M JEDEC standard pinouts for very fast TTL I/O SRAMs. The system designer can now much more easily design around future products as higher density memories are developed, no longer causing extensive board redesigns and higher costs to upgrade.

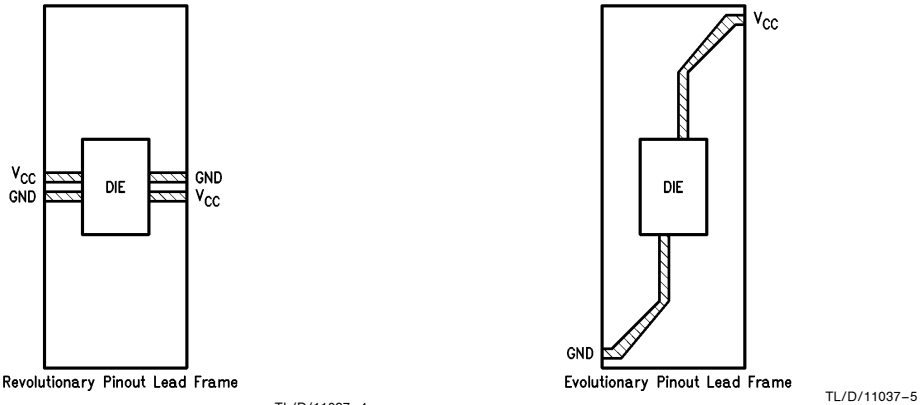


FIGURE 3. Revolutionary and Evolutionary Pinout Lead Frames

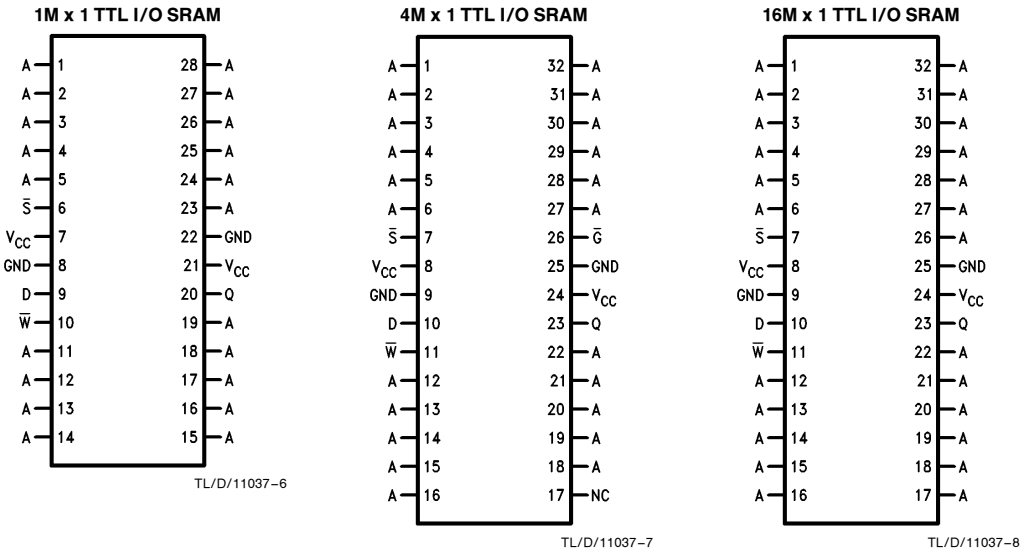


FIGURE 4. JEDEC Standard Revolutionary Pinouts for 1M x 1, 4M x 1 and 16M x 1 TTL I/O SRAMs

Second, today's Evolutionary pinouts do not have any commonality between bit wide (x1), nibble wide (x4) and byte wide (x8) pinouts *(Figure 5)*. This results in multiple devices and higher costs passed on to the consumer, because the manufacturer simply cannot use the same die to service more than one configuration. However, with today's Revolutionary standards, the consistent pinout will allow simple options to create one die to function as x1, x4 and x8 organizations in the same density. The manufacturer will also be able to pass on this shorter product development cycle (normally not all organizations are available in the same time frame) in terms of cost, quality and manufacturability to the customer.

SUMMARY

High-speed TTL I/O system designers must be very careful when dealing with system noise issues, including decoupling power supplies adequately and terminating transmission lines properly.

Very high-speed TTL I/O SRAM manufacturers must be equally as careful in providing their customers with the fastest, least noise generating product possible. The creation of the new JEDEC Revolutionary Pinout Standards has made this universally possible.

National Semiconductor is committed to helping its customers of very fast BiCMOS SRAMs gain the highest performance possible from their systems. By introducing very fast 1 Megabit BiCMOS TTL I/O SRAMs, with the JEDEC Revolutionary Pinout Standard and carefully designed on-chip output drivers, National's customers can gain a huge performance edge with a superior speed-noise optimization.

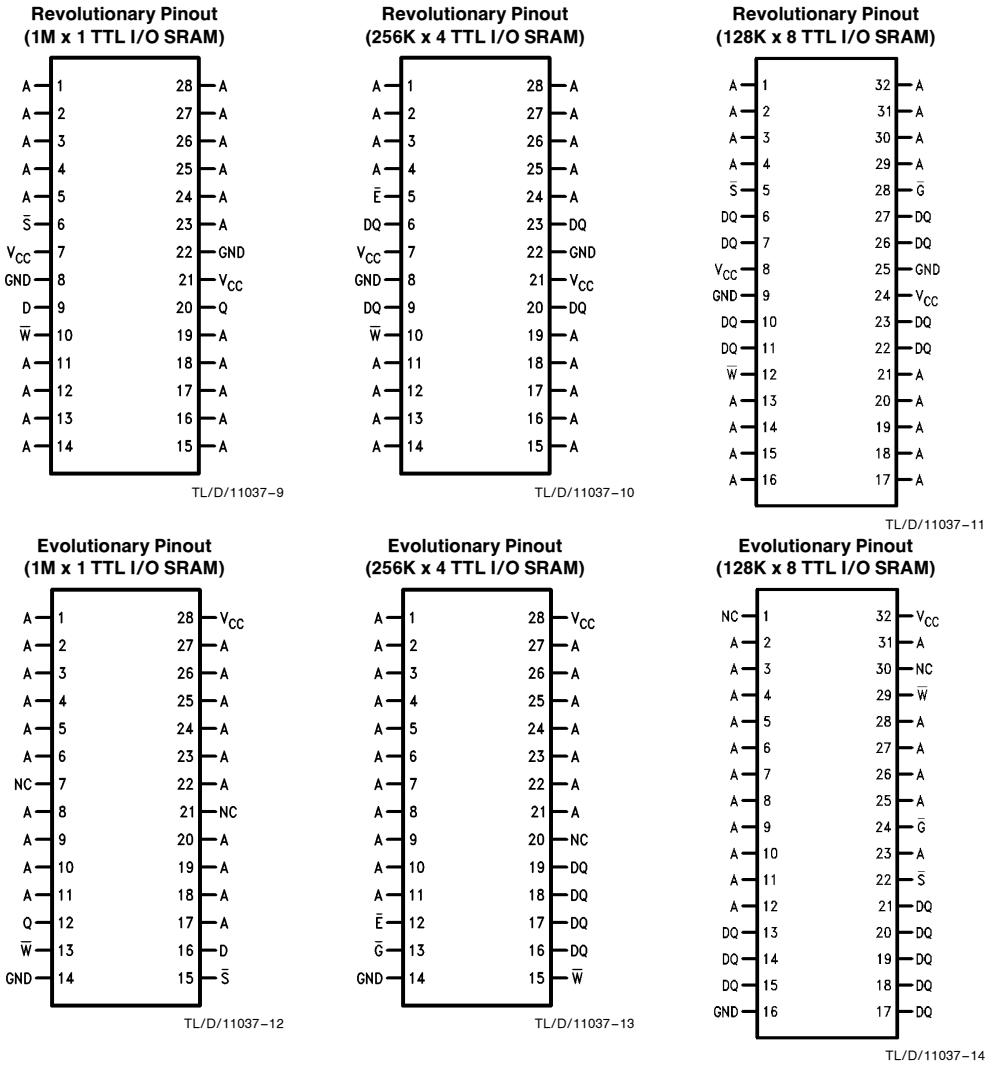
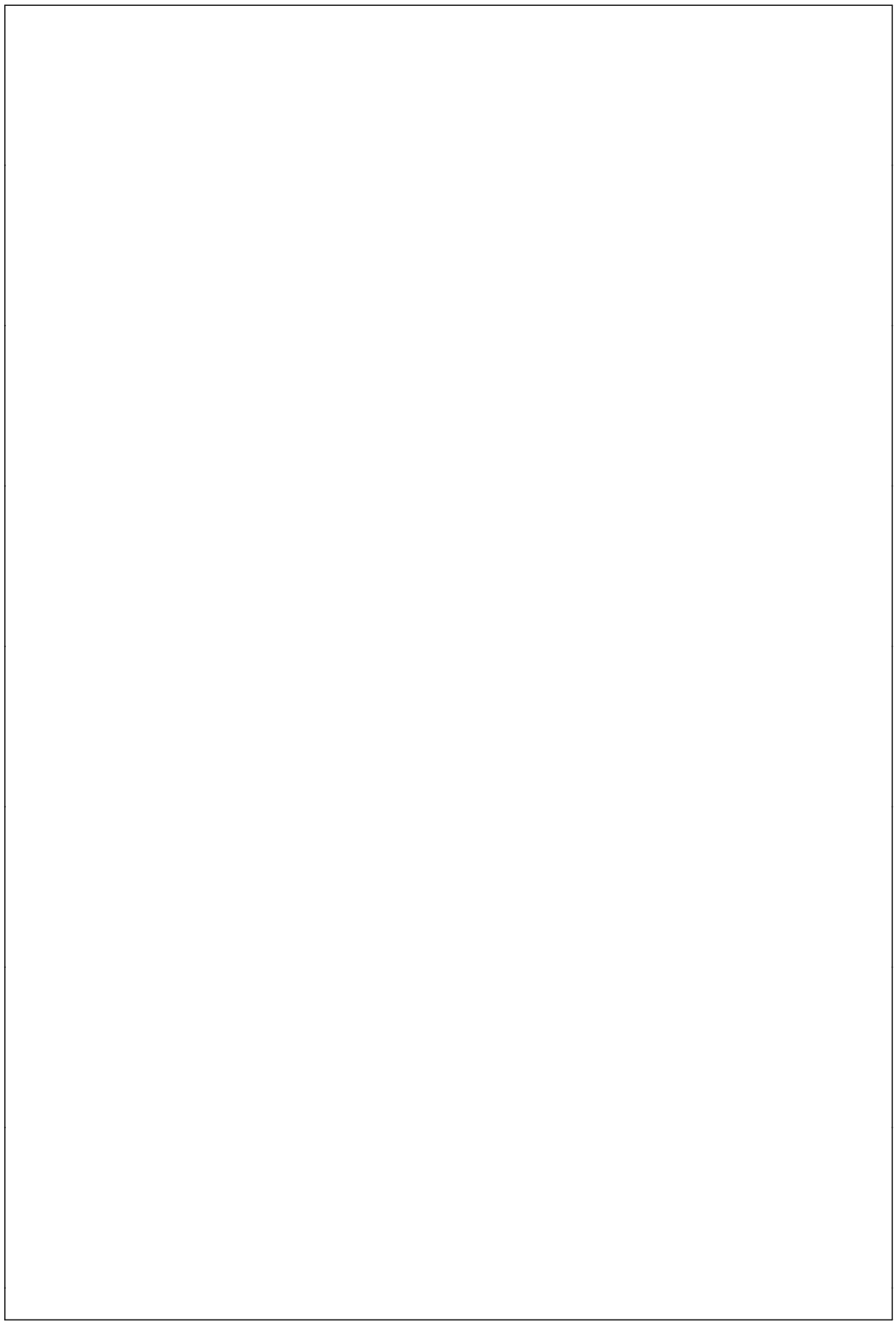


FIGURE 5. JEDEC Standard Revolutionary Pinouts (Above) and Evolutionary Pinouts (Below) for 1M x 1,256K x 4 and 128K x 8 TTL I/O SRAMs



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