Designing with National's High Performance CMOS EPROM

National Semiconductor
Application Note 717
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September 1990

INTRODUCTION

The purpose of this application note is to inform the system designer of possible pitfalls of using high speed EPROM. In older generation EPROM the fastest commonly available data access times were 150 ns and 100 ns, but with the current generation EPROM, data access times of less than 100 ns are common, and this is true of National Semiconductor's family of 1.2 micron (0.9 Leff) EPROM. This family of EPROM is differentiated from other National EPROM by using a part number prefix of NM rather than NMC. For availability of specific part numbers and speeds contact your local National Semiconductor sales office or franchised distributor.

The problems that are encountered are typically seen as noise on the data-out lines, noise on the data-in lines, or possibly noise on the control signals. The cause of the noise must be understood to truly eliminate it.

In EPROM chip design, there are several ways to decrease the overall data access time. The major areas are:

1. Memory Cell—Designers are always looking for ways to decrease the size of the memory cell as this significantly affects the total die size. Typically as the memory cell becomes smaller, the cell current becomes less, and as the cell current becomes lower, the delay at the sense amplifier has to be increased to assure correct data is being read. On the other side of the issue, overall smaller die sizes and smaller geometries bring higher speed, therefore the actual speed improvement realized depends on the design.
2. Interconnect Technology—By decreasing the resistance of the poly-silicon interconnects lines in the EPROM, the device can be significantly faster. This is one of the few speed enhancements that doesn't carry a significant penalty in some other area.
3. Output Buffers—The output buffers on EPROM have typically had a 35 ns to 45 ns transition time (10% to 90%). This is done to avoid ground bounce internal to the device as there are 8 simultaneous switching outputs. Very fast output buffers are sometimes used, but requires specific PC Board layout and decoupling.

National Semiconductor has used an aggressively small memory cell in conjuction with a patented adjustable sense amplifier delay to optimize speed in the first area. Second, the interconnect is polycide, which is a modified poly silicon interconnect layer with significantly lower resistance. Finally, a moderately fast output buffer transition time was selected. It was deemed that a 30 ns transition would still meet designers needs for layout of two layer PC Boards without noise and provide a significant speed enhancement. The test circuit used to measure the output transition is shown in *Figure 1.*

As mentioned earlier, using the faster EPROM may cause noise to show up in several areas not directly related to the output buffers. When the 8 output buffers switch they cause current to be injected into the ground of the EPROM, and this high frequency current spike results in a ground reference that is not the same at all points within the EPROM. As a result of this ''ground bounce'' the reference for the inputs into the EPROM is temporarily altered. There is sufficient margin built into the EPROM to account for this internal noise and still meet the specification, although if the input signals are marginal or the ground to the EPROM is highly inductive the inputs are likely to detect a transition. A transition on the address inputs will cause the EPROM to begin a new data access cycle, thus delaying the valid data at the Q outputs by an amount equal to the T_{ACC}.

There are several modifications that can be implemented on an existing design without altering the PC layout that will

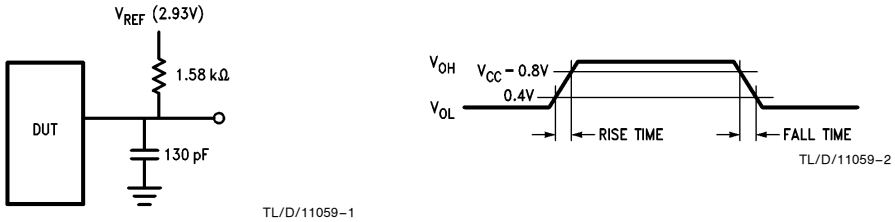

FIGURE 1. Output Transition Time Measurement

  RRD-B30M75/Printed in U. S. A.

overcome the problem, although the best solution is to use these modifications in the circuit design as well as follow some specific PC layout rules. The non-layout modifications are as follows:

1. Improve the input high voltage levels to the EPROM. The goal of this modification is to provide as much V_{IH} margin as possible so that more ground bounce can be tolerated. This can be accomplished in several ways. Many systems use a resistor from the signal line to V_{CC} to avoid oscillation while the line is in the high impedance mode (or in the case of a OC output the resistor is mandatory). If the minimum V_{IH} observed is at or near the specified 2.0V V_{IH} of the EPROM (it should be at 2.4V minimum for reasonable margin and system to system variation) the pull-up resistor value should be decreased. Most output drivers (1.2 mA) can guarantee a good V_{IL} with a 4.7 kΩ pull-up resistor, or in the case of an output driver capable of 800 μA a 7 kΩ resistor is a reasonable minimum. It may not be necessary to use such a low value resistor. A minimum value resistor can be selected simply by applying ohm's law as follows:

$$\frac{\text{Max } V_{CC} - V_{IL} \text{ of EPROM}}{\text{Max } I_{OL} \text{ of driver} - \text{Max } I_{IL} \text{ of total loads on driver}} = R$$

   Max V_{CC} is maximum voltage of the voltage supply to the resistor.

   V_{IL} of EPROM is the maximum input low voltage of the EPROM. In this case it is 0.8V. It is good to allow margin so using 0.45V is conservative.

   Max I_{OL} of driver is the maximum output low current the driver is capable of at the V_{IL} level assumed above.

   Max I_{IL} of total loads on driver is the sum of all currents at the node excluding the current of the resistor.

   Using this method a pull-up resistor value can be selected that will aid in providing the best V_{IH} while guaranteeing a V_{IL} with good margin. Since the ground bounce problem is normally a problem that affects the Input High Threshold, the V_{IH} should be given the most margin.

2. A second method of improving V_{IH} to the EPROM and thus making the EPROM more immune to ground bounce is to use latches or drivers that have a better V_{OH}. Many CMOS devices will drive a V_{OH} near V_{CC} making them an excellent choice for this application.

3. Improving the ground connection (making it less inductive) can have significant impact. If the EPROM has a ground connection that is capacitive rather than inductive and is closely coupled to the drivers (in respect to signal and ground), steps 1 and 2 above may not be necessary. To accomplish a low inductive/high capacitive ground supply, each device should have a ceramic capacitor in the range 0.1 μF to 0.47 μF, or similar. In addition there should be a charge storage capacitor electrically close. This should be similar to an aluminum electrolytic in the range of 4.7 μF to 15 μF. *Figure 2* shows a satisfactory 2-layer PC board layout using latches on all address lines. Typically only eight of the address lines will require latches and the other address lines will be directly driven from the micro, this is only to demonstrate a sound layout including capacitors and power connections.

   Many systems use dedicated layers in the PC board for V_{CC} and ground. In these systems there is little to be concerned about due to the excellent characteristics of this approach. Equally satisfactory results can also be obtained with routed V_{CC} and ground, but close attention must be given to the result.

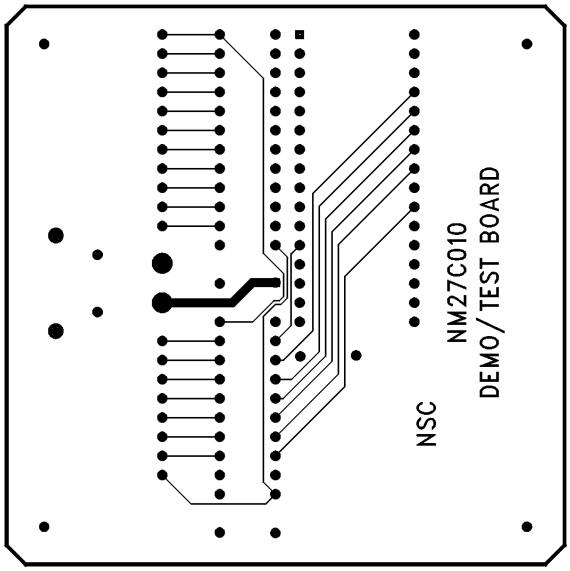

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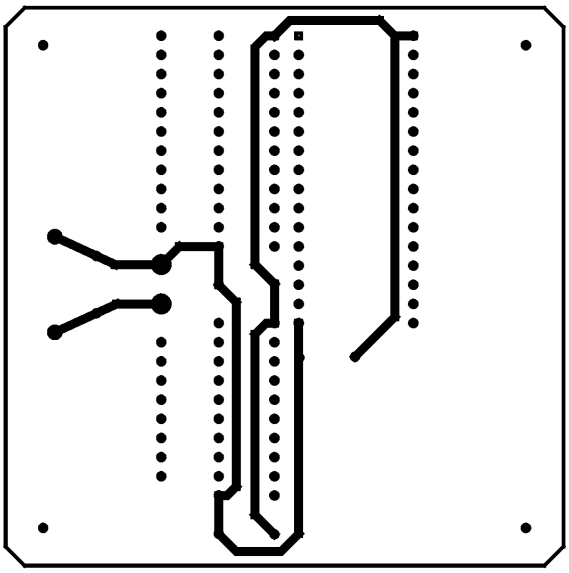
FIGURE 2. 2-Layer PC Board Layout



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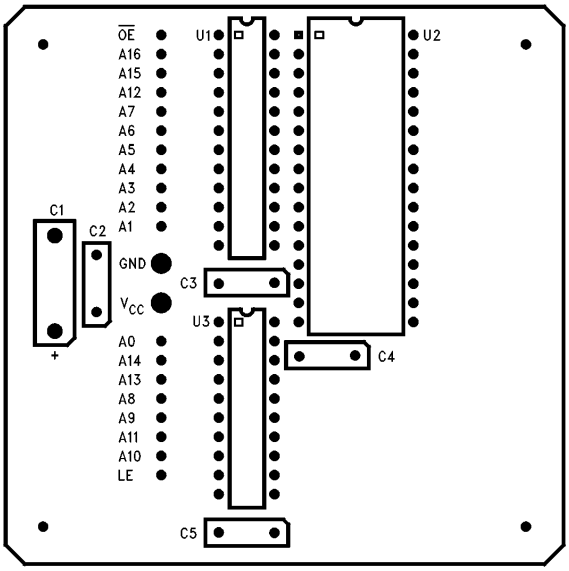

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U1 = DM74ACT
U2 = NM27C010N90
U3 = DM74ACT373N
C1 = 4.7 μF capacitor
C2–C5 = 0.47 μF capacitor

FIGURE 2. 2-Layer PC Board Layout (Continued)

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