Description of the NS32CG160 Bus Fairness Mechanism

National Semiconductor
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INTRODUCTION

This application note describes the Bus Fairness Mechanism in the NS32CG160 Integrated System Processor. The NS32CG160 is composed of a 32-bit CPU, a Direct Memory Access Controller (DMAC), an interrupt control unit (ICU), timers, and a BitBLT Processing Unit (BPU). The Bus Fairness Mechanism is a programmable feature designed to enable the NS32CG160 user to control the bus arbitration between the CPU and the DMAC.

The note is divided into 3 sections. Section 1 presents a general description of the DMAC, including the bus arbitration and bus fairness mechanisms.

Section 2 presents a complete description of the bus fairness mechanism and its parameters.

Section 3 presents examples of different bus fairness parameters and their effect on NS32CG160 behavior.

1.0 BACKGROUND

The DMAC supports two channels for transferring blocks of data between memory and I/O devices with minimal CPU intervention. Each channel uses FLYBY mode only. This means that at least one end of each channel is an I/O device.

Bus fairness between the CPU and the DMAC gives a low priority device the chance to gain control of the bus even though a higher priority device is requesting control at the same time. The bus fairness mechanism is user programmable.

The DMAC enters the bus acquisition state (to obtain control of the bus) when it detects a channel request signal on the corresponding DMA channel REQUEST ($\overline{DRQ}$) pin. The subsequent bus arbitration is done using a fixed priority scheme. The priority scheme is ordered as follows: HOLD request has the highest priority, followed by channel 0, then channel 1. The CPU has the lowest priority.

Once the bus is granted in response to a DMA channel request and no higher priority request is pending, the selected channel can use the bus for a certain number of back-to-back transfers before it is forced to relinquish the bus. The determination of when to relinquish the bus is controlled by the bus fairness mechanism. This mechanism prevents a DMAC channel from monopolizing the bus. The maximum number of back-to-back transfers can be programmed through the Block Transfer Length (BLT) field in the Mode Control register. The channel relinquishes the bus for at least one cycle after the programmed number of transfers is complete. This frees the bus for a lower priority request.

Note: The CPU has priority over the second channel during the cycle when the bus is released because of the bus fairness mechanism. Note that except for this instance, the second channel always has priority over the CPU.

2.0 DESCRIPTION

The bus fairness mechanism is controlled by the Mode Control Register BLT field (bits [10:14]) *(Figure 1)*. Since each channel has its own MODE register each channel can have different parameters for bus fairness.

The fields for these parameters are:

BWA— Device A Bus Width Bits [7:8] of Mode Register
- 00— 8 Bits Bus Width
- 01— 16 Bits Bus Width
- 10— (Reserved)
- 11— (Reserved)

BLT— Block Length Transfer Bits [10:14] of Mode Register.

Table I presents a functional description of each combination within the BLT field and describes the maximum number of back-to-back transfers for different values of BLT field in MODE control register.

31 15	14 10	9	8 7	6	5 4	3	2	1	0
RESERVED	////////// blt //////////	ada	//////// bwa ////////	0	0 0	dir	0	res	0t

FIGURE 1

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TABLE I

BLT in Mode Control Reg. Bits [10:14]	Functional Description	BWA = 00	BWA = 01
00000	DMAC will not relinquish the bus unless the respective DRQ pin is deasserted, or the block transfer is completed.	Unlimited	Unlimited
00001	DMAC will relinquish the bus after each transfer.	1	1
00010	DMAC will relinquish the bus whenever the least significant bit of Transfer Complete Counter (TCC) equals 0. The TCC counts the number of bytes transferred.	2	1
00100	DMAC will relinquish the bus whenever the two least significant bits of the TCC equal 00.	4	2
01000	DMAC will relinquish the bus whenever the three least significant bits of the TCC equal 000.	8	4
10000	DMAC will relinquish the bus whenever the four least significant bits of the TCC equal 0000.	16	8

3.0 EXAMPLES

This section contains a number of examples of how to use the bus fairness mechanism. A table at the beginning of each example describes the parameters to be programmed and their meaning. Each table is followed by a timing diagram that describes the behavior of the NS32CG160 under those circumstances.

Example 1

The DMAC relinquishes the bus after each transfer. Each transfer is 1 byte because the bus width is 1 byte. The CPU obtains control of the bus as soon as the DMA relinquishes it (Table II).

TABLE II. Parameters for Programming the DMAC to Relinquish the Bus after Each Byte Transfer

Bus Fairness Parameters	Values	Description
BWA Field	0 0	Bus Width is 8 Bits (BYTE)
BLT Field	0 0 0 0 1	DMA relinquishes the bus after each transfer.
MODE CONTROL REGISTER	H'608	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 1; Source is Memory Buffer BLT (see above)

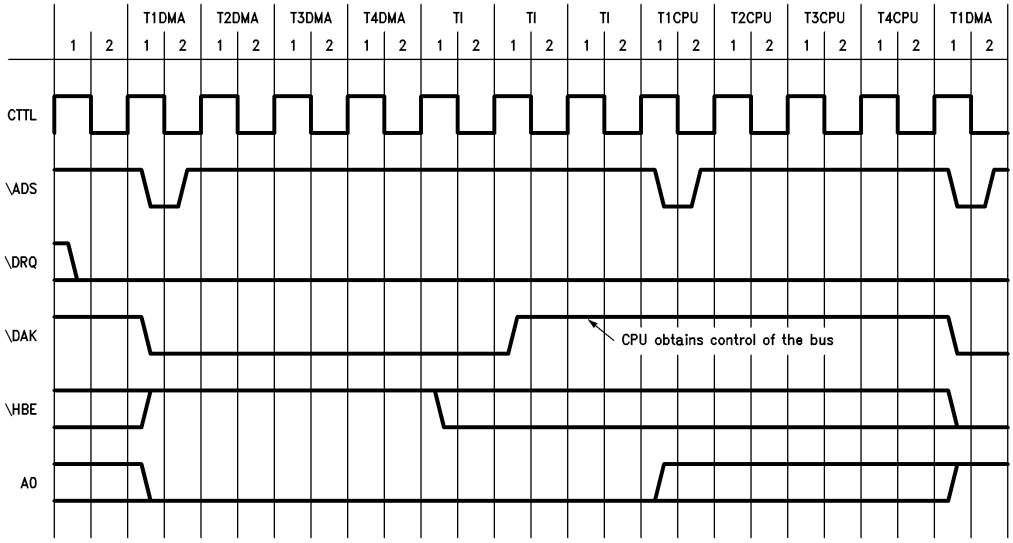

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Diagram 1

Example 2

The DMAC relinquishes the bus after each transfer. Each transfer is 1 word because the bus width is 1 word. The CPU obtains control of the bus as soon as the DMAC relinquishes it.

TABLE III. Parameters for Programming the DMAC to Relinquish the Bus after Each Transfer

Bus Fairness Parameters	Values	Description
BWA Field	0 1	Bus Width is 16 Bits (WORD)
BLT Field	0 0 0 0 1	DMAC relinquishes the bus after each transfer.
MODE CONTROL REGISTER	H'488	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 0; Source is an I/O Device BLT (see above)

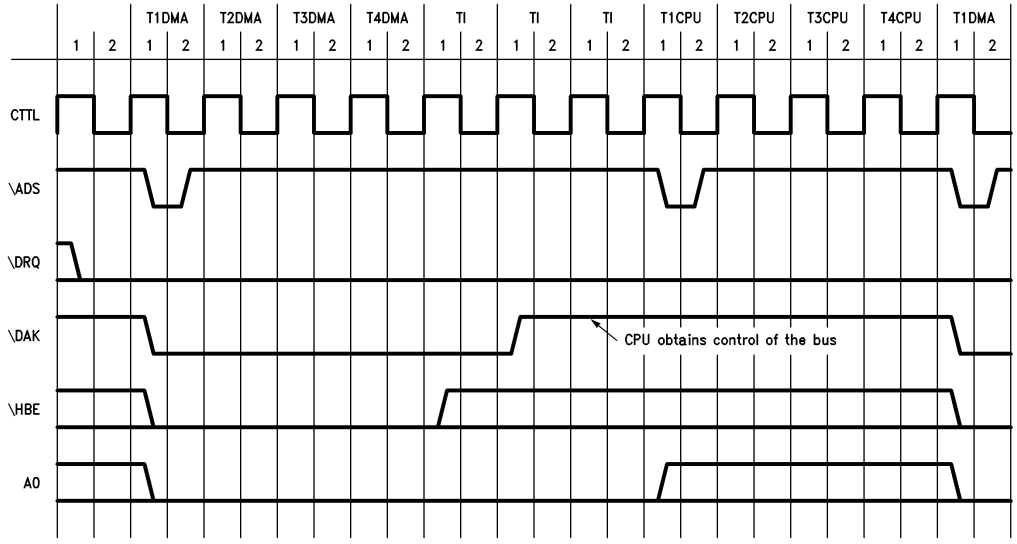

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Diagram 2

Example 3

The DMAC relinquishes the bus after each transfer. The bus width is 1 byte, therefore the DMAC performs two back-to-back byte transfers and then relinquishes the bus for one cycle. The CPU obtains control of the bus as soon as the DMAC relinquishes it.

TABLE IV. Parameters for Programming the DMAC to Relinquish the Bus after Each Word Transfer (Bus Width is of 1 Byte therefore Number of Back-to-Back Transfers is Two)

Bus Fairness Parameters	Values	Description
BWA Field	0 0	Bus Width is 8 Bits (BYTE)
BLT Field	0 0 0 1 0	DMAC relinquishes the bus after each word transfer.
MODE CONTROL REGISTER	H'A08	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 1; Source is Memory Buffer BLT (see above)

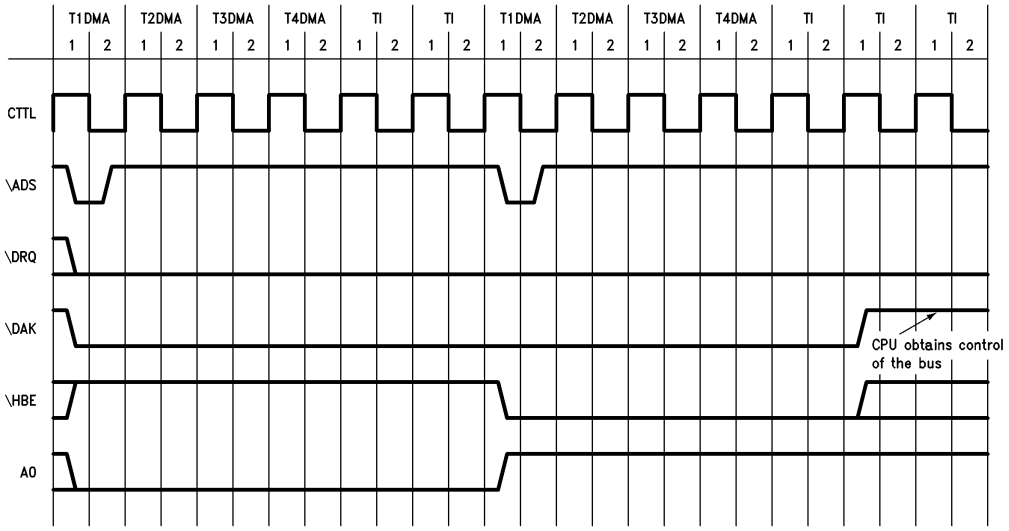

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Diagram 3

Example 4

The DMAC relinquishes the bus after each word transfer. The bus width is 1 word, therefore the DMAC performs a 1 word transfer and relinquishes the bus for one cycle. The CPU obtains control of the bus as soon as the DMAC relinquishes it.

TABLE V. Parameters for Programming the DMAC to Relinquish the Bus after Each Word Transfer (Bus Width is of One Word, therefore Bus is Relinquished after Each Transfer)

Bus Fairness Parameters	Values	Description
BWA Field	0 1	Bus Width is 16 Bits (WORD)
BLT Field	0 0 0 1 0	DMAC relinquishes the bus after each word transfer.
MODE CONTROL REGISTER	H'A88	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 1; Source is Memory Buffer BLT (see above)

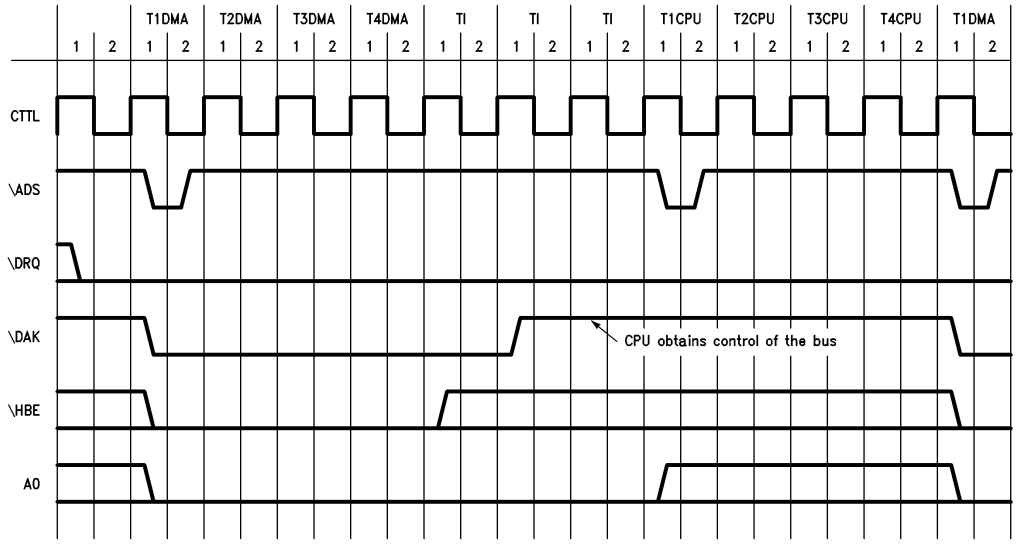

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Diagram 4

Example 5

The DMAC relinquishes the bus after each double-word transfer. Each bus width is 1 word, therefore the DMAC performs 2 back-to-back word transfers and relinquishes the bus for one cycle. The CPU obtains control of the bus as soon as the DMAC relinquishes it.

TABLE VI. Parameters for Programming the DMAC to Relinquish the Bus after Each Double-Word Transfer (Bus Width is of One Word, therefore Bus is Relinquished after 2 Back-to-Back Word Transfers)

Bus Fairness Parameters	Values	Description
BWA Field	0 1	Bus Width is 16 Bits (WORD)
BLT Field	0 0 1 0 0	DMAC relinquishes the bus after each double-word transfer.
MODE CONTROL REGISTER	H'1088	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 0; Source is an I/O Device BLT (see above)

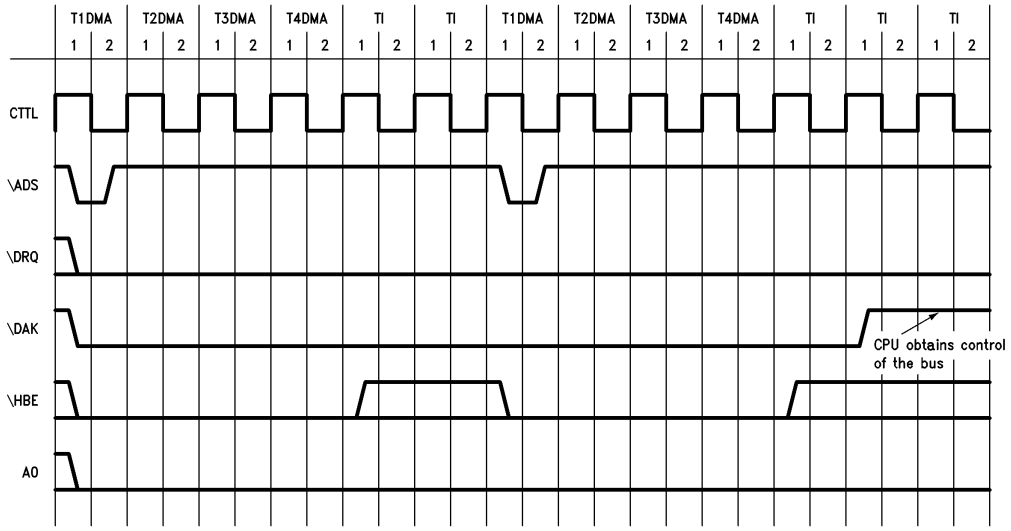

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Diagram 5

Example 6

Example 6 presents the case in which the DMAC relinquishes the bus, but the CPU does not obtain control of the bus, because it doesn't need the bus. This may occur when the CPU is in a middle of executing a long instruction at the time that the DMAC relinquishes the bus. Diagram 6 shows what happens when the DMAC obtains control of the bus for another byte transfer after it relinquishes the bus after each byte transfer for 1 cycle, and as the CPU does not apply for the bus. After the idle bus cycle the DMAC is granted the bus for another transfer.

TABLE VII. Parameters for Programming the DMAC to Relinquish the Bus after Each Transfer (Bus Width is of One Byte, therefore Bus is Relinquished after Each Byte Transfers)

Bus Fairness Parameters	Values	Description
BWA Field	0 0	Bus Width is 8 Bits (BYTE)
BLT Field	0 0 0 0 1	DMAC relinquishes the bus after each transfer.
MODE CONTROL REGISTER	H'608	OT = 0; Auto-Initialize Off DIR = 1; Write Cycle in Flyby BWA (see above) ADA = 1; Source is Memory Buffer BLT (see above)

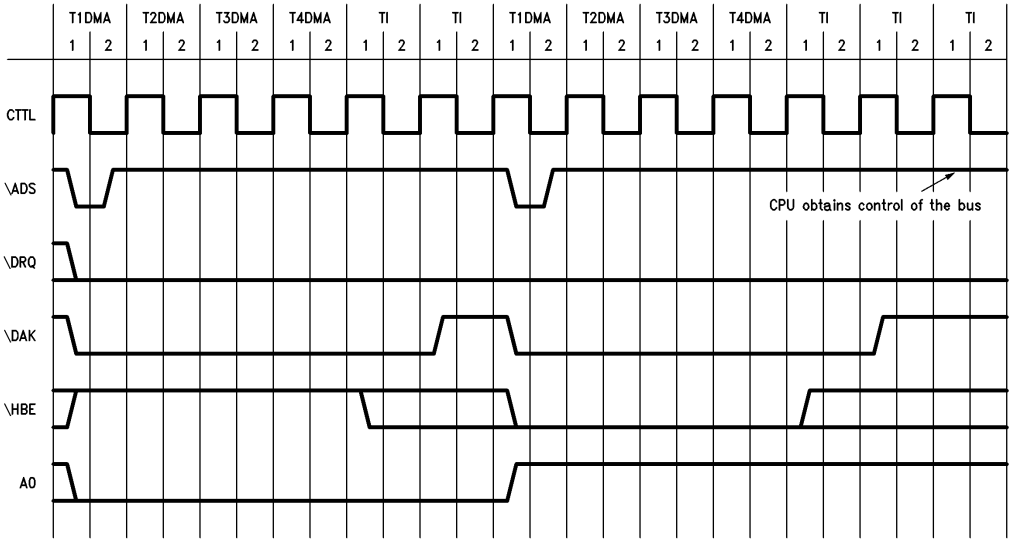

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Diagram 6

Example 7

Example 7 presents the case in which the DMAC is programmed to transfer data without releasing the bus. In this case, the DMAC does not relinquish the bus until the corresponding $\overline{DRQ}$ pin is deasserted or block transfer is completed.

TABLE VIII. Parameters for Programming the DMAC not to Relinquish the Bus

Bus Fairness Parameters	Values	Description
BWA Field	0 0	Bus Width is 8 Bits (BYTE)
BLT Field	0 0 0 0 0	DMAC will not relinquish the bus until the corresponding DRQ is deasserted, or EOT occurs, or block transfer is complete.
MODE CONTROL REGISTER	H'200	OT = 0; Auto-Initialize Off DIR = 0; Read Cycle in Flyby BWA (see above) ADA = 1; Source is Memory Buffer BLT (see above)

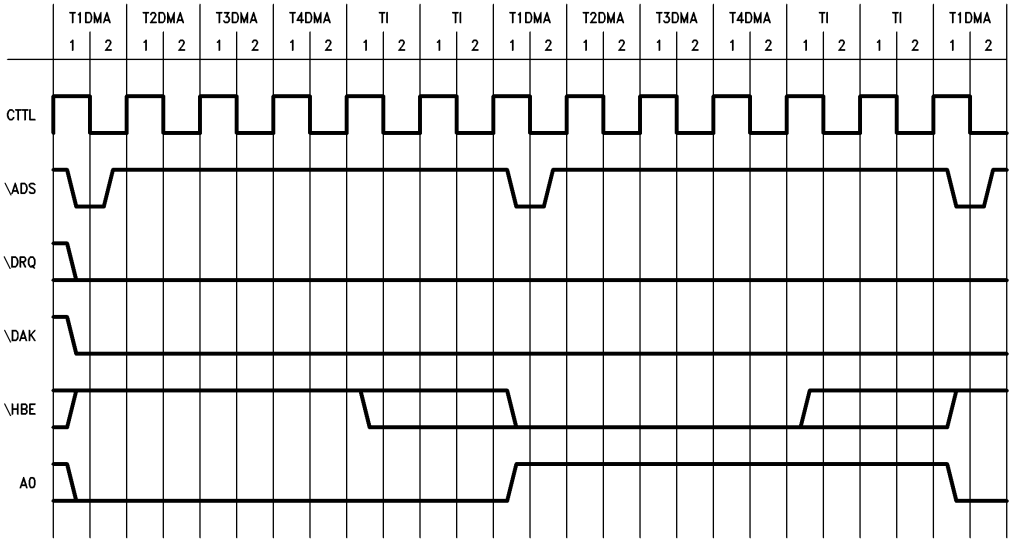

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Diagram 7

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