Configuring DRAM to NS32GX320

National Semiconductor
Application Note 719
Gerardo Nahum
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1.0 ABSTRACT

This application note describes the possible configuration of DRAM with page lower than 8k byte at an NS32GX320 based system. Some examples with different bus widths are given at the appendix together with the implementation of a PAGE signal extended for pages from 0.5k to 8k.

2.0 INTRODUCTION

The NS32GX320 features the page signal optimizing the access to a DRAM memory. The page signal will be activated if the last transaction with PLAT active was to the same 8k bytes (A13:A31 are compared). Thus, row address latch can be avoided by the DRAM controller, giving a faster access to the DRAM. The PLAT signal has to be activated when accessing the DRAM. Then prefetch from PROM or accessing other devices will not affect the address comparison.

When using a DRAM configuration with page smaller than 8k byte an upgrade must be done to make sure the accesses are to the same page. More address bits must be compared.

In the sections that follow, we will describe some possible configurations of DRAM and for each one a circuit to upgrade the PAGE signal of the NS32GX320.

This application considers DRAMs with different page size, memory bus width and usage of standard SIMMs existing in the market.

3.0 DESCRIPTION

The common DRAMs used in standard designs are 256k x 4-bit, 1M x 1-bit, 1M x 4-bit, 4M x 1-bit, 4M x 4-bit and 16M x 1-bit. DRAM modules using the above mentioned elements can be used as well.

For each one, depending on the bus width used, we describe the DRAM configuration.

All the following configurations are valid for DRAM with fast page mode as well as for static column mode and nibble mode. The unique differences between these types is the behavior of the CAS signal in burst cycles.

3.1 256k x 4 DRAM

The 256k x 4 DRAM page size is 0.5k words. The address mux of a system with 8-bit bus selects A0:A8 as column address and A9:A17 as row address. If we want to optimize the DRAM access using the page feature of the NS32GX320 we must generate a signal indicating that the current access is to the same 0.5k byte page than the last DRAM access. Thus, additionally to the PAGE signal, we must compare the lines A9, A10, A11 and A12 of the access to their value on the last access. The lines A13 until A31 are compared by the NS32GX320.

At 16-bit bus the column address is given by A1 until A9 and the row address is given by A10 until A18. In this case we need to generate page signal to the lines A10, A11 and A12.

At 32-bit bus, the column address is given by A2:A10 and the row address by A11:A19. We need to build hardware for the lines A11 and A12

The hardware will be described in the section 4.0

3.2 DRAM 1M x 1, 1M x 4

The 1Mx1/x4 dram has a 1k word page. A system with 8-bit bus will need hardware implementing the page signal for the lines A10, A11 and A12. (The row address is given by A10 to A19.)

A system with 16-bit bus will need hardware implementing the page signal to A11 and A12. (The row address is A11 to A20.)

A system with 32-bit bus will need extra hardware because the row address is given by A12:A21, then page signal must be implemented to the signal A12 only. A13 to A31 are given by the NS32GX320 page mechanism.

3.3 DRAM 4M x 1, 4M x 4

The 4M words DRAM have a 2k words page. A system with 8-bit bus will have a column address given by A0:A10 and a row address given by A11:A21. Thus the page signal must be generated to the lines A11 and A12, additionally to the NS32GX320 page signal. A system with 16-bit bus will need a page signal for the line A12 only (the row address is given by A12:A22).

A system with 32-bit bus won't need any upgrade to the NS32GX320 page mechanism.

3.4 DRAM 16M x 1

The 16M bit DRAM have a page of 4k words. Only an 8-bit bus system will need an upgrade to the PAGE signal being the row address A12:A23. Thus only the line A12 must be included in the extra page mechanism.

Systems with 16-bit or 32-bit bus won't need any upgrade, the NS32GX320 PAGE signal must be used alone at the DRAM controller.

4.0 IMPLEMENTATION

The following section describes the circuit needed to upgrade the page mechanism of the NS32GX320. The implementation is a superset of the above described cases. A new signal is generated complementing the PAGE signal of the NS32GX320. This signal (called SPAGE in this application note) is active low and will be asserted when the current access is to the same $1/16$ page of the last access with PLAT active (each page 8k bytes).

The size of the new page depends on which addresses are connected. The following table summarizes the options. The unconnected pins must be pulled up.

Page size	Address signals to be connected
0.5k	A9, A10, A11, A12
1k	A10, A11, A12,
2k	A11, A12
4k	A12
8k and up	None

The hardware consists in a PAL® 16R4, the grade depends on the system frequency (see Table II), that samples at the rising edge of BCLK the addresses A12, A11, A10 and A9 if PLAT is active and CONF,RDY and BMT indicates end of last T2.

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 TL/EE11063 RRD-B30M75/Printed in U. S. A.

The NS32GX320's PLAT must be sampled by a 74F74 using $\overline{BCLK}$ to extend it until the end of last T2, if the system supply PLAT valid until the end of last T2, this sampling level can be avoided and PLAT can be used as input directly.

The SPAGE signal is generated by comparing the sampled address lines to the current ones. If they are equal and the NS32GX320's PAGE is active the SPAGE is asserted (low).

The comparison and the mask are done at the PAL. The PAL generates two SPAGE signals (SPAGEL corresponding to A9 and A10 and SPAGEH corresponding to A11 and A12). They are both active low and not masked by PAGE. The PAL generates a third line, SPAGE, that is active if all the SPAGEh, SPAGEL and PAGE signal are active.

The user can use SPAGE signal alone or if timing is more critical than number of input pins, the above mentioned 3 signals can be used and the AND function can be implemented directly at the DRAM controller.

Commonly the DRAM controller will sample the SPAGE signal, if the timing is critical (e.g., the DRAM controller is implemented in to an ASIC), then the two AND functions can be implemented at the sampling level. This will eliminate the second asynchronous pass at the PAL. (See Timing considerations section.)

4.1 Timing Considerations

The signal SPAGE is generated asynchronously from the Address bits.

TSPAGEv = max (TAv + 2 * Tpal delay, TPAGEv + Tpal delay)

TSPAGEv = max (9 + 2 * 10, 18 + 10) = max (29, 28) = 29 ns using a PAL grade D

if the AND function is implemented at the DRAM controller TSPAGEv = max (TAv + Tpal delay TPAGEv)

TSPAGEv = max (9 + 10, 18) = 19 ns

5.0 TABLES

TABLE I. Page Upgrade

Memory	PAGE Size	Bus Width	Address Signals
256k x 4	512	8-Bit	A9, A10, A11, A12
		16-Bit	A10, A11, A12
		32-Bit	A11, A12
1M x 1	1024	8-Bit	A10, A11, A12
		16-Bit	A11, A12
		32-Bit	A12
4M x 1	2048	8-Bit	A11, A12
		16-Bit	A12
		32-Bit	None
16M x 1	4096	8-Bit	A12
		16-Bit	None
		32-Bit	None

5.1 SPAGE Timing

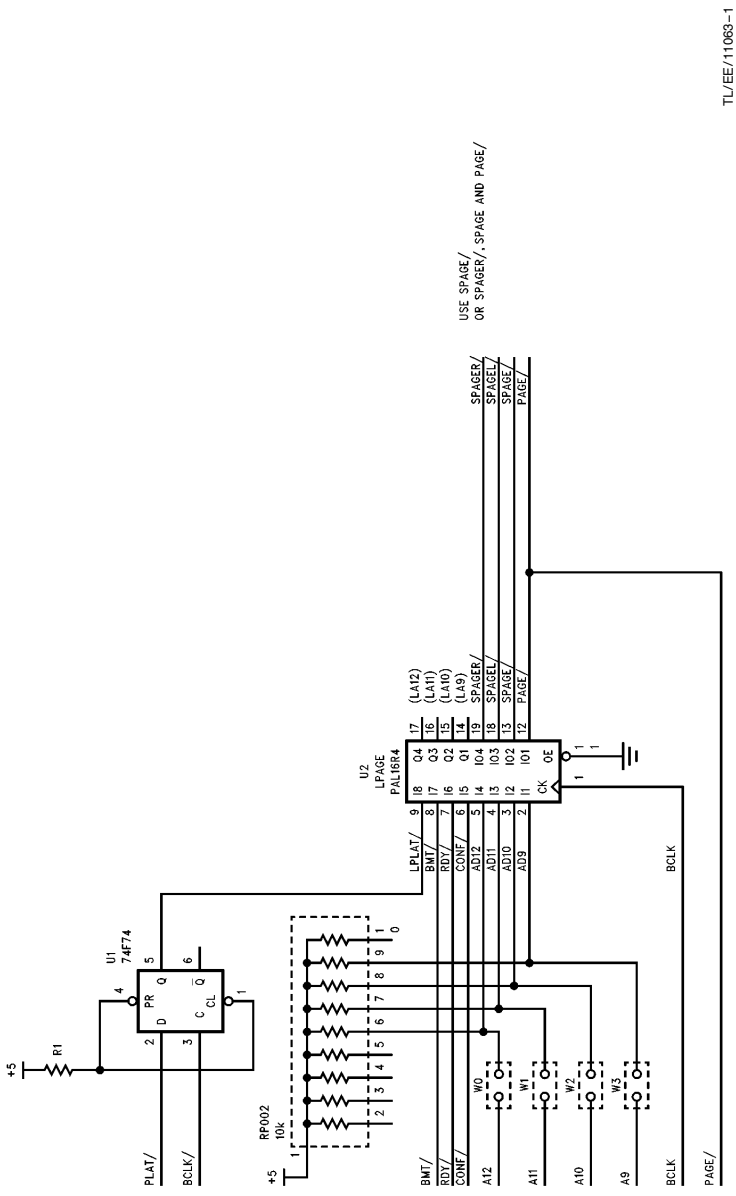
TABLE II. SPAGE Setup Time

Mask Function at the PAL outside DRAM Controller			
Number of Input Pins	**PAL GRADE**	**25 MHz**	**20 MHz**
1	GRADE C	7 ns	17 ns
1	GRADE D	11 ns	21 ns
Mask Function at DRAM Controller			
Number of Input Pins	**PAL GRADE**	**25 MHz**	**20 MHz**
3	GRADE C	19 ns	29 ns
3	GRADE D	21 ns	31 ns

6.0 PAL EQUATIONS

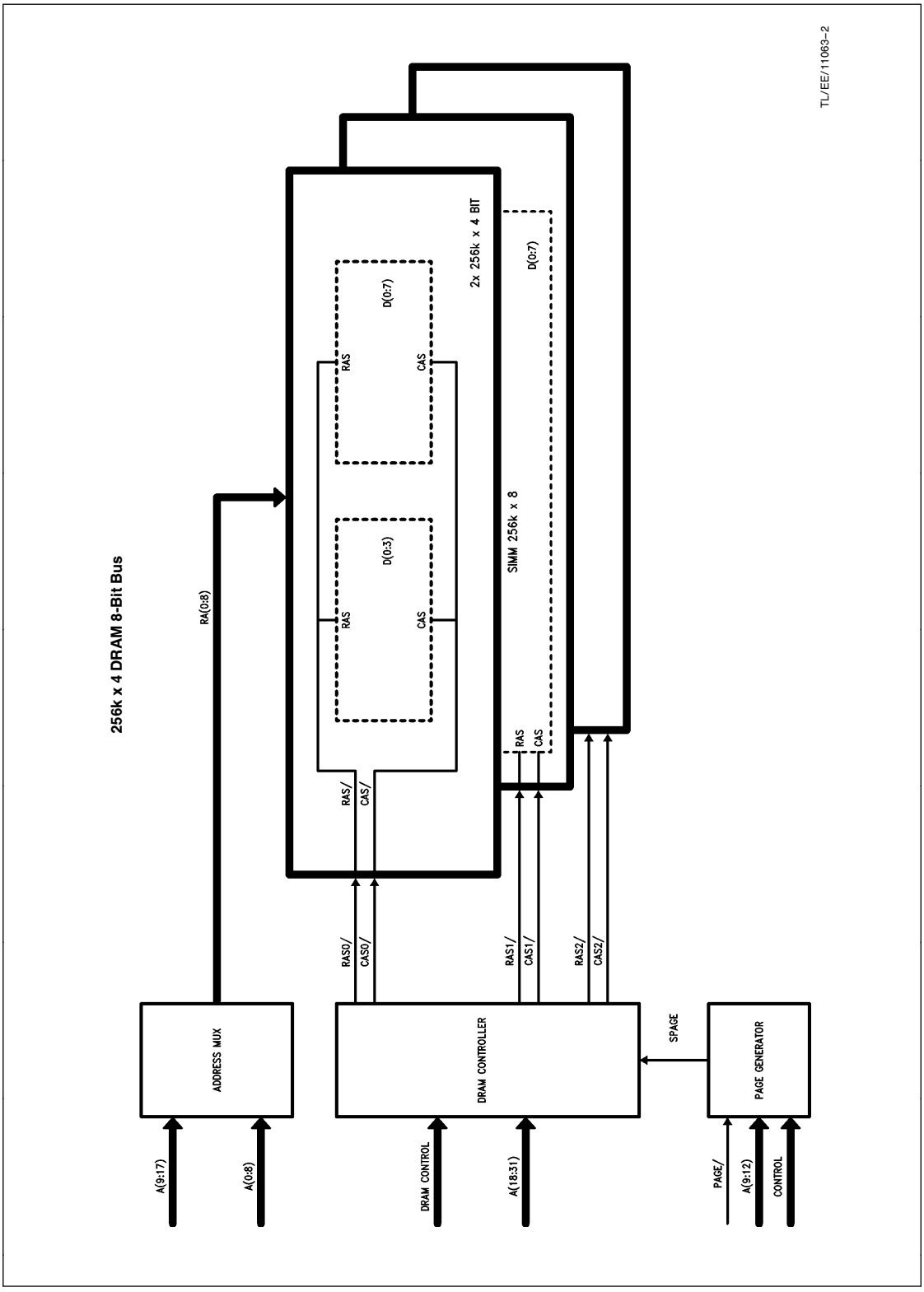
```
module lpage
flag '-r3' , '-t2' , '-s','-q2'
title 'Low Page signal generator              22-Apr-90'
" This pal generates the SPAGE signal used together with the NS32GX320 PAGE
" signal to identify in-page access to DRAM with less than 4k word page
    LPAGE device 'P16R4';
CLK   pin 1;   " r.e. of BCLK
OE    pin 11;  " Always GND
"Inputs
A9        pin 2;  " NS32GX320 address signals
A10       pin 3;  " The not needed address lines must be left constant
A11       pin 4;  " high (pulled up)
A12       pin 5;
CONF      pin 6;  " Control signals to identify last T2
RDY       pin 7;
BMT       pin 8;
PLAT      pin 9;  " Plat if continued until last T2 or sampled Plat.
PAGE      pin 12; " Page signal from NS32GX320
" Outputs
SPAGEL    pin 19; " Low Page signal to DRAM controller
SPAGEH    pin 18; " High page signal to DRAM controller
SPAGE     pin 13; " New PAGE signal
" Internal registers
LA9       pin 14; " Sampled address of last DRAM access
LA10      pin 15;
LA11      pin 16;
LA12      pin 17;
" Definitions
    x,c,z = .X.,.C.,.Z.;
    LA = [LA12, LA11, LA10, LA9];
    A  = [A12, A11, A10, A9];
Equations
" Sample address at last T2 with PLAT active
!LA := !A & !PLAT & !CONF & !RDY & BMT     " if LAST T2 with PLAT sample new A
      # !LA & !(  !PLAT & !CONF & !RDY & BMT); " else hold sampled address
" SPAGEx : assert when LA==A
!SPAGEL = (LA9==A9) & (LA10==A10);
!SPAGEH = (LA11==A11) & (LA12==A12);
" SPAGE active if both SPAGEH and SPAGEL active and PAGE active
!SPAGE = !SPAGEL & !SPAGEH & !PAGE;
" Note: The SPAGEx signal is split because of the number of minterms of
"       this pal. In an ASIC design they can be unified in one single
        equation.
END lpage
```

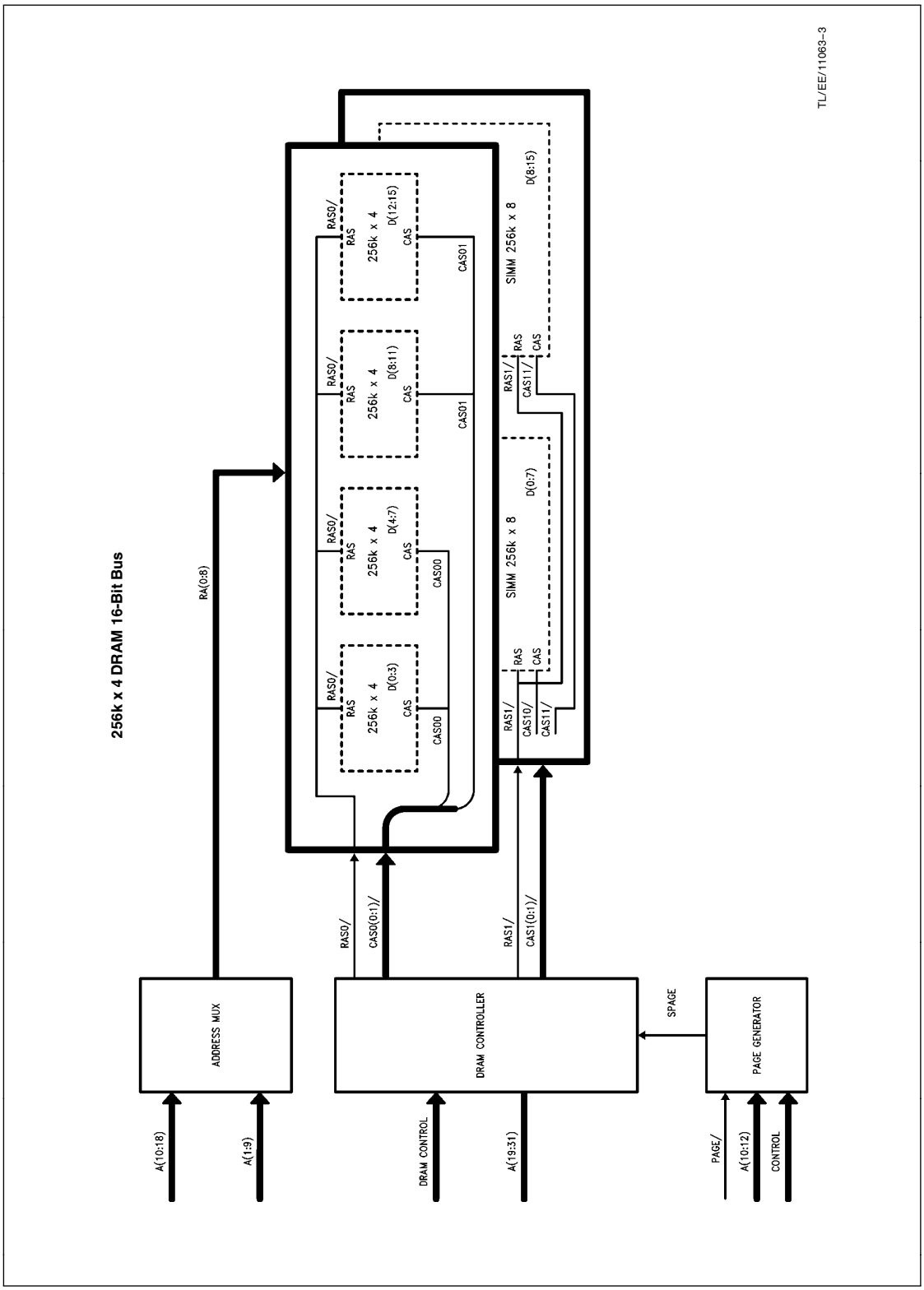
7.0 APPENDIX 1

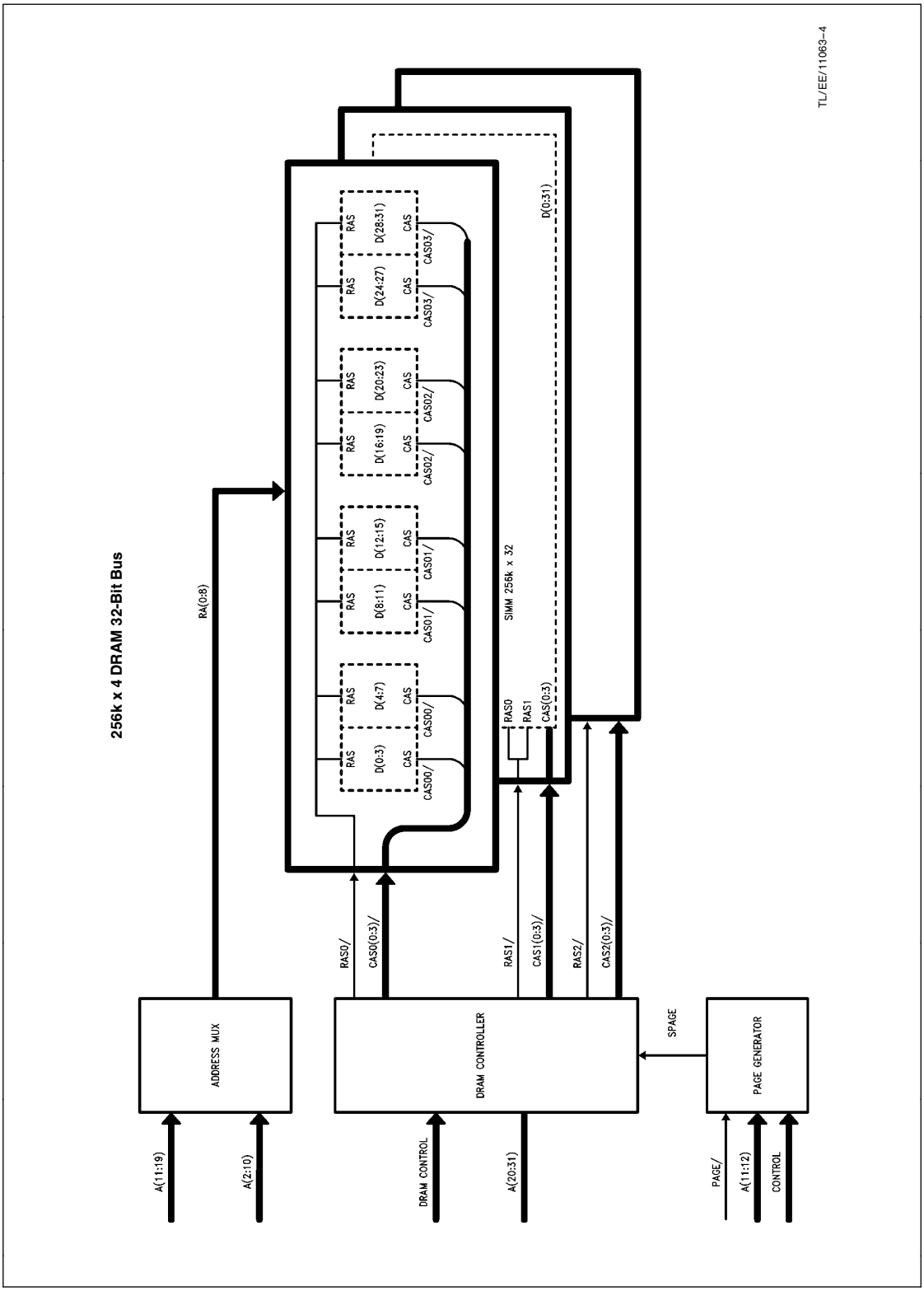


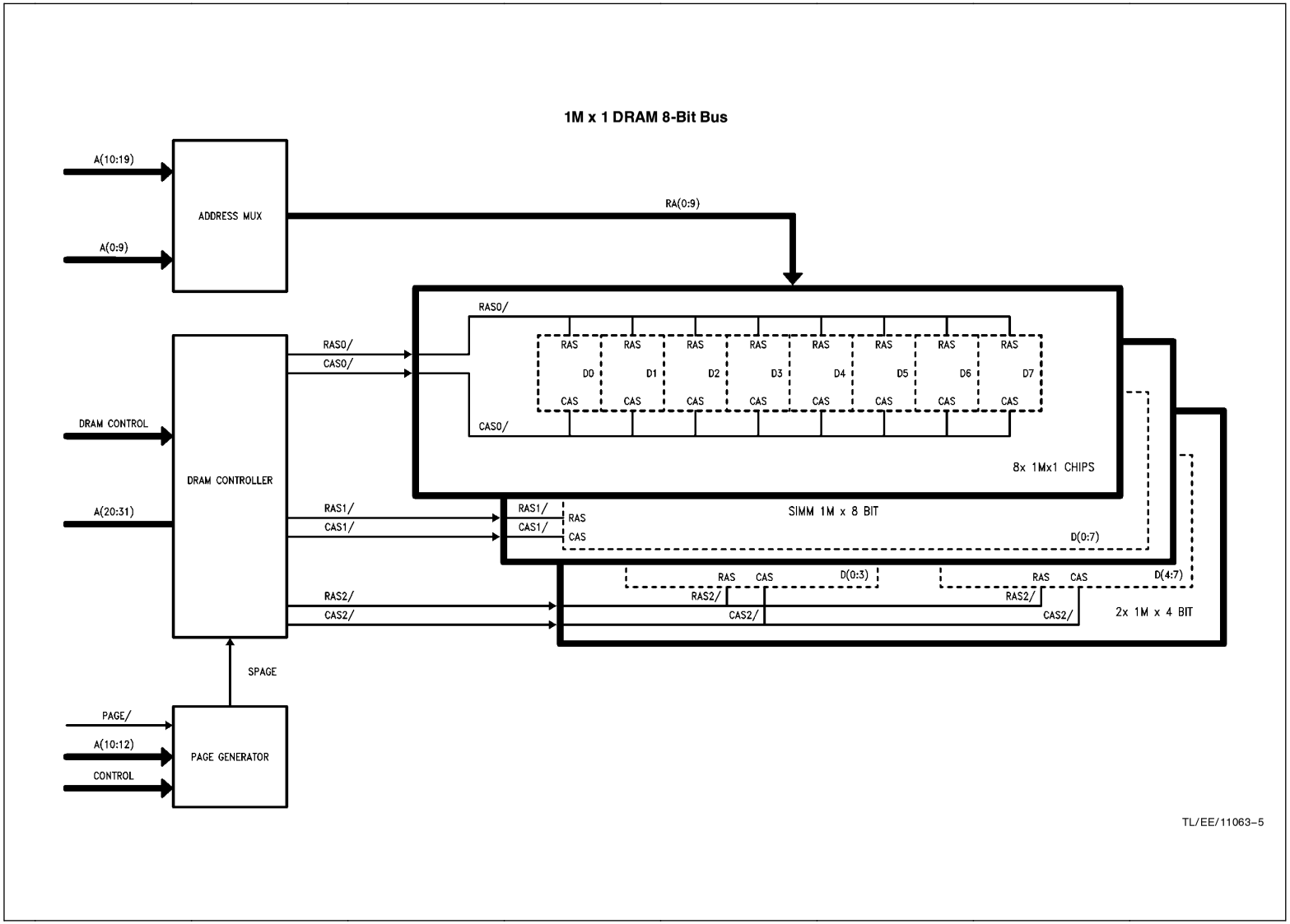
TL/EE/11063–1

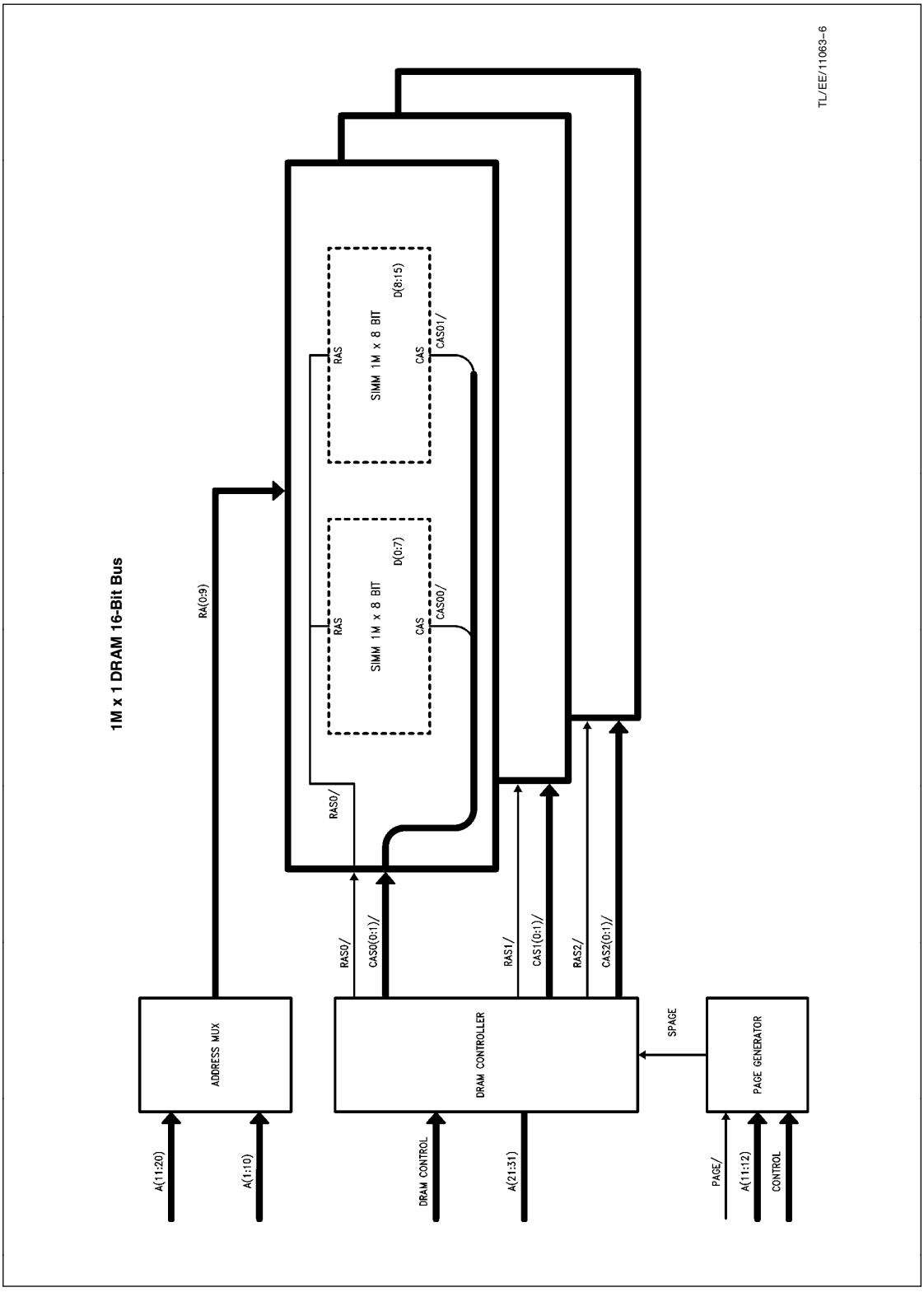
Page Size	Jumper W0	W1	W2	W3
0.5k	IN	IN	IN	IN
1k	IN	IN	IN	OUT
2k	IN	IN	OUT	OUT
4k	IN	OUT	OUT	OUT
8k	OUT	OUT	OUT	OUT

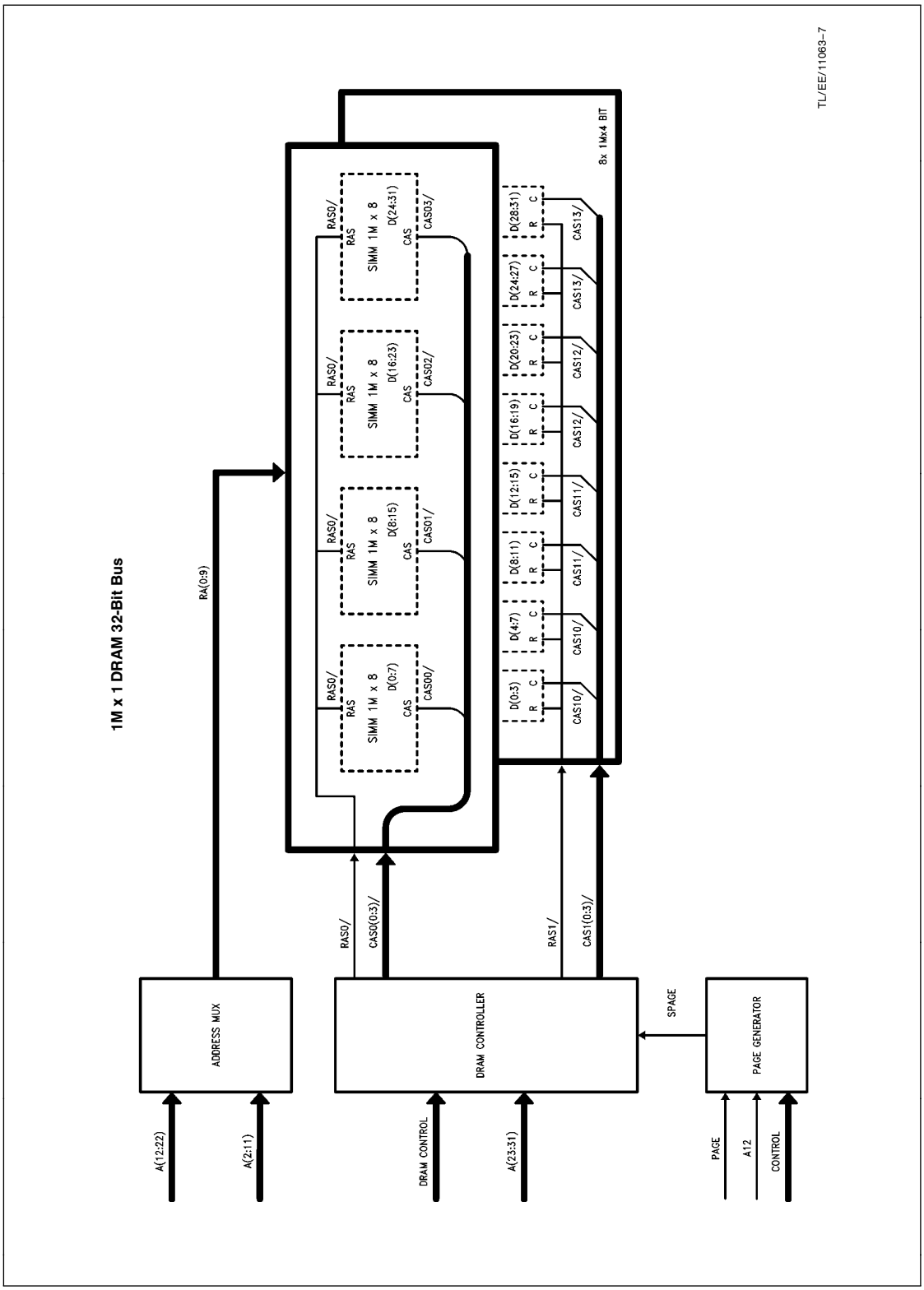

256k x 4 DRAM 8-Bit Bus
TL/EE/11063–2
RA(0:8)
2x 256k x 4 BIT
SIMM 256k x 8
D(0:7)
D(0:3)
D(0:7)
RAS
CAS
RAS
CAS
RAS
CAS
RAS/
CAS/
RAS0/
CAS0/
RAS1/
CAS1/
RAS2/
CAS2/
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
A(9:17)
A(0:8)
DRAM CONTROL
A(18:31)
PAGE/
A(9:12)
CONTROL

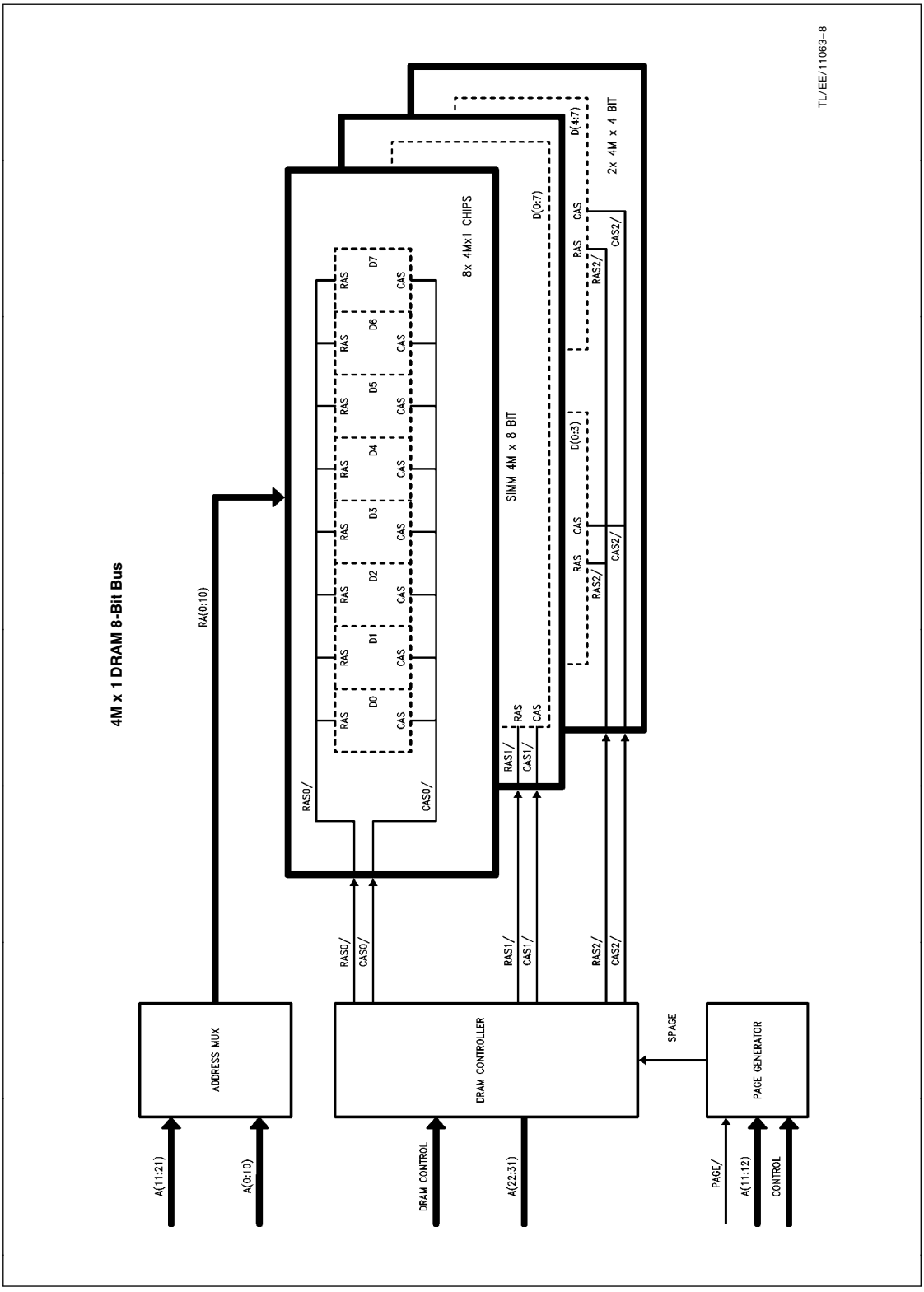

256k x 4 DRAM 16-Bit Bus
TL/EE/11063–3
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
RA(0:8)
RAS0/
CAS0(0:1)/
RAS1/
CAS1(0:1)/
SPAGE
A(10:18)
A(1:9)
DRAM CONTROL
A(19:31)
PAGE/
A(10:12)
CONTROL
SIMM 256k x 8
D(0:7)
D(8:15)
256k x 4
D(0:3)
D(4:7)
D(8:11)
D(12:15)
RAS
CAS
CAS00
CAS01
CAS10/
CAS11/


256k x 4 DRAM 32-Bit Bus
TL/EE/11063–4
SIMM 256k x 32
RA(0:8)
D(0:31)
RAS0
RAS1
CAS(0:3)
RAS
CAS
D(0:3)
D(4:7)
D(8:11)
D(12:15)
D(16:19)
D(20:23)
D(24:27)
D(28:31)
CAS00/
CAS01/
CAS02/
CAS03/
RAS0/
CAS0(0:3)/
RAS1/
CAS1(0:3)/
RAS2/
CAS2(0:3)/
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
A(11:19)
A(2:10)
DRAM CONTROL
A(20:31)
PAGE/
A(11:12)
CONTROL


1M x 1 DRAM 8-Bit Bus
A(10:19)
A(0:9)
ADDRESS MUX
RA(0:9)
RAS0/
CAS0/
DRAM CONTROL
DRAM CONTROLLER
A(20:31)
RAS1/
CAS1/
RAS2/
CAS2/
SPAGE
PAGE/
A(10:12)
CONTROL
PAGE GENERATOR
RAS
CAS
D0
D1
D2
D3
D4
D5
D6
D7
8x 1Mx1 CHIPS
SIMM 1M x 8 BIT
D(0:7)
D(0:3)
D(4:7)
2x 1M x 4 BIT
TL/EE/11063–5


1M x 1 DRAM 16-Bit Bus
TL/EE/11063–6
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
RA(0:9)
SIMM 1M x 8 BIT
D(0:7)
D(8:15)
RAS
CAS
CAS00/
CAS01/
RAS0/
CAS0(0:1)/
RAS1/
CAS1(0:1)/
RAS2/
CAS2(0:1)/
A(11:20)
A(1:10)
DRAM CONTROL
A(21:31)
PAGE/
A(11:12)
CONTROL


1M x 1 DRAM 32-Bit Bus
TL/EE/11063–7
8x 1Mx4 BIT
RA(0:9)
RAS0/
CAS0(0:3)/
RAS1/
CAS1(0:3)/
SPAGE
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
A(12:22)
A(2:11)
DRAM CONTROL
A(23:31)
PAGE
A12
CONTROL
SIMM 1M x 8
D(0:7)
CAS00/
D(8:15)
CAS01/
D(16:23)
CAS02/
D(24:31)
CAS03/
D(0:3)
D(4:7)
D(8:11)
D(12:15)
D(16:19)
D(20:23)
D(24:27)
D(28:31)
CAS10/
CAS11/
CAS12/
CAS13/
R
C


4M x 1 DRAM 8-Bit Bus
TL/EE/11063–8
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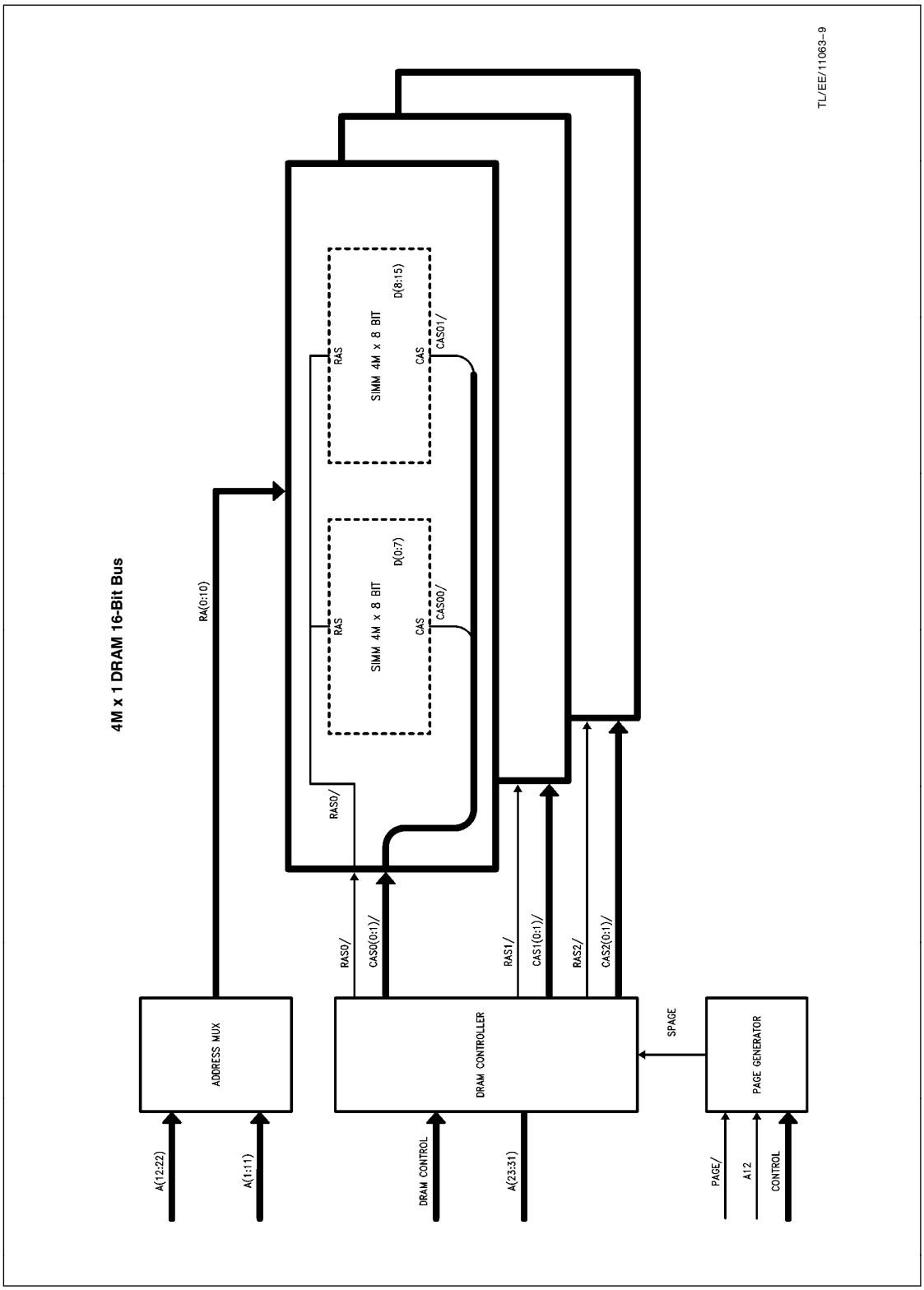
A(0:10)
ADDRESS MUX
RA(0:10)
DRAM CONTROL
A(22:31)
RAS0/
CAS0/
RAS1/
CAS1/
RAS2/
CAS2/
SPAGE
PAGE/
A(11:12)
CONTROL
PAGE GENERATOR
8x 4Mx1 CHIPS
SIMM 4M x 8 BIT
2x 4M x 4 BIT
D(0:7)
D(0:3)
D(4:7)
RAS
CAS
D0
D1
D2
D3
D4
D5
D6
D7


4M x 1 DRAM 16-Bit Bus
TL/EE/11063–9
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
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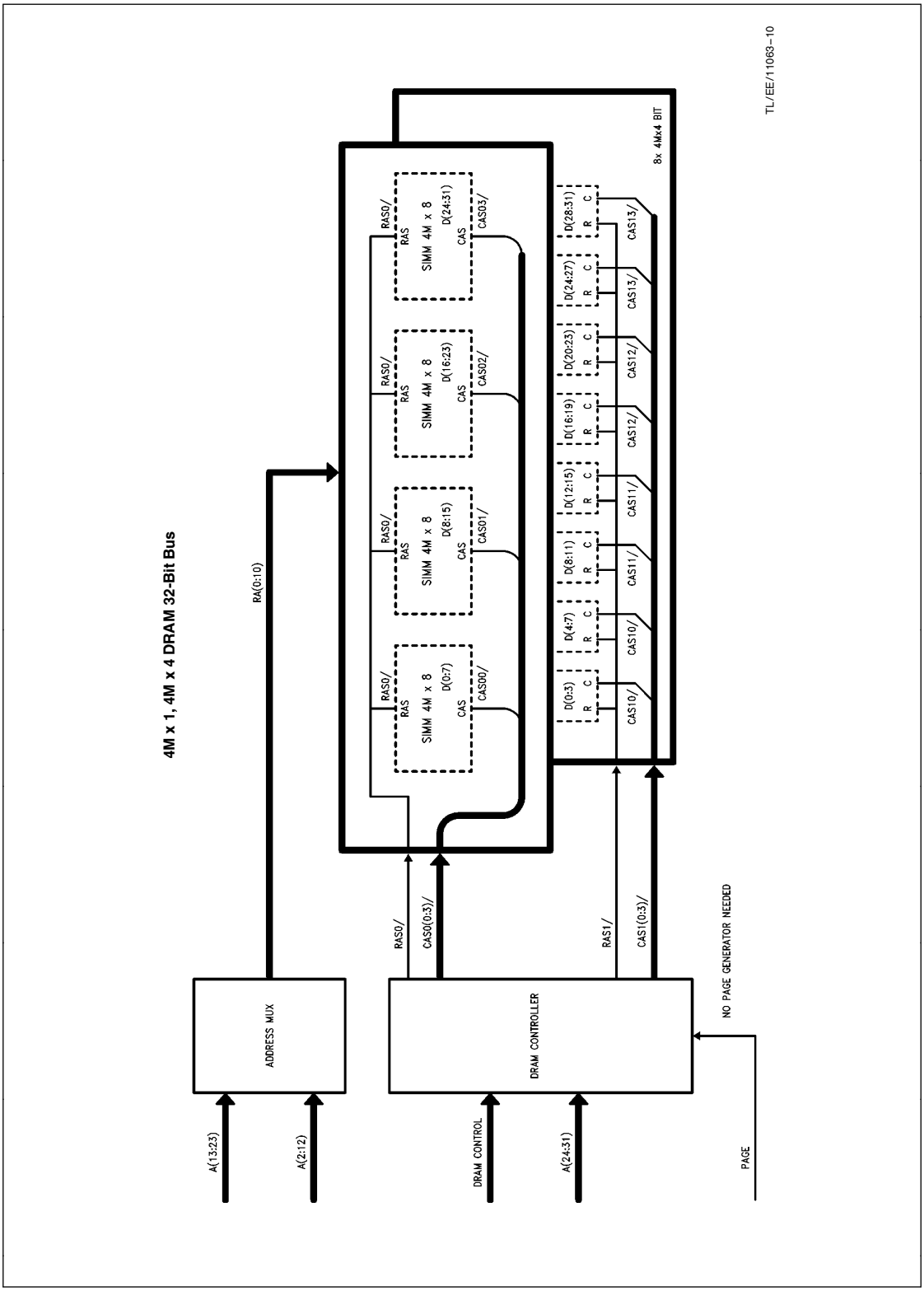
RAS0/
CAS0(0:1)/
RAS1/
CAS1(0:1)/
RAS2/
CAS2(0:1)/
SIMM 4M x 8 BIT
RAS
CAS
D(0:7)
CAS00/
SIMM 4M x 8 BIT
RAS
CAS
D(8:15)
CAS01/
A(12:22)
A(1:11)
DRAM CONTROL
A(23:31)
PAGE/
A12
CONTROL


4M x 1, 4M x 4 DRAM 32-Bit Bus
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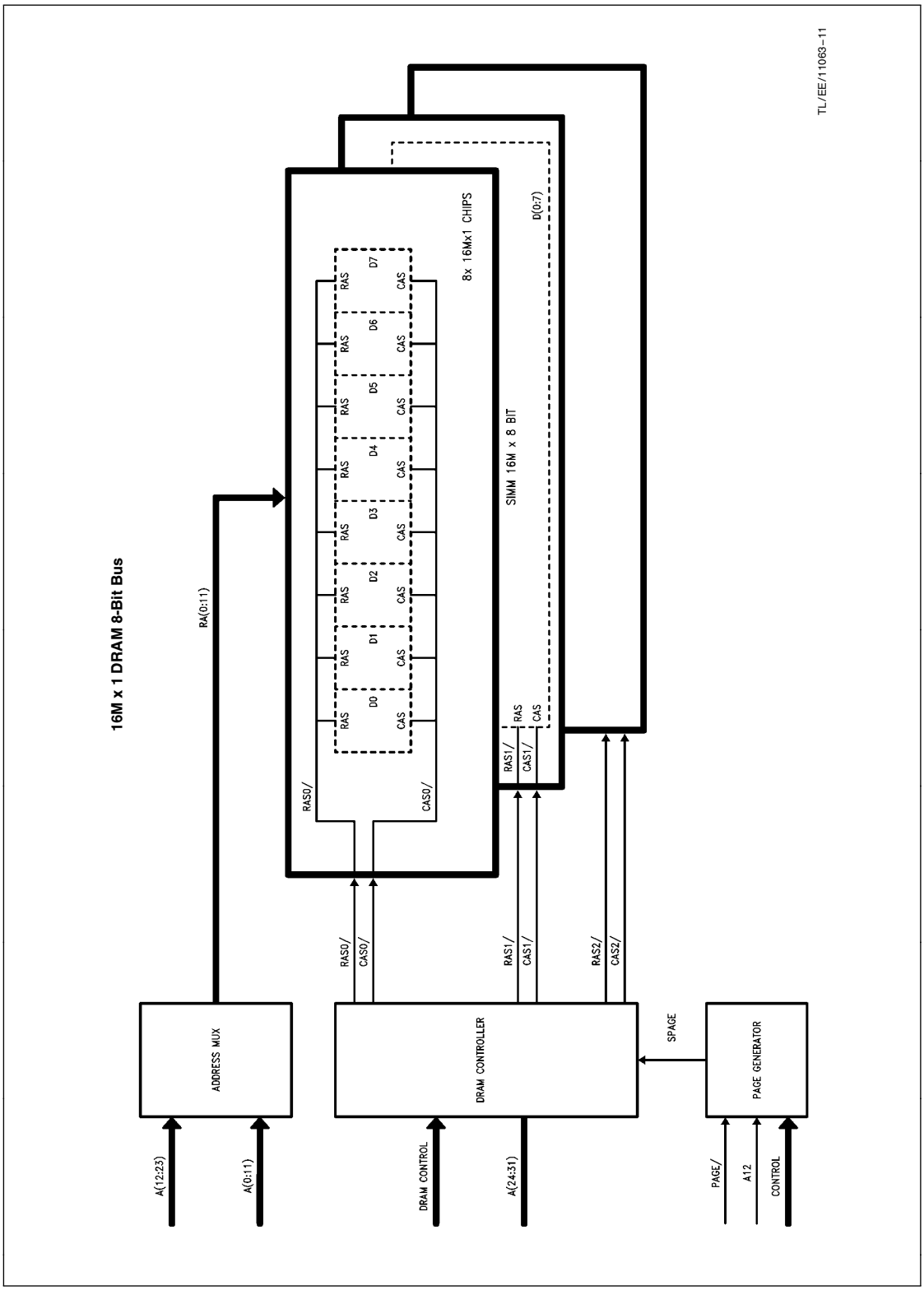
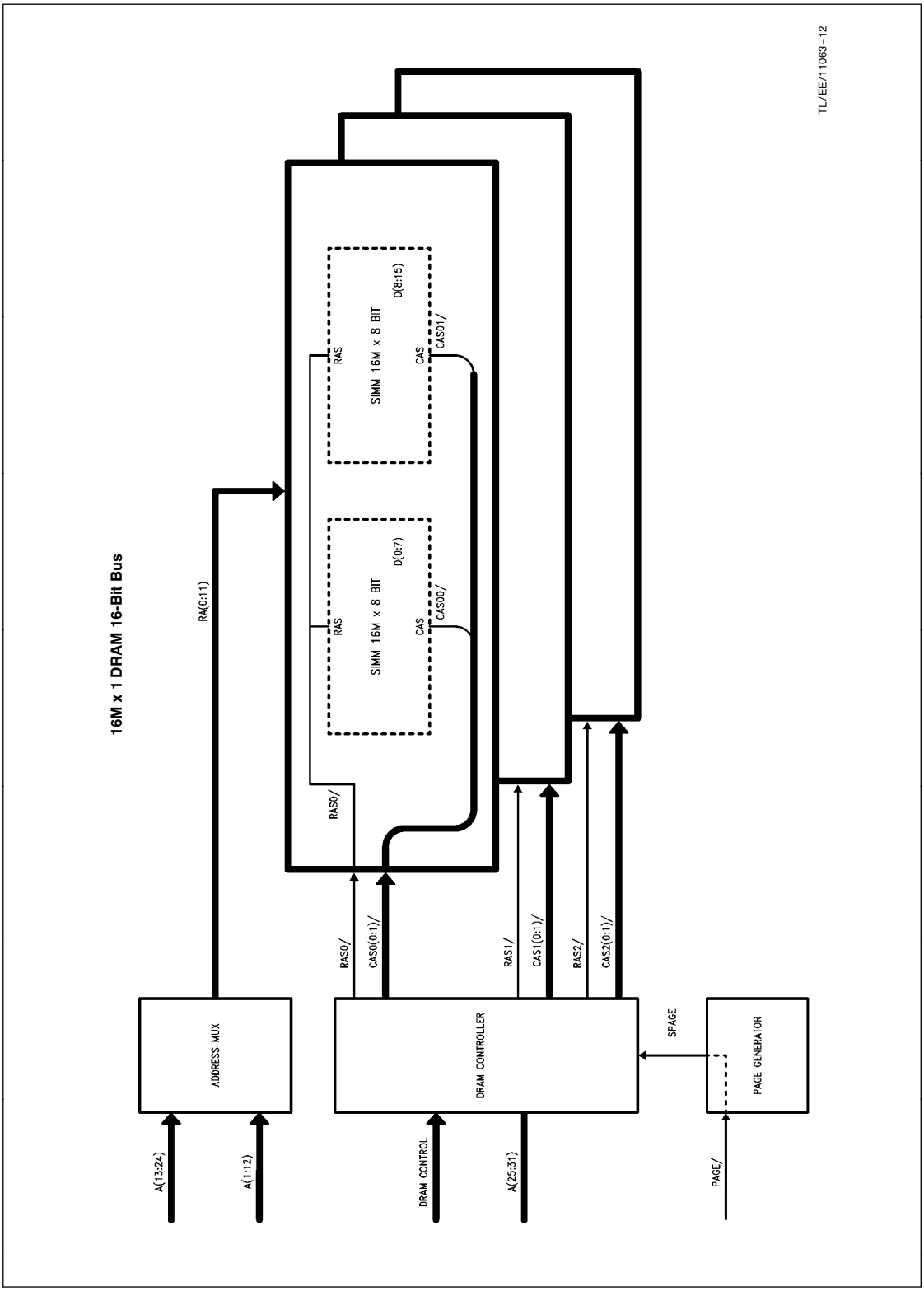
SIMM 4M x 8
D(0:7)
D(8:15)
D(16:23)
D(24:31)
RAS
CAS
RAS0/
CAS00/
CAS01/
CAS02/
CAS03/
RA(0:10)
D(0:3)
D(4:7)
D(8:11)
D(12:15)
D(16:19)
D(20:23)
D(24:27)
D(28:31)
R C
CAS10/
CAS11/
CAS12/
CAS13/
ADDRESS MUX
DRAM CONTROLLER
RAS0/
CAS0(0:3)/
RAS1/
CAS1(0:3)/
NO PAGE GENERATOR NEEDED
A(13:23)
A(2:12)
DRAM CONTROL
A(24:31)
PAGE


16M x 1 DRAM 8-Bit Bus
TL/EE/11063–11
RA(0:11)
8x 16Mx1 CHIPS
SIMM 16M x 8 BIT
D(0:7)
RAS
CAS
D0
D1
D2
D3
D4
D5
D6
D7
RAS0/
CAS0/
RAS1/
CAS1/
RAS2/
CAS2/
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
A(12:23)
A(0:11)
DRAM CONTROL
A(24:31)
PAGE/
A12
CONTROL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SIMM 16M x 8 BIT
D(0:7)
D(8:15)
RAS
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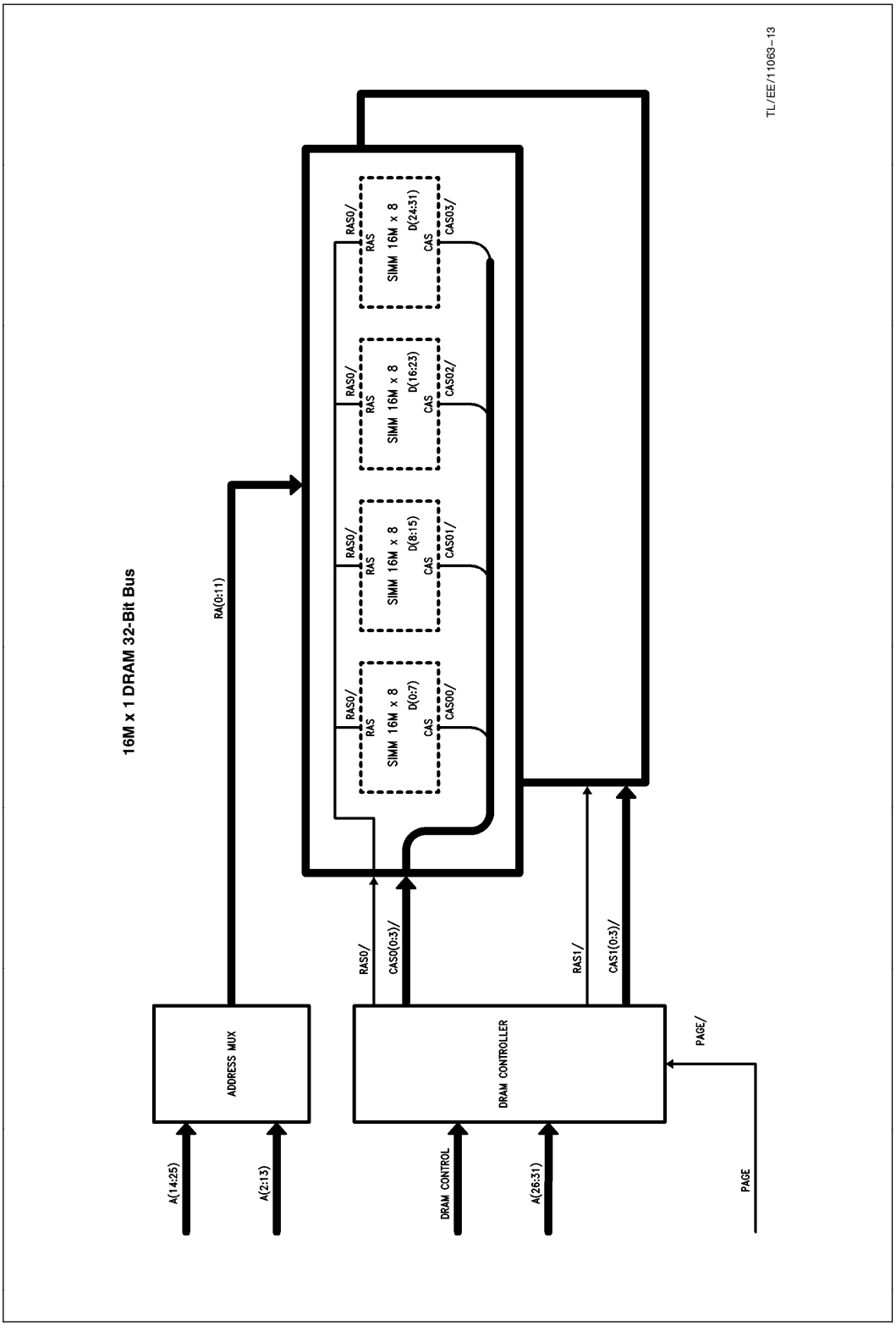
CAS00/
CAS01/
RAS0/
CAS0(0:1)/
RAS1/
CAS1(0:1)/
RAS2/
CAS2(0:1)/
ADDRESS MUX
DRAM CONTROLLER
PAGE GENERATOR
SPAGE
A(13:24)
A(1:12)
DRAM CONTROL
A(25:31)
PAGE/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A(14:25)
A(2:13)
ADDRESS MUX
RA(0:11)
DRAM CONTROL
A(26:31)
DRAM CONTROLLER
RAS0/
CAS0(0:3)/
RAS1/
CAS1(0:3)/
PAGE/
PAGE
RAS0/
RAS
SIMM 16M x 8
D(0:7)
CAS
CAS00/
RAS0/
RAS
SIMM 16M x 8
D(8:15)
CAS
CAS01/
RAS0/
RAS
SIMM 16M x 8
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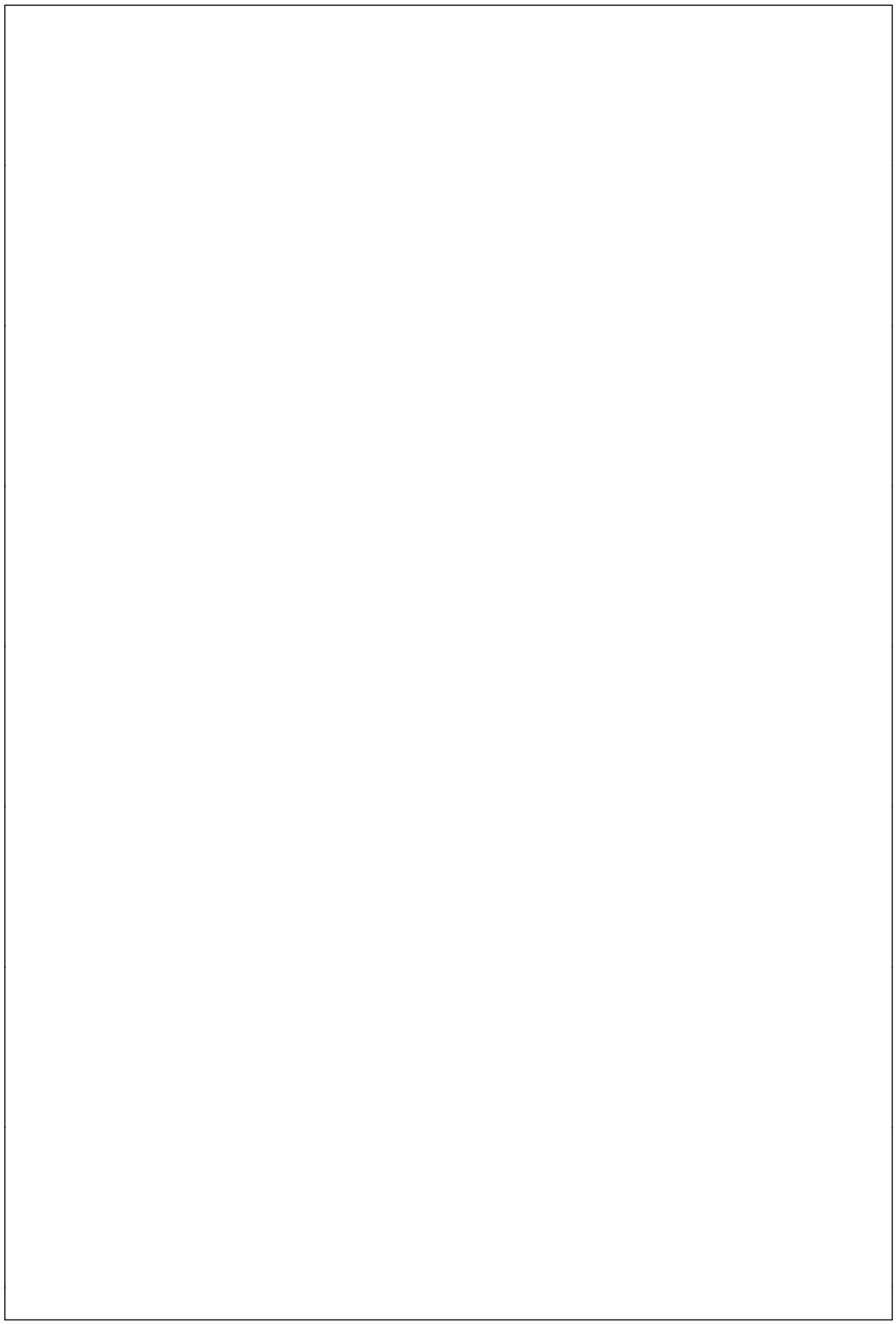
CAS
CAS02/
RAS0/
RAS
SIMM 16M x 8
D(24:31)
CAS
CAS03/



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Tel: 1(800) 272-9959
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National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

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National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
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Nottinghill, Melbourne
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Tel: (3) 558-9999
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