Performance Comparison of Direct Exception Mode vs Non-Direct Exception Mode on the NS32CG160 Processor

National Semiconductor
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1.0 INTRODUCTION

The NS32CG160 is a highly-integrated 32-bit microprocessor specifically optimized for office imaging peripherals and real-time applications.

The NS32CG160 integrates a full 32-bit CPU Core, a 2-channel DMA controller (DMAC), a 16-bit operand BitBLT Processing Unit (BPU), a 15-level Interrupt Control Unit (ICU) and three 16-bit timers, while providing a 16 Mbyte linear address space and a 16-bit external data bus.

Among its features which support office imaging peripheral and real-time applications, is a special Direct-Exception mode. This mode provides fast interrupt service and task switching.

This application note presents the performance comparison between direct and non-direct exception modes as found on the NS32CG160.

2.0 DESCRIPTION

The NS32CG160 supports two different methods for exception handling. These are known as direct exception mode, and non-direct exception mode. Non-direct exception mode can be used for applications based on modular software. Direct exception mode is preferred for applications which require fast interrupt response and task switching.

The desired exception mode is selected by the value of the Direct Exception (DE) bit in the Configuration Register (CFG). Non-Direct exception mode is enabled by resetting the DE bit (DE = 0). Direct exception mode is enabled by setting the DE bit (DE = 1). It can only be accessed in supervisor mode.

3.0 NON-DIRECT EXCEPTION MODE

The Non-Direct Exception mode is enabled while the DE bit in the CFG register is 0. In this case the CPU first pushes the saved Program Status Register (PSR) contents along with the contents of the MOD and PC registers onto the Interrupt stack. Then it reads the double-word entry from the Interrupt Dispatch table at address "INTBASE + vector * 4". The CPU uses this entry to call the exception service procedure, interpreting the entry as an external procedure descriptor. A new value number is loaded into the MOD register from the least-significant word of the descriptor, and the Static-Base pointer for the new module is read from the memory and loaded into the SB register. Then the program-base pointer for the new module is read from memory and added to the most-significant word of the module descriptor, which is interpreted as an unsigned value. Finally, the result is loaded into the PC register.

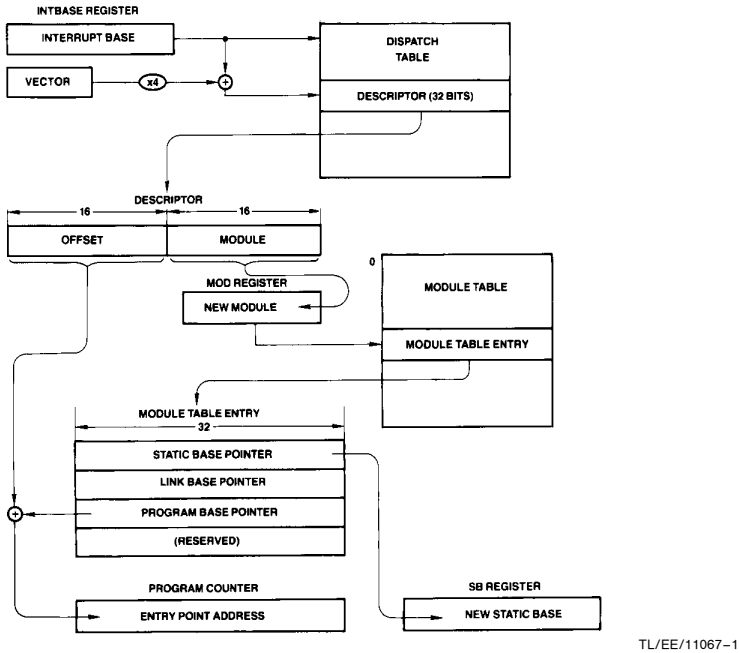

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FIGURE 1. Non-Direct Exception Mode Exception Handling

4.0 DIRECT EXCEPTION MODE

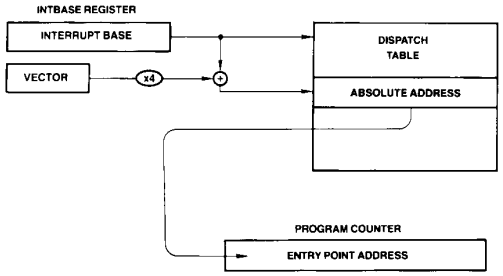

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FIGURE 2. Direct-Exception Mode Exception Handling

The Direct exception mode is enabled when the DE bit in the CFG register is set to 1. In this case the CPU first pushes the saved PSR contents along with the contents of the PC register onto the Interrupt stack. The 16-bit word stored on the interrupt stack between the saved PSR and PC registers is reserved for future use; its contents is undefined. The CPU then read the double-word entry from the Interrupt Dispatch table address ''INTBASE + vector * 4''. The CPU uses this entry to call the exception service procedure, interpreting the entry as an absolute address that is simply loaded into the PC register. The MOD and SB register are not initialized before the CPU transfers control to the service procedure. Consequently, the service procedure is restricted from executing any instruction, such as CXP, that uses the contents of the MOD or SB registers in effective address calculation.

5.0 Performance Comparison

Following is a performance comparison between the Direct and Non-Direct exception modes.

Direct exception mode enables the CPU to respond more quickly to interrupts and other exceptions because fewer memory references are required to process an exception. Direct-Exception Mode also enables faster execution of Return from Interrupt (RETI) and Return from Trap (RETT) instructions. This is because the contents of the MOD and SB are not restored.

A list of the memory references during exception processing as performed by each mode is shown in Table I.

TABLE I. Memory References

Direct-Exception Disabled DE Bit = 0	Direct-Exception Enabled DE Bit = 1
1. Write PSR Copy 2. Write MOD 3. Write High-Word PC 4. Write Low-Word PC 5. Read Low-Word from Dispatch Table 6. Read High-Word from Dispatch Table 7. Read Low-Word SB 8. Read High-Word SB 9. Read Low-Word Program Base 10. Read High-Word Program Base	1. Write PSR Copy 2. Write High-Word PC 3. Write Low-Word PC 4. Read Low-Word from Dispatch Table 5. Read High-Word from Dispatch Table

Table II compares the two modes in terms of Return from Interrupt (RETI) and interrupt latency. The RETI latency is defined as the time in cycles from the End of Interrupt cycle till the fetch of the user instruction. The interrupt latency is defined as the time in cycles from the Interrupt Acknowledge cycle till the fetch of the first instruction in the interrupt handler.

TABLE II. Interrupt/RETI Latency (In Cycles)

	Non-Direct	Direct
Interrupt	67	35
RETI	69	48

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