Understanding National's NM95C12 EEPROM with Programmable Switches

National Semiconductor
Application Note 735
Sean Pitonak
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INTRODUCTION

National's NM95C12 is a 1024-bit Serial EEPROM with 8 programmable switches. These outputs can provide logic and analog switch inputs and outputs on a parallel bus, allowing this device to perform functions such as polling via the serial bus, interrupts via the serial bus and converting parallel data onto the serial bus.

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the NM95C12. It consists of a 61-word x 16-bit EEPROM array, a 16-bit Initial Switch Register (ISR), a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and control logic.

Addresses 0–60 of the EEPROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions.

Address 61 is also an EEPROM location, but it is used as the ISR to provide the initial switch configuration information automatically on power-up.

Address 62 is the location of the SCR, which controls the switch logic of the output terminals. This address contains a volatile memory and therefore does not have endurance or programming time limits associated with it, allowing the outputs to be reconfigured an unlimited number of times.

Address 63 contains the SRR. This is a read-only register that reads back the logic levels present on the switch terminals. Only 8-bits of the SRR are used.

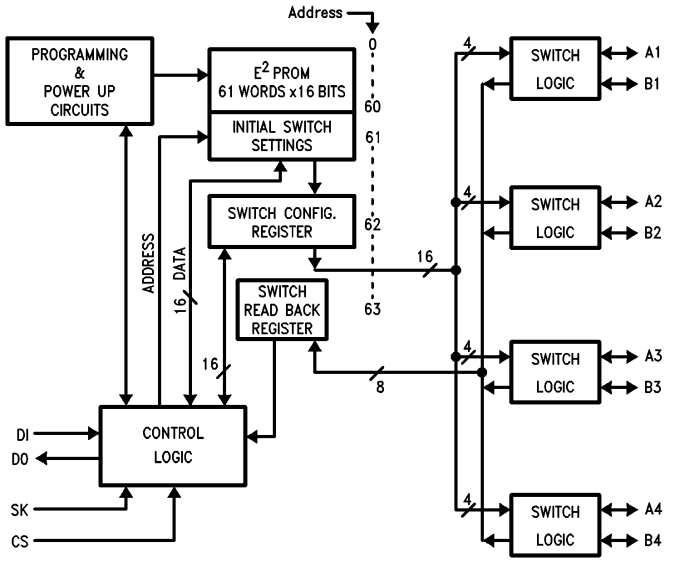
The NM95C12 also includes a Sequential Register Read function that allows the user to obtain an endless loop of data by entering the read mode and leaving the CS high.

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals.

Each switch pair can be individually configured to 1 of 14 modes. Therefore both logic and analog switches can be implemented simultaneously.

The logic switch configurations are at standard TTL levels.



TL/D/11097–1

FIGURE 1. NM95C12 Block Diagram

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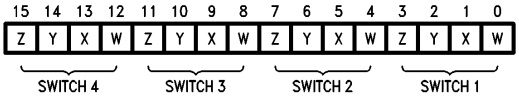
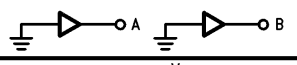
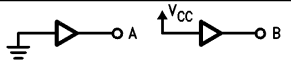
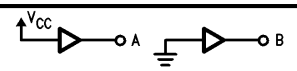
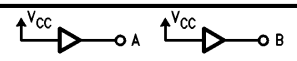
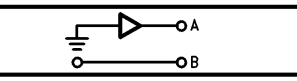
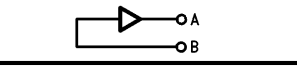
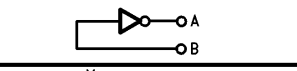
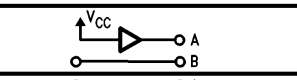
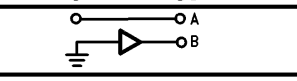
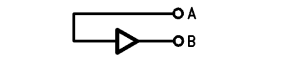
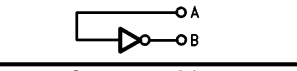
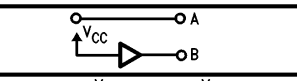
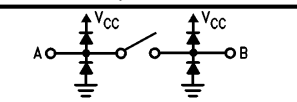
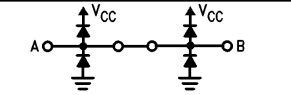


TL/D/11097–2

FIGURE 2. Switch Configuration Register (SCR)

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = Tristate
5	0	1	0	1		A = B
6	0	1	1	0		A = $\bar{B}$
7	0	1	1	1		A = 1 , B = Tristate
8	1	0	0	0		A = Tristate , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\bar{A}$
11	1	0	1	1		A = Tristate , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

TL/D/11097–3

*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

For example, in Mode 1, Terminal A would be driving V_{OL} and Terminal B would be driving V_{OH}. In Mode 5, where an input and output structure exists, Terminal A would be driving V_{IL} or V_{IH}. The switches also include a TRI-STATE® mode to represent an open terminal.

Each switch pair can also function as input/output terminals in Modes 5, 6, 9, 10 and 13. Modes 4, 7, 8, 11 and 12 represent the same input/output functions, but with the switch in the ''open'' configuration.

POWER-UP MODE

When the NM95C12 is powered-up:

1. The data previously stored in the ISR is automatically transferred to the SCR.
2. The SCR controls the switch logic, producing the switch configuration of the terminals A1 through A4 and B1 through B4.

The switch configuration is valid 1 ms after the device power supply reaches 4.5V or greater.

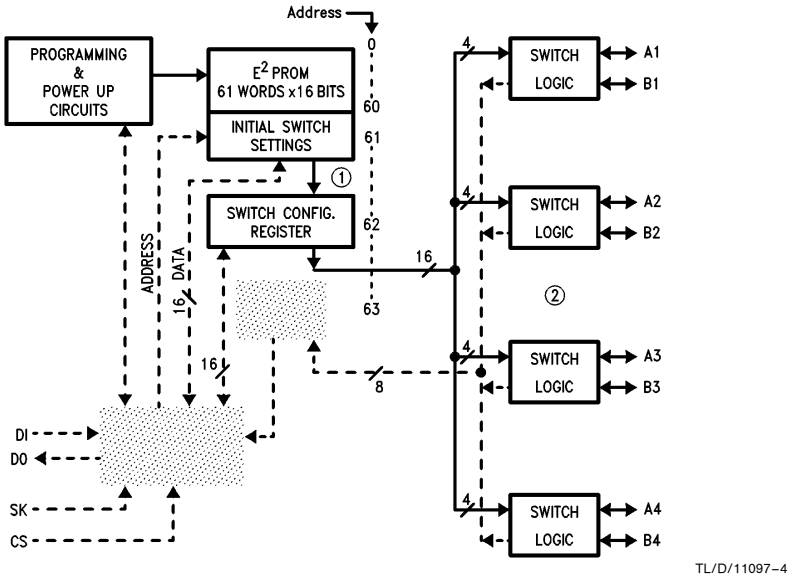


FIGURE 3. Power-Up Mode

UPDATE MODE

To update the information that is contained in the SCR and therefore on the output terminals:

1. The SCR is updated via the serial bus by writing to address 62.
2. The switch logic updates the outputs by selecting the 1 of 14 modes detailed in Table I. The configuration change becomes effective at the terminals after a brief propagation delay (t_{SWPD}), referenced to the falling edge of CS.

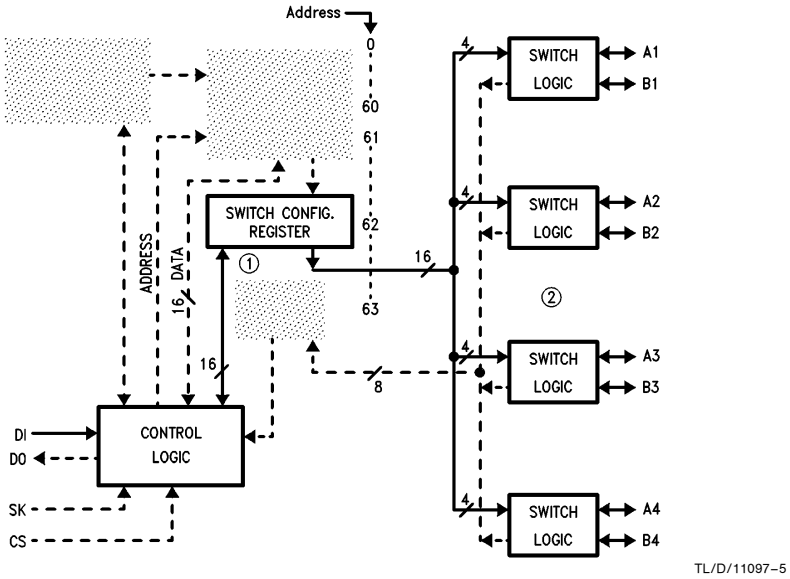


FIGURE 4. Update Mode

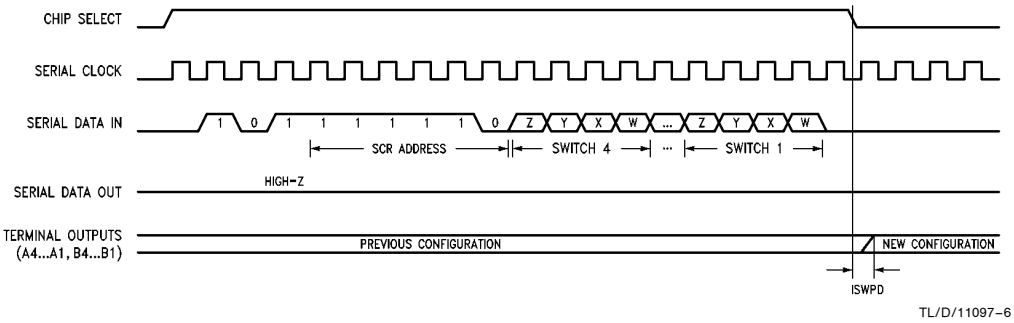


FIGURE 5. SCR Write (Update Mode) Timing Diagram

INPUT MODE

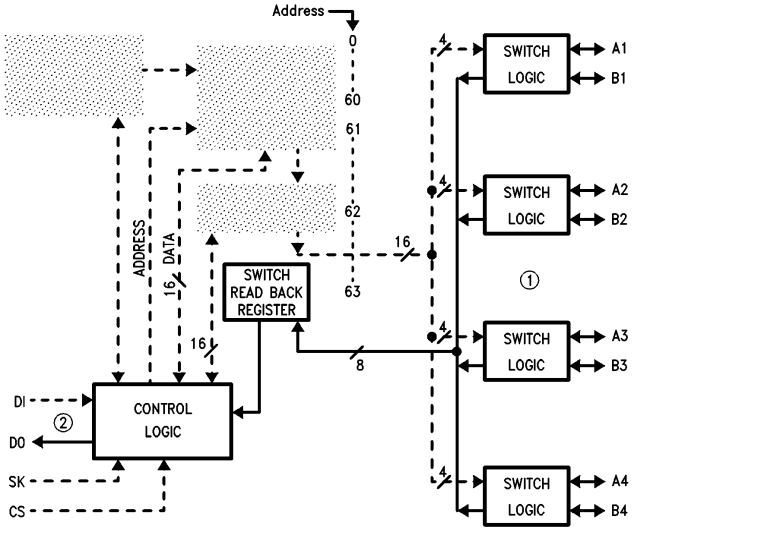
The SRR allows the current logic level present at the switch terminals to be read back on the MICROWIRE™ bus:

1. The states of the output terminals are loaded into the SRR by reading address 63.
2. The control logic allows the 8-bit parallel input to be converted to serial output on the DO pin.

The bit assignments and the conceptual function of the SRR are shown in *Figure 7*. Only bits 15 through 8 are used; Bits 7 through 0 are always read as logical 0.

The SRR Read Timing diagram is shown in *Figure 8*. Note that it is valid to terminate any read cycle early, allowing the user to avoid reading Bits 7 through 0 if that is desired. It is also valid to include leading zeros after the CS has gone high and before sending the start bit. Combining leading zeros and terminating the read cycle early may help simplify device control and speed read cycles.

Mode 12, Analog switch open, is valid for SRR input mode. For switch mode 13 (Analog switch closed), the SRR will not report the actual levels present at the terminals due to the analog levels. As a default, bits 15 through 8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the Analog switch mode.



TL/D/11097–7

FIGURE 6. Input Mode

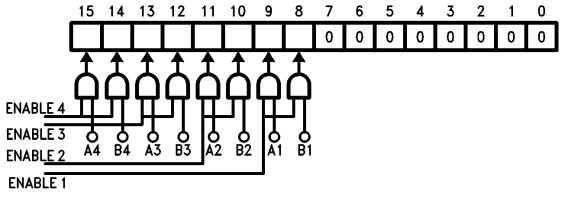


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FIGURE 7. Bit Assignments and Conceptual Function of the Switch Readback Register

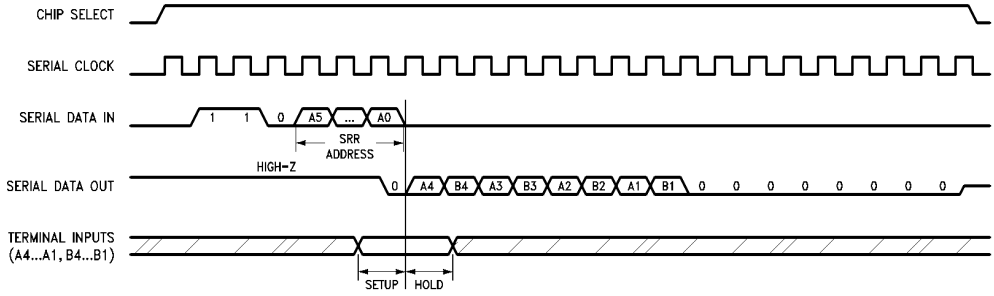

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FIGURE 8. SRR Read (Input Mode) Timing Diagram

SEQUENTIAL REGISTER READ FUNCTION

In a read mode, normally the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the DO pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. In this mode the address count will continue through the ISR, SCR and SRR and then wrap around to Address 0.

During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bit separating the data words.

WRITE CYCLE CONSIDERATIONS

After loading the WRITE instruction and the 16-bit data, the chip enters into a self-timed programming cycle when CS is forced LOW before the next rising edge of the SK clock (refer to *Figure 9*). The timer status is available on the DO pin if the CS input is forced HIGH within 1 ms of starting the programming cycle. LOW on the DO pin indicates that programming is still in progress (BUSY), while HIGH indicates that the device is READY for the next instruction.

If the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

CONCLUSION

National's NM95C12 offers users the standard functionality of a 1024-bit EEPROM and includes 8 programmable terminals that can be used to implement both logic and Analog switch functions simultaneously. These switches can be used, for example, to replace mechanical DIP and SPST switches, as well as allow interrupt polling via the serial bus.

When the device is powered-up, the switch configuration is automatically transferred to the output terminals. The terminals can be updated easily by executing a write cycle. In the input mode, the current logic level at the output terminals is read into the device and output onto the serial bus.

The NM95C12 combines unique and useable features with the simplicity of standard EEPROM functionality.

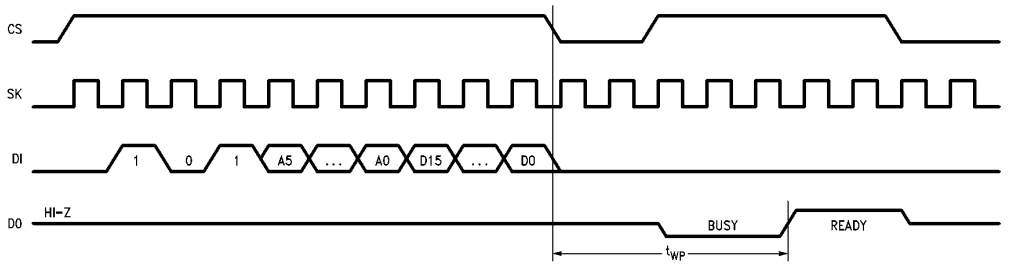

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FIGURE 9. WRITE Timing Diagram

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998