

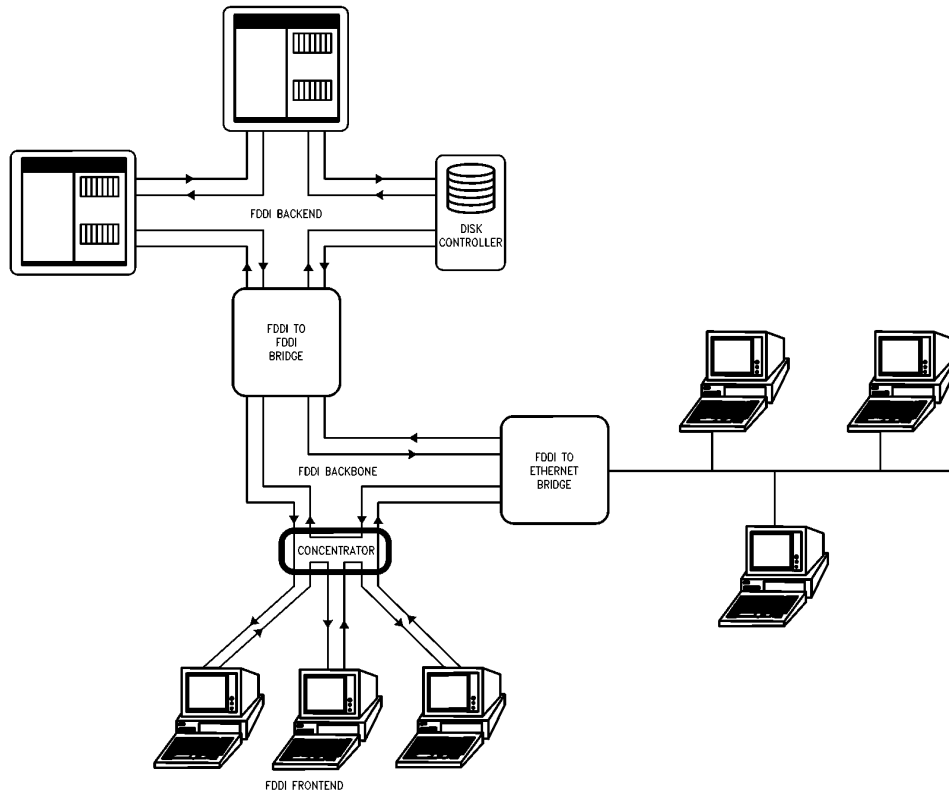
FDDI Concentrator

National Semiconductor
System Brief 112
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FDDI Concentrator

FDDI Applications



TL/F/11005-1

SYSTEM DESCRIPTION

The Concentrator plays an important role in the Fiber Distributed Data Interface (FDDI) architecture. FDDI offers a whole range of network topology alternatives. The concentrator simplifies the wiring of networks and allows logical ring topologies to be created from the typical star wiring configuration. The concentrator provides a very reliable and economic method of obtaining fault tolerance. The concentrator provides drops to individual nodes in order to include them in the network. When the concentrator senses a failure on one of the drops, it 'heals' the ring by electronically bypassing that station. Properly designed concentrators can bypass any number of drops with no degradation in performance.

The concentrator is an extremely chip intensive system. The small footprint, low power consumption, and special bridging features provide the ideal solution for concentrator applications. Concentrators are ideal for the needs of interconnectivity as addressed through high performance FDDI networks.

KEY DESIGN CHALLENGES

Management Software

Developing the Network Management software to manage all aspects of the concentrator and participate in the network management protocols is not a trivial task. The concentrator is also the best location for network diagnostic support including network monitors.

Modular Design

Keeping the design modular, while maintaining its manageability and flexibility, can save design time and manufacturing costs. Key to the architecture is to provide high throughput and flexibility to interface to a variety of system configurations.

In a multiboard design several other design challenges are present including other clock distribution, multi-processor communication, and backplane design issues.

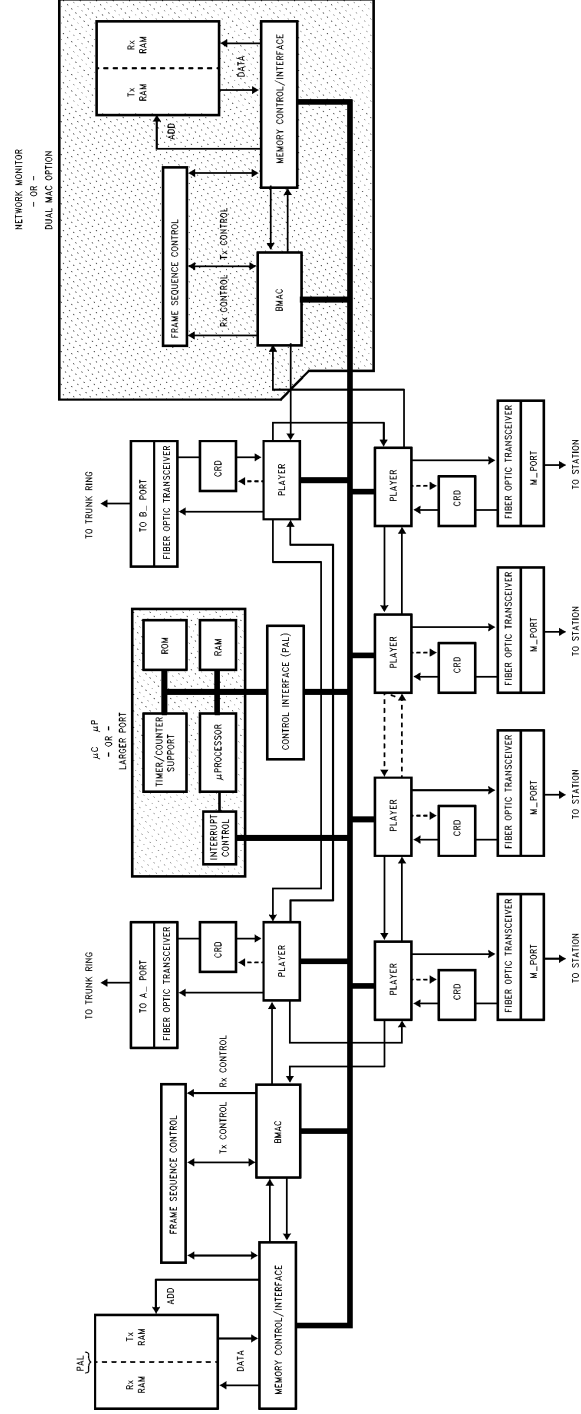
Clock Distribution

Each port within a concentrator requires 125 MHz and 12.5 MHz clocks; the distribution of these clocks is not a simple task; the CDD device provides an elegant solution.

BMAC™, CDD™, CRD™ and PLAYER™ are trademarks of National Semiconductor Corporation.

SB-112

System Diagram



Single Board Concentrator Design

TL/F/11005-2

KEY COMPONENTS

PLAYER™ (Physical Layer Controller) device converts the BMAC device Mbyte stream into an encoded bit stream as specified in the FDDI PHY standard. It synchronizes the received bit stream to the local clock and decodes the 4B/5B data into internal code. The PLAYER device also contains a configuration switch for use in dual attachment stations and concentrators.

BMAC™ (Basic Media Access Controller) device implements the functions defined by the ANSI X3T9.5 FDDI Media Access Control (MAC) standard. The device consists of the transmit and receive state machines, an address magnitude compare unit, a CRC generator and checker, protocol timers, and diagnostic counters.

CDD™ (Clock Distribution Device) device generates the clocks required by the PLAYER and BMAC devices, one per board.

CRD™ (Clock Recovery Device) device extracts specific incoming clock data from the upstream station. Its features include on-chip loopback control, crystal control, the ability to lock to a master line state in less than 100 μ s, and a single +5V supply.

NS32GX32
or HPC

Performs the control interface with fast and flexible I/O control, efficient data manipulation, and high speed computation.

BILL OF MATERIAL

Function	Description	Part No.	Quantity
Controller	BMAC	DP83261	1/2
Controller	PLAYER	DP83251/55	4
Clock Distribution	CDD	DP83241	1(4)
Clock Recovery	CRD	DP83231	4
Controller or	HPC or	HPC16400	1
Processor	GX	NS32GX32	1
Logic	PAL		1
RAM	8k DRAM or		1
	16k SRAM		1
Power	+5V Supply		1

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