Laser Beam Printer (LBP) Controller Solution Card

National Semiconductor
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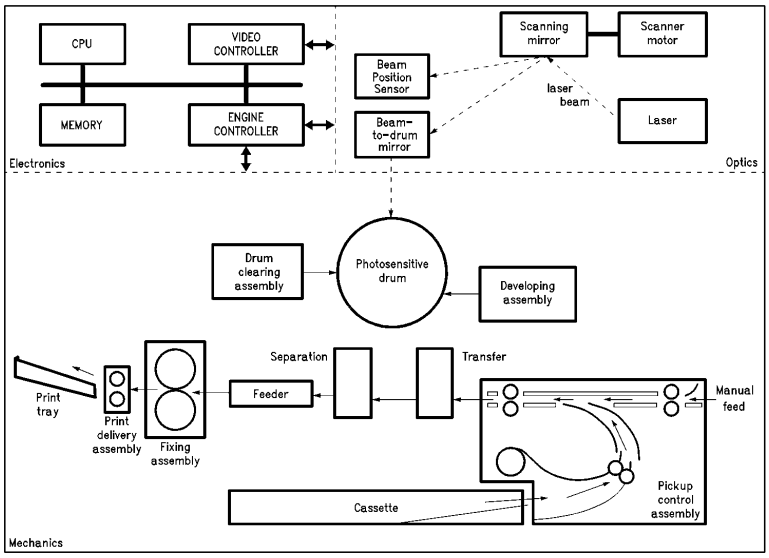

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FIGURE 1. A Laser Printer Block Diagram

SYSTEM DESCRIPTION

A Laser Beam Printer (LBP) can be divided into three sections: mechanics, optics, and electronics, as can be seen in *Figure 1*. The mechanics of an LBP handle the physical path of the paper. The optics generate the laser beam and synchronizing signals. The electronics control the laser printer operation and are often referred to as the LBP formatter or RIP (Raster Image Processor).

The LBP formatter performs computation and control tasks aimed at transferring images, provided by the host computer in a Page Description Language (PDL) format, to the bitmap image that is sent to the printer optics and mechanics. The PDL contains the instructions needed to create the imaged page, a task that requires a high performance 32-bit CPU. In addition the formatter controls the operation of the user panel and the printing engine. Inputs are received from microswitches, sensors, and the video controller. Outputs are fed to motors, solenoids, relays, and the video controller.

Embedded processors are specifically targeted to execute in the imaging environment. A family of processors to cover low-to-high range LBP applications is available, with different degrees of performance and integration. The choice of an embedded processor for a non-impact printer controller is of high importance. The processor should be selected by considering its impact on the system cost and performance. The applicability of the instruction set, integration, bus interface, and development tools are important issues.

Figure 2 shows a block diagram of an LBP controller. The choice of CPU, for high-performance printer formatters, or for mid-range performance should have the same level of integration, including on-chip Interrupt Control Unit (ICU), 2-channel DMA Controller (DMAC), and 3 timers/counters. The hardware Floating Point Unit (FPU) is optional. It increases the system performance, typically by 20%, when running PostScript™. For small memory systems a 16-bit data bus is provided, which is fully transparent to the internal 32-bit architecture. A 32-bit external data bus, with burst mode, is used for high-performance systems. The control logic, the 32-bit video shifter, the printer mechanism control, and the keyboard display control, may all be implemented in a system ASIC. To support RS-232 serial interface, and a Centronics type interface. UART with parallel interface, or a UART with FIFOs, parallel interface, and decode logic, may be used.

PDLs are large programs requiring large amounts of memory for code, font and image storage. The code and font require 512 kBytes for a PCL™ style printer, and 1.5 MBytes for a PostScript type printer.

RRD-B30M105/Printed in U. S. A.

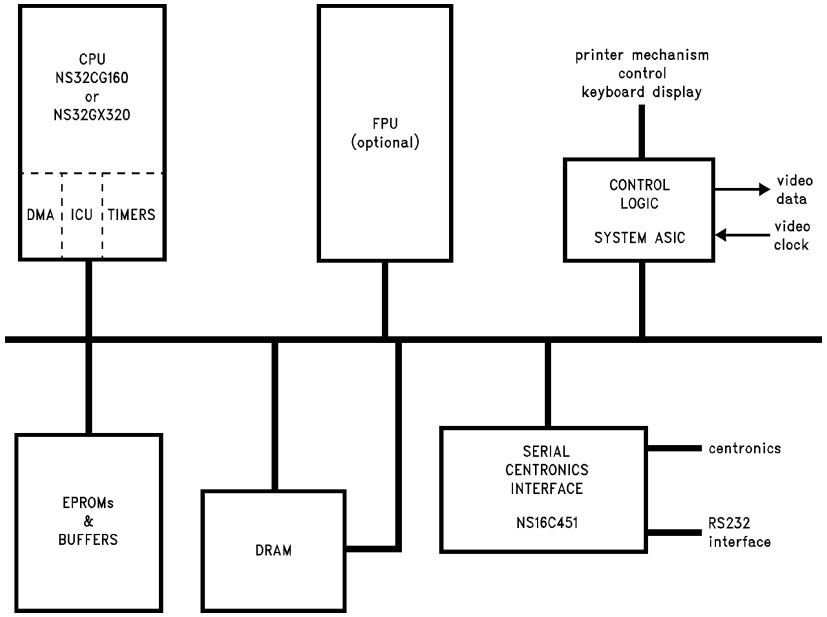

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FIGURE 2. Block Diagram of a Laser Printer Controller

DESIGN CHALLENGES

Performance

Get the best performance for the price.

For a solid performance of 4 to 15 pages per minute (ppm) printer the NS32CG16, NS32CG160, and NS32FX16, are recommended. For printers of 15 ppm and beyond the NS32GX32 and NS32GX320 are the processors of choice.

Component Count

Reduce component count through efficient bus architecture, integration, and code density.

Code Compactness

Series 32000® Architecture code is the most compact in the industry, and may be some 60% less is size then a generic RISC code, which relates to fewer EPROMs in the system for lower cost and smaller size.

Graphics Support

Graphics supported by dedicated on-chip hardware and specialized instructions for printer operations.

KEY COMPONENTS

NS32CG16, NS32CG160, NS32FX16, NS32GX32 or NS32GX320, NS32081, NS32181 or NS32381	CPU Function FPU Function
NS32CG821	DRAM Controller Designed to Interface with Series 32000 Embedded Processor
NS16C451/NS16C551	UART with Parallel Interface, (FIFOs, and Decode Logic)
EPROM	Program and Font Storage
DRAM	Working Space and Data Buffers
EEPROM	Setup Storage

BILL OF MATERIAL OF MAJOR COMPONENTS 15 PPM LBP CONTROLLER

Function	Description	NSC Part	Other Mfg	Qty
CPU	Embedded Processor	NS32GX320		1
FPU	Floating-Point Unit	NS32381		1
Interface	Serial and Parallel Interface	NS16C451		1
Memory				
EPROM	1 Mbyte	NMC27C010		8
DRAM	4 Mbyte			
EEPROM Memory Control	256 Byte DRAM Controller	NMC93CS56 NS32CG821		1 1
Logic				
System ASIC	Interface	(Note 1)		1

Note 1: The system ASIC may be designed using National's ASIC capabilities.

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