An FDDI—Ethernet Router

National Semiconductor
System Brief 115
November 1990

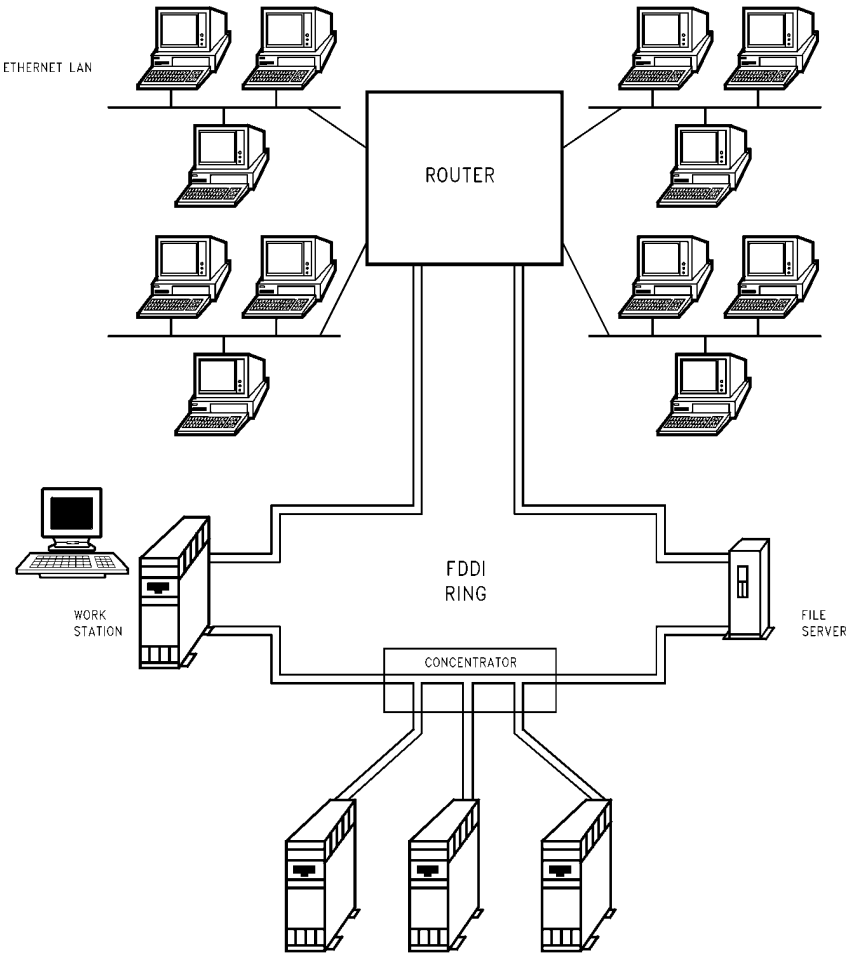

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FIGURE 1. A Router Configuration in a Typical Network

SYSTEM DESCRIPTION

A router connects multiple networks and routes packets between them. *Figure 1* illustrates a typical router configuration. Here, a dual attach FDDI node and four Ethernet ports enable the router to interconnect an FDDI ring and up to four Ethernet LANs. The FDDI and Ethernet interfaces are implemented using high performance peripherals: the DP83200 FDDI chip set and the DP83932 Systems Oriented Network Interface Controller (SONIC™).

TCP/IP is an industry standard for networking and many routers implement the IP protocol. The router presented here implements TCP/IP in full, providing reliable routing of packets across multiple networks. In doing so it offers such services as confirmation of packet delivery, packet routing and fragmentation, error reporting, address filtering and so on. Such a software intensive application requires a highly integrated, high performance embedded processor and therefore the NS32GX320 was chosen.

Figure 2 illustrates the router architecture. It consists of two 32-bit wide buses that separate network traffic from the processor bus activity. Each contains a 4/16 Mbyte bank of DRAM: one for the GX320 to run it's application software and the second for buffering received packets and queuing new ones to be transmitted.

In addition, there is a third ''bus'' for accessing the FDDI chip set registers and all the 8-bit system devices, such as EPROMs, an EEPROM, a UART and a SCSI controller.

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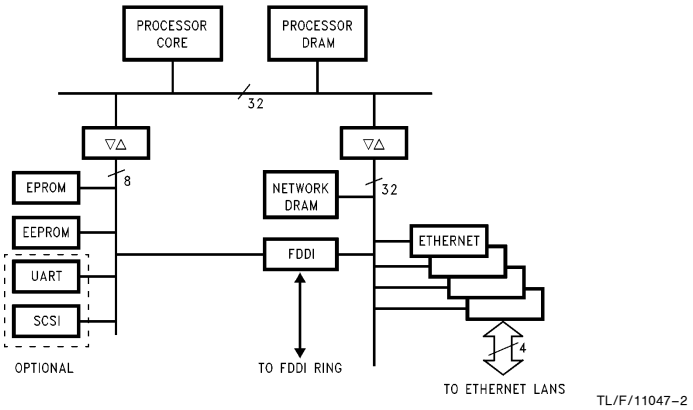


FIGURE 2. The Router Block Diagram

DESIGN CHALLENGES

Throughput and Bandwidth Considerations

A router must be able to process frames arriving at a peak rate of 100 Mbits/sec over the FDDI ring and 10 Mbits/sec on each of the four Ethernet LANs and then route them back onto the network with minimum latency. This is achieved using the above architecture and National Semiconductor's advanced chips.

Application Software

The application software plays a dominant role in a router. The software design consists of a router program and TCP/IP protocol (compatible with BSD UNIX 4.3 implementations of Routed and TCP/IP, respectively), buffer management and device drivers. Also included is FDDI SMT (Station Management) software. All these modules must run coherently to produce high performance and throughput.

Future Expansion

The router's design accommodates future enhancement and expansion. It may also serve as a hardware platform for other applications such as a multiple network file server or a network printer interface.

KEY COMPONENTS

a. DP83200 FDDI Product.

Includes: BSI, BMAC, PLAYER, CRD, CDD Devices and SMT software. The FDDI chip set fully implements a 32-bit wide system interface, all MAC (Media Access Control) functions and the physical layer interface to the fiber optic ring. The FDDI Product also includes FDDI SMT software.

b. DP83932 SONIC

The Systems Oriented Network Interface Controller provides a 32-bit wide system interface, implements all MAC functions and includes an ENDEC (Encoder-Decoder) for the serial interface to an Ethernet transceiver.

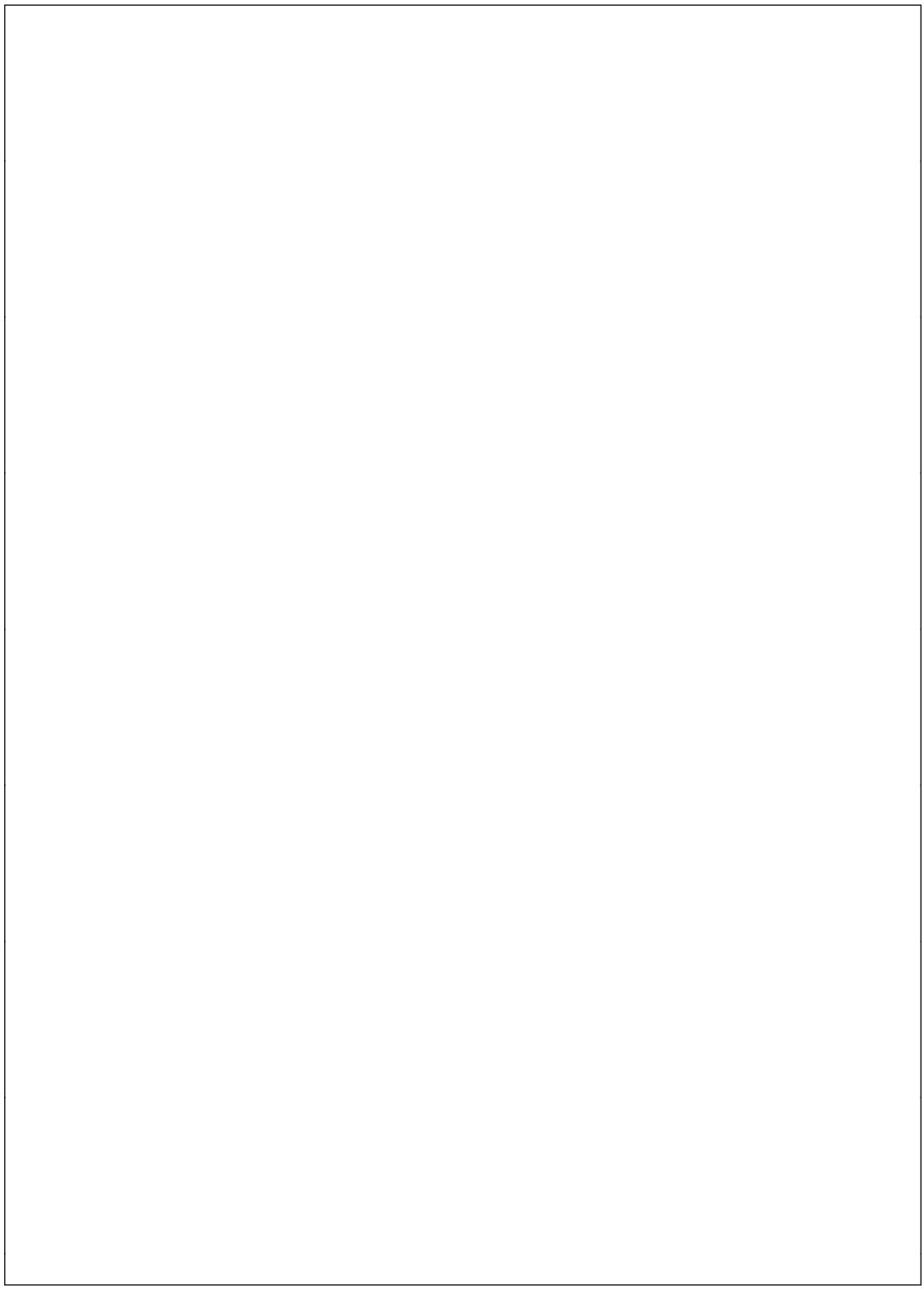
c. NS32GX320

The GX320 is a highly integrated, high performance embedded system processor designed for computation intensive applications. It incorporates a four stage instruction pipeline, on chip instruction and data caches and a hardware multiplier unit. The internal organization allows for a high degree of parallelism in instruction execution.

Integrated on the same chip with the CPU are also a two channel DMA controller, a fifteen level Interrupt Controller Unit and three 16-bit timers.

BILL OF MATERIALS

Function	Description	Part No.	Quantity
System Processor	Embedded Controller	NS32GX320	1
Controller	BSI™	DP83265	1
Controller	BMAC™	DP83261	1
Controller	PLAYER™	DP83255	2
Clock Recovery	CRD™	DP83231	2
Clock Distribution	CDD™	DP83241	1
Controller	SONIC	DP83932	1
Memory	4/16 Mbyte Bank of DRAM		2
Logic	PAL®s/GAL®s Octels		17 12
Optical	Transceivers		2
Power	+5V, +12V, −12V		1



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