FDDI—Adapter Card

National Semiconductor
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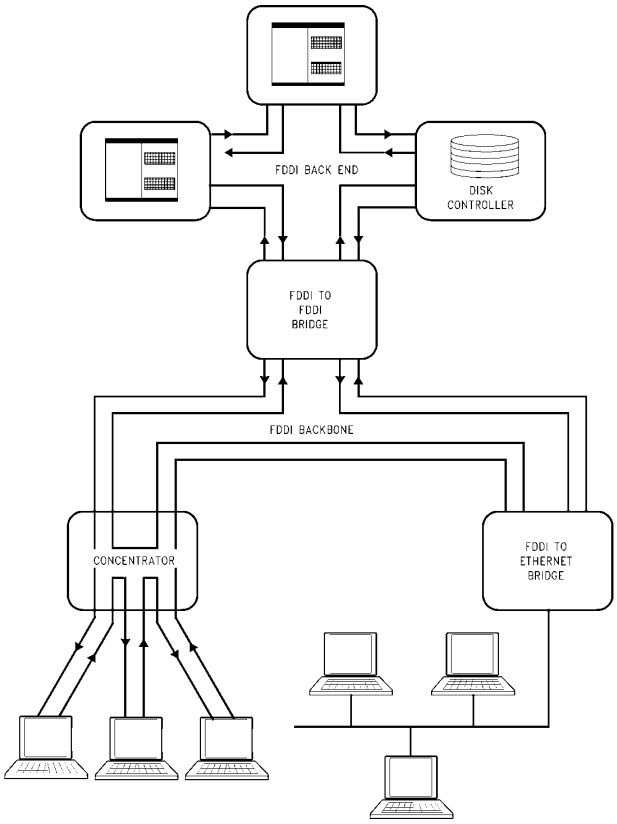

FIGURE 1. System Diagram of Adapter Cards Found in WS/PCs and the Concentrator

SYSTEM DESCRIPTION

Computer vendors have unique system architectures like countries of the world have different languages. The goal of an FDDI adapter card is to bridge the ''language barrier'' between the host and an FDDI network in a speedy and efficient manner. Choosing the interface that best fits the application is the key to achieving this goal.

The National Semiconductor FDDI chipset provides a simple but powerful interface that can deliver the potential bandwidth of an FDDI network to a wide variety of system architectures. This interface gives the designer the flexibility to define systems which require high network bandwidth with minimal latency or systems in which footprint size and system cost are the most important constraints.

An example of the need for a high bandwidth network can be found in a factory environment. Such a network would be responsible for tying together time critical tasks in a highly reliable manner. An FDDI network, which is fiber based and inherently reliable, is ideally suited for this application. The interface from the FDDI network to the system host must provide low latency and high throughput. With the National Semiconductor FDDI chipset, it is possible to connect directly to the system bus as a bus master with a peak bandwidth of 96 megabytes per second. In this configuration, the constraints of the design are met with a solution that is efficient and requires little or no external logic.

Workstations that pack supercomputer power, fit into a footprint that fits on a desktop, and cost under $10,000 are leading edge example of the evolutionary growth of computer technology. This ability to process information at break neck speeds has increased the need for high bandwidth, cost effective networking solutions that can effectively connect these systems. Features of the National Semiconductor chipset allow the designer to tailor the network interface to satisfy constraints imposed by the host architecture. For example, the chipset may be connected directly as a bus master on the system bus or through shared memory which may use low-cost DRAMs or faster SRAMs. Bit ordering and high-speed protocol processing are also handled by the National Semiconductor FDDI implementation. Additionally, the chipset can easily be used to implement an FDDI concentrator which delivers the power of FDDI at a lower cost by reducing the number of networking ICs built into each end station.

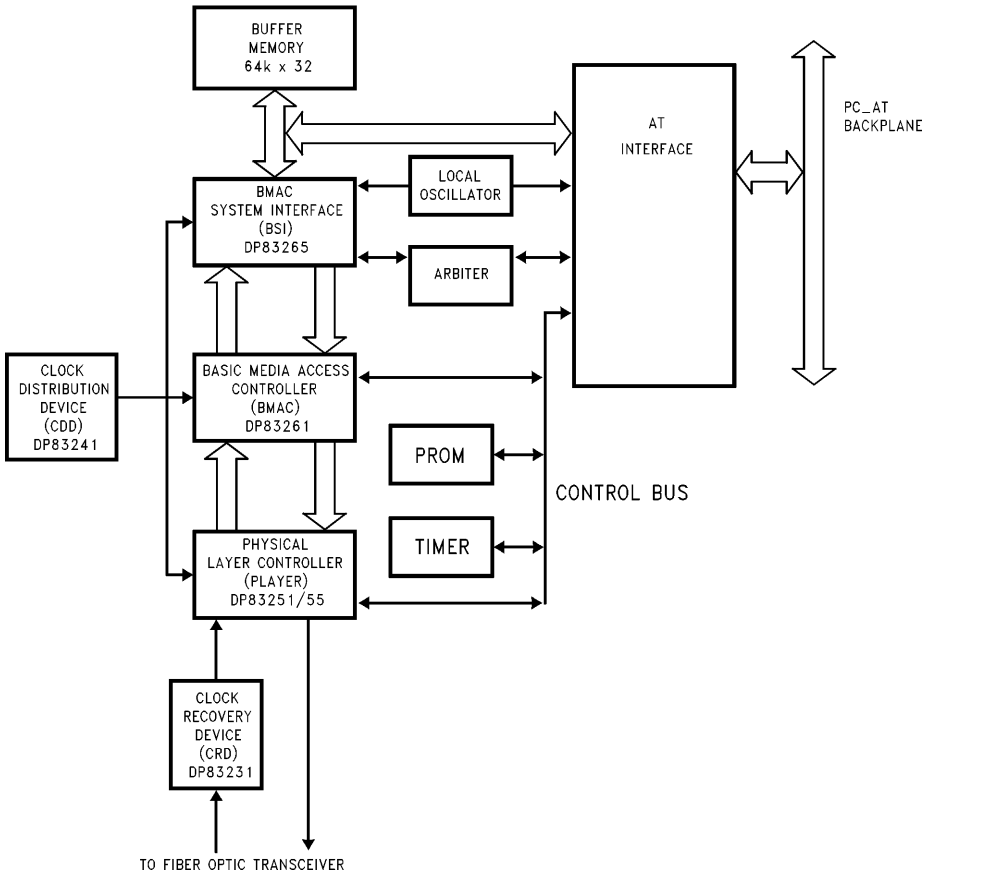

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FIGURE 2. Example of AT Based FDDI Adaptor Card

MAJOR CHALLENGES

1. Choice of an FDDI implementation

   A successful adapter card design must first start with the best FDDI solution. The National Semiconductor FDDI chipset offers a full-featured and complete solution.

2. Design of the network/host interface

   The design of an FDDI interface must eliminate data bottle necks without demanding excessive design complexity or component count. The National Semiconductor FDDI chipset provides full FDDI bandwidth through a simple but powerful system interface. This interface can be tailored to create an optimal interface to a variety of system architectures.

3. Future integration

   In order to maintain a leadership position in FDDI networking, an FDDI vendor must follow the same evolutionary path on the performance/value curve that has been defined by the computer industry. National Semiconductor has developed an aggressive strategy to provide the user with a consistent interface to work with while driving toward a one chip FDDI solution.

KEY COMPONENTS

DP83261 Basic Media Access Controller (BMAC™ Device)
DP83255/51 Physical Layer Controller (PLAYER™ Device)
DP83231 Clock Recovery Device (CRD™ Device)
DP83241 Clock Distribution Device (CDD™ Device)

The four devices listed above compose an FDDI-compliant, full-featured networking solution. The solution offers a full-duplex data pipe that delivers maximum FDDI bandwidth. Additional features include a thorough SMT interface and provisions for the straight forward design of bridges, routers, and concentrators.

DP83265 BMAC System Interface (BSI™ Device)

The BSI provides a simple but powerful system interface. The architecture can be connected directly to the host bus as a bus master or connected to the host through a shared memory architecture which uses low-cost DRAMs or faster SRAMs.

BILL OF MATERIAL

Function	Description	Part No.	Quantity
System I/F	BSI	DP83265	1
Controller	BMAC	DP83261	1
Controller	PLAYER	DP83251/55	1
Clock Recovery	CRD	DP83231	1
Clock Distribution	CDD	DP83241	1
SMT Node Processor	Embedded Controller	HPC46003	1
SMT Timer	Real Time Clock	DP8570A	1
Memory	DRAM/SRAM PROM	(if necessary) 	 1
Logic	PALS/GALS Octels	(if necessary) (if necessary)	
Fiber Optic Transceivers	125 MHz RX/TX		2

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408