NM95C12 Flexibility in Industrial Control Applications

National Semiconductor
Application Note 755
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INTRODUCTION

This application note describes a general purpose industrial controller and details how a NM95C12 can be used to integrate a number of different functions typically found in such a design.

General purpose application examples of the use of the NM95C12 are presented rather than a specific design. Each design idea and software can be incorporated into the designer's required application.

The basic building blocks of an industrial controller (for example, heating, process control, etc.) are a microcontroller, an Analogue to Digital Converter (ADC), an EEPROM, a display (LCD, LED, etc.), I/O interfaces, and power driver/control circuits. The NM95C12 forms the basis of this design performing the non-volatile parameter storage, a low cost ADC, an I/O expander, and providing a simple control interface.

Figure 1 shows the basic block diagram with the shaded parts representing the functions performed by the NM95C12.

This application note will describe the theory of operation behind the design and give detailed software examples to show how to interface a popular microcontroller to the NM95C12.

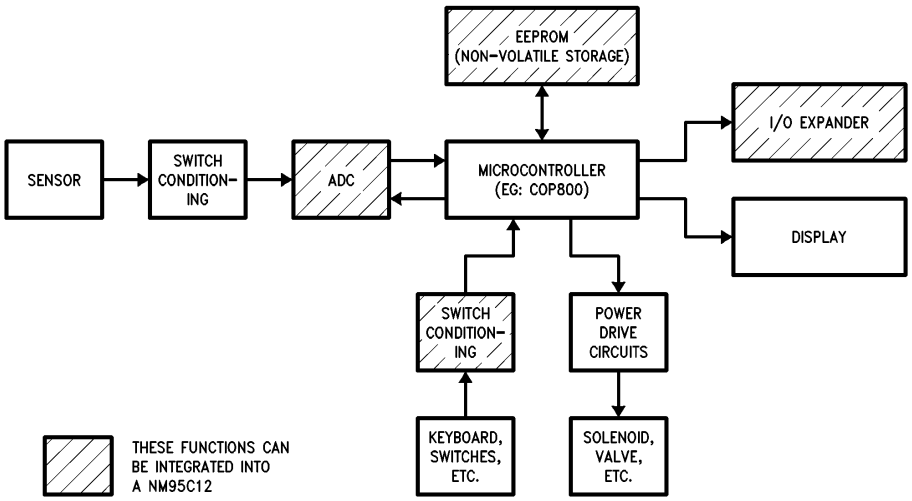

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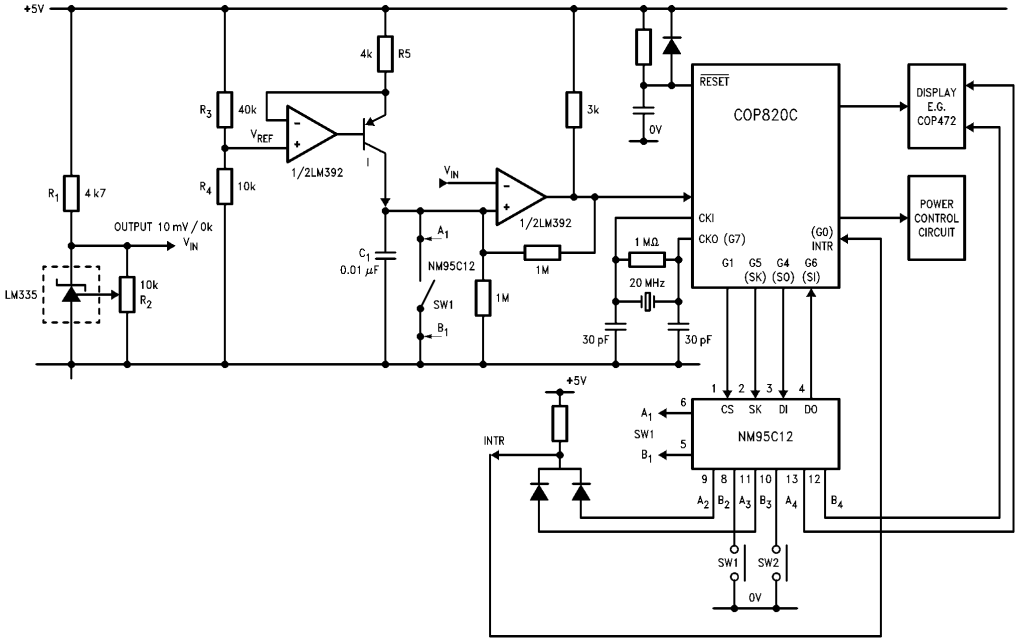
FIGURE 1. Typical Industrial Controller Block Diagram



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COP820/NM95C12 Industrial Controller

THE NM95C12 1024-BIT CMOS EEPROM WITH DIP SWITCHES

The NM95C12 features 1K-bit EEPROM memory with 8 switch logic terminals. These switch logic terminals are individually programmable outputs which may be used as DIP switch positions or as SPST switch positions.

The NM5C12 uses the MICROWIRE™ serial I/O interface which is fully compatible with COPS™ microcontrollers via 4 simple control lines:

SK — Serial Clock

CS — Chip Select

DI — Data In

DO — Data Out

The EPROM array (addresses 0 to 60) is addressed via five instructions:

READ — Read Data from register

WEN — Write enable

WRITE — Writes data to register

WRALL — Writes to all registers

WDS — Disables all programming instructions

This area of memory is used for the normal EEPROM applications such as the storage of user changeable, non-volatile parameters such as time on/off, temperature on/off limits, etc.

CONTROLLING THE SWITCH LOGIC

Address locations 61 to 63 control the switch operation.

Address	Name	Description
61	ISS	Provides the initial switch configuration automatically on power-up. Controlled via a WRITE operation.
62	SCR	The SCR is not an E2 location and hence is volatile. The SCR is loaded automatically from address 61 on power-up. The SCR controls the switch terminals A1–A4 and B1–B4.
63	SRR	The SRR allows the current logic levels of the switch terminals to be read back via the MICROWIRE bus.

THEORY OF OPERATION

The relationship for charge of a capacitor is as follows:

Charge (Q) = Voltage (V) × Capacitance (C)
= Current (I) × Time (T)

Therefore the voltage across the capacitor, V_{CAP}

$V_{CAP} = (I \times T)/C$

Assuming that the current I is a constant source, and the capacitance value C does not vary gives:

V_{CAP} is proportional to T.

Mode of Operation

— initially switch S1 is closed to short out V_{CAP} to measure input voltage V_{IN}

To Measure V_{IN}:

— microcontroller opens S1 and starts internal timer at T1

— V_{CAP} is proportional to time T

— when $V_{CAP} > V_{IN}$ then comparator output V_{COMP} goes high

— microcontroller stops internal timer at T2

— V_{IN} is proportional to time T = T2 − T1

— microcontroller closes S1 ready for next measurement

CURRENT SOURCE/VOLTAGE COMPARATOR FOR ADC

This is based on a LM932 which has an Operational Amplifier and a Voltage Comparator in the same 8-pin package. This device operates from a single +5V supply.

Refer to the National Semiconductor General Purpose Linear Databook for further details of the LM392.

INPUT SENSOR

For this example assume temperature needs to be controlled.

LM335: This is a precision, low-cost, easily calibrated two terminal temperature sensor that behaves like a zener diode with a voltage of +10 mV/degree Kelvin. The initial accuracy is ±1° and can be externally trimmed with a potentiometer connected to the ADJ pin.

Refer to the National Semiconductor Linear Databook 2 for further details of the LM335 Temperature Sensors.

NM95C12 SWITCH LOGIC APPLICATIONS/ CONFIGURATIONS

A_1, B_1—Control the Charge/Discharge of Capacitor for ADC

Switch Configuration:

Analog Switch Open: Mode 12, ZYXW = 110?
(? = don't care)

Analog Switch Closed: Mode 13, ZYXW = 111?

To change the state of the switch terminals A_1, B_1, follow the flowchart in *Figure 3*.

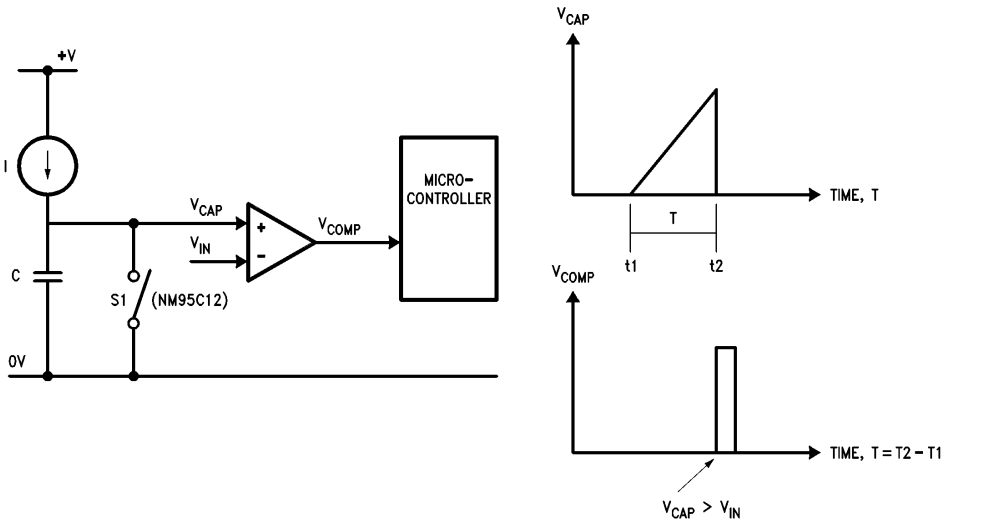

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FIGURE 2. Single Slope Analogue to Digital Converter

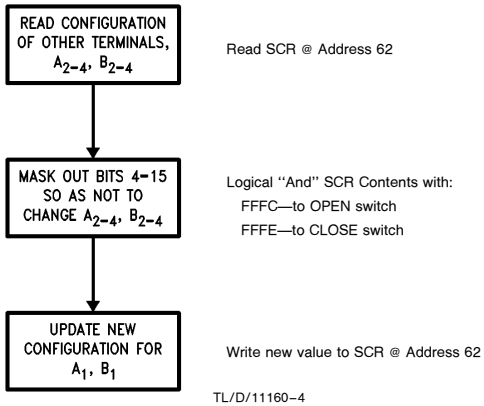

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FIGURE 3. Controlling Switch Terminals A1, B1

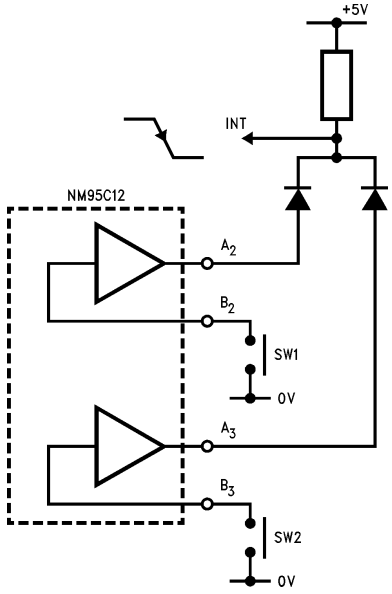
A_2, B_2 and A_3, B_3 — Switch Debouncing

The switch logic configuration is shown in *Figure 4*. When either of the mechanical switches SW1 or SW2 are pressed, this causes the interrupt line (INT) to be pulled low signalling to the microcontroller that a switch has been pressed. As part of the interrupt service routine the microcontroller can generate a delay to allow time for mechanical switch debouncing, before reading the NM95C12 SRR to determine which mechanical switch was pressed.

The advantage of this design is that it saves input pins on the microcontroller and means that the software does not have to perform periodic polling of the inputs to determine the mechanical switch status since the circuit is interrupt driven.

Switch Configuration: both A_2,B_2 and A_3,B_3 will be configured in mode 5; ZYXW = 0101.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 5*.



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A_2,B_2, A_3,B_3 Configured in mode 5, ZYXW = 0101

FIGURE 4. Switching Conditioning

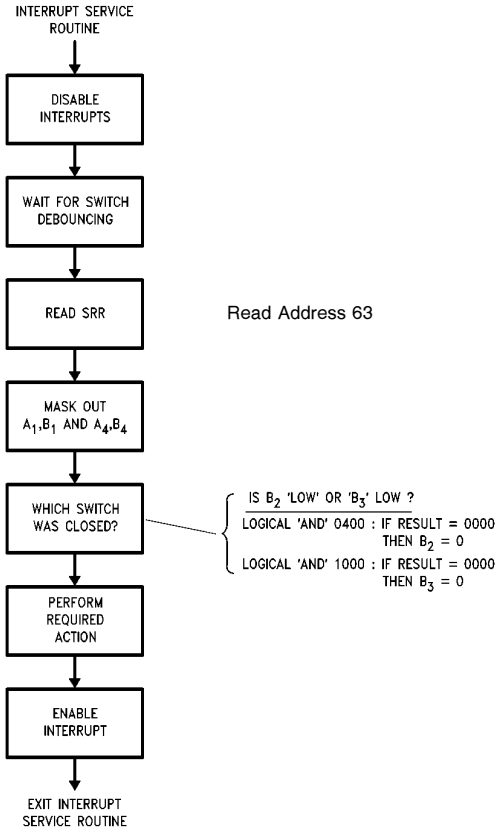

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FIGURE 5. Controlling Switch Terminals A_2,B_2, A_3,B_3

A_4,B_4 Programmable I/O

These two terminals use mode 1 to 4 according to the logic level required on the output. In this example A_4 is used for the Display Chip Select signal and B_4 is used for the Display On/Off control signal.

In order to update and display the contents of the Display then both terminals A_4 and B_4 need to be set to a logic ''1'' therefore A_4,B_4 are configured in mode 3 with ZYXW = 0011.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 6*.

SOFTWARE TO INTERFACING THE NM95C12 TO THE COP820 MICROCONTROLLER

This section includes a number of subroutines to interface to a NM95C12 as described in the design example above. There are subroutines to implement each of the basic instructions together with routines for configuring and controlling the switch logic. These subroutines can be used as the basis for a design and be tailored to meet the individual application requirements.

CONCLUSION

The NM95C12 is an extremely versatile and inexpensive device which allows simple interfacing to all popular microcontrollers and microprocessors via a 4-wire serial bus. The complete operation of the NM95C12 can be controlled by a few simple instructions.

The design outlined offers an inexpensive solution for industrial control applications with the key benefits of:

— simple interfacing between microcontroller, EEPROM, ''ADC''

— low part count

— fully software controlled and changeable

This has highlighted the flexibility of the NM95C12 and how the switch terminals can be configured for a wide range of applications including: mechanical switch replacement, programmable Address Decoder, programmable I/O expander and a programmable interrupt controller. The NM95C12 offers greater reliability than mechanical switches with the benefits of software control and lower cost.

Plus you still get the 1K-bit EEPROM memory as well!; together with the 8 switch terminals it forms a truly remarkable device.

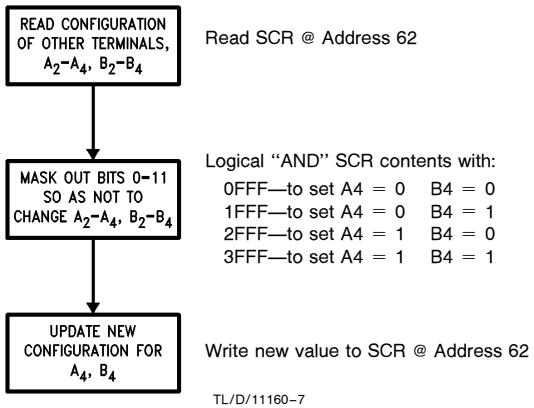

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FIGURE 6. Controlling Switch Terminals A_4,B_4

```
;
; THIS FILE PREDECLARES ITEMS FREQUENTLY USED BY THE
; COP820 PROGRAMMER.
; REGISTER NAMES, CONTROL BITS, ETC. ARE NAMED THE SAME WAY
; AS IN THE DATA-SHEETS.
;
; ************************************************
; * PORT~ , CONFIGURATION- AND CONTROL REGISTERS  *
; ************************************************
      PORTLD   =   0D0         ; PORT L DATA
      PORTLC   =   0D1         ; PORT L CONFIGURATION
      PORTLP   =   0D2         ; PORT L PIN
;
      PORTGD   =   0D4         ; PORT G DATA
      PORTGC   =   0D5         ; PORT G CONFIGURATION
      PORTGP   =   0D6         ; PORT G PIN
      PORTD    =   0DC         ; PORT D
      PORTI    =   0D7         ; PORT I
;
      SIOR     =   0E9         ; SID SHIFT REGISTER
      TMRLO    =   0EA         ; TIMER LOW BYTE
      TMRHI    =   0EB         ; TIMER HIGH BYTE
      TAULO    =   0EC         ; TIMER REGISTER LOW BYTE
      TAUHI    =   0ED         ; TIMER REGISTER HIGH BYTE
;
      CNTROL   =   0EE         ; CONTROL REGISTER
      PSW      =   0EF         ; PSW REGISTER
;             ********************
;             * CONSTANT DECLARE *
;             ********************
;              ---- CNTRL - REGISTER BITS ----

;
      TSEL     =   7
      CSEL     =   6
      TEDG     =   5
      TRUN     =   4
      MSEL     =   3
      IEDG     =   2
      S1       =   1
      S0       =   0
;
;              ---- PSW- REGISTER BITS ----
      HCARRY   =   7
      CARRY    =   6
      TPND     =   5
      ENTI     =   4
      IPND     =   3
      BUSY     =   2
      ENI      =   1
      GIE      =   0

;             I/O - SIGNALS ----
;
      TMRINP   =   3
      INTR     =   0
      TIO      =   3
      SO       =   4
      SK       =   5
      SI       =   6
      CKO      =   7
;
      .CHIP    820
      LD       SP,#02F          ; DEFAULT INITIALIZATION OF SP
```

```
;INCLD COP820.INC
;
; This program provides in the form of subroutines, the ability to enable,
; disable, read and write to the NM95C12 EEPROM with DIP switches.
;
;       ***********************************************
;       * PROGRAM VARIABLE MEMORY LOCATION DEFINITIONS  *
;       ***********************************************
;
SNDBUF  = 0 ;CONTAINS THE COMMAND BYTE TO BE WRITTEN TO NM95C12
RDATL   = 1 ;LOWER BYTE OF THE NM95C12 REGISTER DATA READ
RDATH   = 2 ;UPPER BYTE OF THE NM95C12 REGISTER DATA READ
WDATL   = 3 ;LOWER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
WDATH   = 4 ;UPPER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
ADDRESS = 5 ;THE LOWER 6-BITS OF THIS LOCATION CONTAIN THE ADDRESS
            ;OF THE NM95C12 REGISTER TO BE READ/WRITTEN
FLAGS   = 6 ;USED FOR SETTING UP FLAGS
            ;
            ; FLAG VALUE        ACTION
            ; ----------        ------
            ;    00             WRITE ENABLE,DISABLE,WRITE ALL
            ;    01             READ CONTENTS OF NM95C12 REGISTER
            ;    03             WRITE TO NM95C12 MEMORY REGISTER
            ;    07             WRITE NM95C12 SCR REGISTER
            ;    OTHERS         ILLEGAL COMBINATION
;
; THE INTERFACE BETWEEN THE COP820C/840C AND THE NM95C12 (1024-BIT EEPROM)
; CONSISTS OF FOUR LINES. THE G1 (CHIP SELECT LINE), G4 (SERIAL OUT SO),
; G5 (SERIAL CLOCK SK) AND G6 (SERIAL IN SI).
;
; ANOTHER PINS USED BY THIS DESIGN IS G0 (INTERRUPT INTR)
;
;
;       ******************
;       * INITIALIZATION *
;       ******************
;
        LD PORTGC,032     ;Setup G1,G4,G5 as outputs
        LD PORTGD,00      ;Initialize G data reg to zero
        LD CNTROL,08      ;Enable MSEL, select MW rate of 2tc
        LD B,fPSW         ;Load B with address of PSW
        LD X,fSIOR        ;Load X with address of Serial I/O Register
;
;
;
;       ********************
;       * WEN INSTRUCTION  *
;       ********************
;
; THIS ROUTINE ENABLES PROGRAMMING OF THE NM95C12. PROGRAMMING MUST
; BE PRECEDED ONCE BY A PROGRAMMING ENABLE (WEN).
;
WEN:
        LD  SNDBUF,f030   ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;       ********************
;       * WDS INSTRUCTION  *
;       ********************
;
```

```
;
; THIS ROUTINE DISABLES PROGRAMMING OF THE NM95C12.
;
WDS:
        LD  SNDBUF,f0       ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;
;       ********************
;       * READ INSTRUCTION *
;       ********************
;
;
; THIS ROUTINE READS THE CONTENTS OF THE NM95C12 REGISTER.
; THE NM95C12 ADDRESS IS SPECIFIED IN THE LOWER 6-BITS OF
; LOCATION "ADDRESS". THE UPPER 2-BITS SHOULD BE SET TO ZERO.
; THE 16-BIT CONTENTS OF THE NM95C12 REGISTER ARE STORED IN
; RDATL AND RDATH.
;
READ:   LD  A,ADRESS    ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f080      ; SET OP CODE BITS TO '10'
        X   A,SNDBUF    ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f1
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRITE INSTRUCTION *
;       *********************
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 REGISTER WHOSE ADDRESS IS CONTAINED IN THE
; LOWER 6-BITS OF THE LOCATION "ADDRESS". THE UPPER 2-BITS OF
; ADDRESS LOCATION SHOULD BE SET TO ZERO.
;
WRITE:  LD  A,ADRESS     ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f040       ; SET OP CODE BITS TO '01'
        X   A,SNDBUF     ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRALL INSTRUCTION *
;       *********************
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO ALL THE NM95C12 REGISTERS
;
WRALL:  LD  SNDBUF,f040  ; LOAD OP CODE AND ADDRESS'
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
```

```
;       **********************
;       * WRSCR 'INSTRUCTION' *
;       **********************
;
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 SCR (SWITCH CONTROL REGISTER) WHOSE ADDRESS IS 62 DECIMAL
; WHICH EQUALS f03E HEXADECIMAL. OP CODE = '01'
; A WRITE TO THE SCR DOES NOT REQUIRE A PROGRAMMING CYCLE
;
WRSCR:  LD  SNDBUF,f07E  ; LOAD OP CODE AND ADDRESS
        LD  FLAGS,f7
        JSR INIT
        RET
;
;
;
;       **********************************
;       * EXECUTE INSTRUCTION SUBROUTINES *
;       **********************************
;
;
;
; THIS ROUTINE SENDS OUT THE START BIT AND THE COMMAND BYTE.
; IT ALSO DECIPHERS THE CONTENTS OF THE FLAG LOCATION AND TAKES
; A DECISION REGARDING WRITE, WRITE SCR, READ OR RETURN TO THE
; CALLING_ROUTINE.
;
INIT:   SBIT 1,PORTGD    ;SET CHIP SELECT HIGH
        LD SIOR,f001     ;LOAD SIOR WITH START BIT
        SBIT BUSY,[B]    ;SEND OUT THE START BIT
PUNT1:  IFBIT BUSY,[B]
        JP PUNT1
        LD A,SNDBUF
        X  A,[X]         ;LOAD SIOR WITH COMMAND BYTE
        SBIT BUSY,[B]    ;SEND OUT COMMAND BYTE
PUNT2:  IFBIT BUSY,[B]
        JP PUNT2
        IFBIT 0,FLAGS    ;ANY FURTHER PROCESSING?
        JP NOTDON        ;YES
        RBIT 1,PORTGD    ;NO, RESET CS AND RETURN
        RET
;
NOTDON:
        IFBIT 1,FLAGS    ;READ OR WRITE?
        JP WR95C12       ;JUMP TO WRITE ROUTINE
        LD SOIR,f000     ;NO, READ NM95C12
        SBIT BUSY,PSW    ;DUMMY CLOCK TO READ ZERO
        RBIT BUSY,[B]
        SBIT BUSY,[B]
PUNT3:  IFBIT BUSY,[B]
        JP PUNT3
        X   A,[X]
        SBIT BUSY,[B]
        X   A,RDATH
```

```
PUNT4:  IFBIT BUSY,[B]
        JP PUNT4
        LD A,[X]
        X  A,RDATL
        RBIT 1,PORTGD
        RET
;
WR95C12:
        LD  A,WDATH
        X   A,[X]
        SBIT BUSY,[B]
PUNT5:  IFBIT BUSY,[B]
        JP  PUNT5
        LD  A,WDATL
        X   A,[X]
        SBIT BUSY,[B]
PUNT6:  IFBIT BUSY,[B]
        JP  PUNT6       ; FINISHED CLOCKING OUT DATA
        RBIT 1,PORTGD   ; RESET CHIP SELECT
        IFBIT 2, FLAGS  ; WRITE/WRALL OR WRSCR?
        RET             ; WRSCR , NO PROGRAMMING TIME SO RETURN
        SBIT 1,PORTGD   ; SET CHIP SELECT TO ALLOW TO POLL DO FOR BUSY/READY
POLL:   IFBIT SI,PORTGP ; IS NM95C12 DO = SI LOW?
        JP ENDTWP       ; DO HAS GONE HIGH, SO END PROGRAMMING CYCLE
        JP POLL         ; DO IS STILL LOW, SO KEEP POLLING
;
ENDTWP;
        BIT 1, FLAGS    ; RESET CHIP SELECT
        RET
;
        .END
```

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