Using the NM95C12 to Solve Common Manufacturing Problems

National Semiconductor
Application Note 756
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INTRODUCTION

This application note describes how the NM95C12 E^{2}P-ROM + Dip Switches is utilized to reduce manufacturing costs and increase reliability.

PROBLEM

The application described herein is a factory programmable power supply. The existing system *(Figure 1)* requires one of three different power supplies, depending on the options installed in the final unit. The design engineer has presented two solutions:

1. Three different assemblies, one for each output configuration, or,
2. One assembly with a dip switch (or jumpers) to select the configuration.

The manufacturing engineer would prefer to have one assembly that would satisfy all three needs. Dip switches are undesirable because they are difficult to flow solder when on the PCB (and later clean the PCB) as well as posing a threat to the final system should an untrained technician choose to change a switch setting (thus altering the output voltage). Jumpers are undesirable since they require hand soldering—an additional step.

The manufacturing engineer would prefer to have one final test program—not three.

THE SOLUTION

The NM95C12 provides the solution. It enables the power supply module to be configured for any of the three output voltages. There only needs to be one assembly. No dip switches or jumpers are used. The Automatic Test Equipment (ATE) used at final test can check all three configurations. The test program can set the final configuration as well as assign a serial number and date of manufacture which is stored in the EEPROM.

THE DESIGN

The power supply is designed using an LM2577 switching regulator (''the Simple Switcher'') in the flyback mode *(Figure 2)*. The resistor divider R_1/R_2 set the output voltages V_{OUT1} and V_{OUT2}. All three output voltages can be set by merely selecting which combination of R_1/R_2 is connected to the feedback pin of the switching regulator. When the switches in the NM95C12 are configured for the analog switch mode, they can be used to connect the appropriate switch to the feedback pin of the Simple Switcher™.

The manufacturing group need only produce one assembly which is electronically configured either at final test or during final assembly. An increase in manufacturing efficiency results.

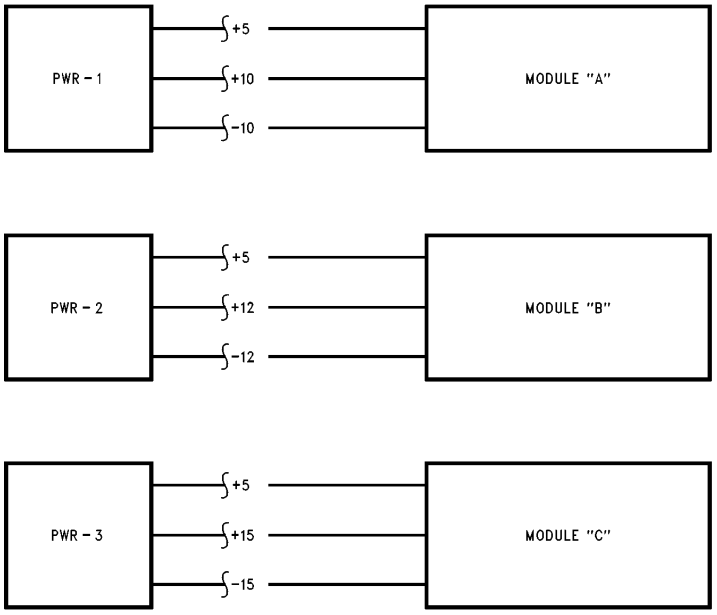

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FIGURE 1. Modules A, B, C Each Require Slightly Different Power Supply Modules

Simple Switcher™ is a trademark of National Semiconductor Corporation.

  RRD-B30M75/Printed in U. S. A.

During final test, the ATE can check each switch position by sending serial commands via the serial μWIRE interface of the NM95C12. The serial number and date of manufacture can be stored at this time. Output configuration can be selected at final test or the power supply modules can be stored and the output voltage programmed at a later time.

Note that there is no microcontroller necessary in the system. While the NM95C12 is typically utilized in a μController based system, it can also be used in non-μController applications. The ATE provides programming and control of the NM95C12 and connects to pads on the PCB via a bed-of-nails test fixture. Alternatively, the Clock, Data IN, Data OUT and Chip Select lines can be routed to fingers on an edge connector.

PROGRAMMING

The programming example is written in the popular Z80 assembly language. An NSC800 is used for this example. Flow charts are shown for each module.

SUMMARY

The NM95C12 is used in this application to replace a dip switch. The user benefits in many ways:

1. Increased efficiency by manufacturing 1 large lot of sub-assemblies rather than 3 smaller ones,
2. Ease of manufacturing since neither mechanical dip switches have to be treated with extra care nor jumpers specially installed,
3. Only 1 sub-assembly needs to be inventoried, cutting costs,
4. Increased reliability because mechanical devices are not used,
5. Increased efficiency at final test since only 1 test program can check all three configurations,
6. Inventory costs are reduced because 1 assembly will satisfy any of 3 different functions, and
7. A history of the module can be stored in the EEPROM portion of the device including serial number, date of manufacture, date of last repair, etc.

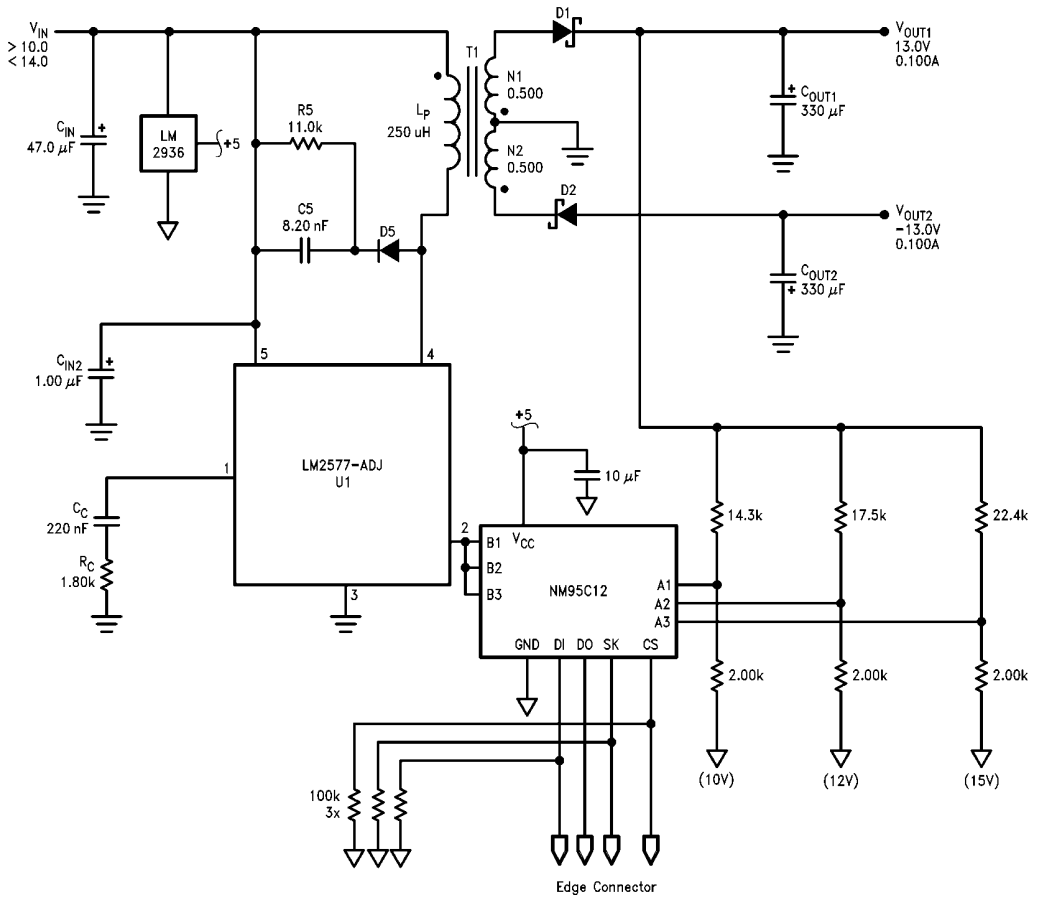
VIN
> 10.0
< 14.0
CIN
47.0 µF
LM
2936
+5
R5
11.0k
LP
250 uH
T1
N1
0.500
N2
0.500
D1
D2
D5
C5
8.20 nF
VOUT1
13.0V
0.100A
COUT1
330 µF
VOUT2
−13.0V
0.100A
COUT2
330 µF
CIN2
1.00 µF
LM2577-ADJ
U1
CC
220 nF
RC
1.80k
10 µF
NM95C12
B1 VCC
B2
B3
A1
A2
A3
GND DI DO SK CS
14.3k
17.5k
22.4k
2.00k
2.00k
2.00k
(10V)
(12V)
(15V)
100k
3x
Edge Connector
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FIGURE 2

```
;
;       THIS PROGRAMMING EXAMPLE IS A SAMPLE
;       THAT COULD BE USED TO PROGRAM THE NM95C12
;
;       IT IS WRITTEN IN Z80 ASSEMBLY LANGUAGE FOR THE NSC800



;
;       EQUATES:
;
READ    EQU     80H             ;READ COMMAND
WEN     EQU     00H+30H         ;WRITE ENABLE COMMAND
WRITE   EQU     40H             ;WRITE COMMAND
WRALL   EQU     00H+10H         ;WRITE ENTIRE MEMORY
WDS     EQU     00H             ;WRITE DISABLE
;
MODE0   EQU     0H              ;A=0,B=0
MODE1   EQU     1H              ;A=0,B=1
MODE2   EQU     2H              ;A=1,B=0
MODE3   EQU     3H              ;A=1,B=1
MODE4   EQU     4H              ;A=0,B=TS
MODE5   EQU     5H              ;A=B
MODE6   EQU     6H              ;A=B'
MODE7   EQU     7H              ;A=1,B=TS
MODE8   EQU     8H              ;A=TS,B=0
MODE9   EQU     9H              ;B=A
MODE10  EQU     0AH             ;B=A'
MODE11  EQU     0BH             ;A=TS,B=1
MODE12  EQU     0CH             ;ANALOG SWITCH OPEN
MODE13  EQU     0DH             ;ANALOG SWITCH CLOSED
;
OPEN    EQU     MODE12          ;
CLOSED  EQU     MODE13          ;
;
;       MASKS USED TO OPEN AND CLOSE SWITCHES
;
AB1CLO  EQU     0000FH          ;SWITCH 1 CLOSED
AB2CLO  EQU     000F0H          ;SWITCH 2 CLOSED
AB3CLO  EQU     00F00H          ;SWITCH 3 CLOSED
AB4CLO  EQU     0F000H          ;SWITCH 4 CLOSED
AB1OPN  EQU     0000CH          ;SWITCH 1 OPEN
AB2OPN  EQU     000C0H          ;SWITCH 2 OPEN
AB3OPN  EQU     00C00H          ;SWITCH 3 OPEN
AB4OPN  EQU     0C000H          ;SWITCH 4 OPEN
AB1MSK  EQU     0FFF0H          ;MASK
AB2MSK  EQU     0FF0FH          ;
AB3MSK  EQU     0F0FFH          ;
AB4MSK  EQU     00FFFH          ;
;
;       EEPROM MEMORY LOCATIONS
;
ENABLE  EQU     0               ;LOC 0,BIT 0=1 IF WR ENABLE
;                               ;           =0 IF WR DISABLED
SN      EQU     1               ;SERIAL NUMBER STORAGE
DATE    EQU     32              ;DATE STORED (DP8570 FORMAT)
PUSCR   EQU     61              ;SCR LOADED FROM HERE ON POWER UP
SCR     EQU     62              ;SWITCH CONFIGURATION REGISTER
SRR     EQU     63              ;SWITCH READ BACK REGISTER (READ ONLY)
```

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```
EEPORT: EQU     00H             ;I/O ADDRESS OF PARALLEL PORT
EE:     EQU     EEPORT          ;SHORTHAND


;       THE PARALLEL PORT IS CONFIGURED AS:
;
;               BIT 0 = DATA OUT     OUTPUT
;               BIT 1 = CLOCK        OUTPUT
;               BIT 2 = CHIP SELECT  OUTPUT
;               BIT 3 = N/U
;               BIT 4 = N/U
;               BIT 5 = N/U
;               BIT 6 = N/U
;               BIT 7 = DATA IN      INPUT
;
;       FOR THIS PROGRAMMING EXAMPLE:
;
;               H  = EEPROM OPCODE
;               L  = EEPROM ADDRESS
;               DE = 16 BIT DATA
;               B  = SHIFT COUNTER
;               C  = PORT DATA STORAGE
;               A  =

        ORG     1000H
;
;
;       MAIN PROGRAM
;
;       THIS SAMPLE PROGRAM SETS SWITCH 1 CLOSED, ALL OTHERS OPEN
;
MAIN:
        LD      H,WEN           ;ENABLE CODE FOR NM95C12
        CALL    WRCMD           ;SEND COMMAND
        LD      DE,AB1CLO+AB2OPN+AB3OPN+AB4OPN
                                ;SWITCH 1 CLOSED
                                ;SWITCH 2 OPEN
                                ;SWITCH 3 OPEN
                                ;SWITCH 4 OPEN
        LD      H,WRITE         ;EEPROM OPCODE
        LD      L,SCR           ;ADDRESS TO WRITE TO
        CALL    WRDATA          ;WR TO SWITCH CONFIGURATION RECISTER
        LD      H,WRITE         ;OPCODE
        LD       L,PUSCR                ;ADDRESS
        CALL    WRDATA          ;WR TO POWER UP SCR
        LD      H,WDS           ;WRITE DISABLE
        CALL    WRCMD           ;DISABLE FURTHER WRITING
        HALT                    ;END OF THIS EXAMPLE
```

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```
;
;       WRITE COMMAND SUBROUTINE
;
;       USE FOR "WEN" AND "WDS" COMMANDS
;
;       WRITES COMMAND TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;
WRCMD:
        CALL    PRECK           ;SET CS, CHECK FOR BUSY
        CALL    SHIFT8          ;SEND COMMAND
        CALL    CSLOW           ;SET CS INACTIVE
        RET                     ;DONE
;
;       WRITE DATA SUBROUTINE
;
;       USE FOR "WRITE" AND "WRALL" COMMANDS
;
;       WRITES COMMAND AND DATA TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;       EXPECTS DATA    TO BE IN D&E REG
;       ASSUMES EEPROM IS WRITE ENABLED
;
WRDATA:
        CALL    PRECK           ;PRELIMINARY CKS
        CALL    SHIFT8          ;SEND COMMAND
        CALL    SHIFT16         ;SEND DATA
        CALL    CSLOW           ;SET CS INACTIVE
        RET
;
;       THIS ROUTINE DOES A PRECHECK OF THE EEPROM STATUS
;
;       IT SETS CS ACTIVE
;       WAITS AT LEAST 500 NS
;       LOOPS TILL NOT BUSY
;       LEAVES CS ACTIVE, DATA OUT LOW
;       IT EXPECTS PORT DATA IN C REG
;
PRECK:
        PUSH    AF              ;SAVE
        LD      A,C             ;GET PORT DATA
        AND     0FDH            ;MASK CLK & DATA LOW
        OR      4               ;SET CS ACTIVE
        LD      C,A             ;SAVE
        OUT     (EE),A          ;WRITE TO PORT
PRECK1:
        IN      A,(EE)          ;READ PORT
        AND     80H             ;ACC = 0 IF BUSY
        JP      Z,PRECK1        ;LOOP UNTILL NOT BUSY
        POP     AF              ;RESTORE
        RET                     ;ELSE DONE
```

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```
;
;       THIS ROUTINE SHIFTS OUT 8 BITS OF COMMAND (+ START BIT)
;
;       IT WRITES TO A PARALLEL PORT WHOSE OUTPUTS ARE CONFIGURED AS:
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       IT SENDS A START BIT (LOW TO HI TRANSITION)
;       THEN IT SENDS DATA MSB FIRST
;       IT EXPECTS PORT DATA IN C REG
;       IT DESTROYS H,L,B
;
SHIFT8:
        PUSH    AF              ;SAVE
        CALL    STRTBT          ;SEND START BIT
        LD      B,7             ;LOOP COUNTER
        LD      A,L             ;ADDRESS
        OR      H               ;COMBINE WITH OPCODE
        LD      L,A             ;SAVE IN L
SNDBIT:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     L               ;CK MSB OF DATA
        JP      NC,SH8LP        ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH8LP:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBIT       ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT 8 BITS
;
        POP     AF              ;RESTORE
        RET                     ;
```

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```
;
;       THIS ROUTINE SHIFTS OUT 16 BITS OF DATA
;
;       IT WRITES TO A PARALLEL PORT WHOSE OUTPUTS ARE CONFIGURED AS:
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       <DE> HOLDS DATA TO BE SENT (MSB FIRST)
;
SHIFT16:
        PUSH     AF
        PUSH    DE              ;
        LD      B,7             ;LOOP COUNTER
SNDBT:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     D               ;CK MSB OF FIRST BYTE OF DATA
        JP      NC,SH16LP       ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH16LP:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBT        ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT FIRST 8 BITS
;
        LD      B,7             ;LOOP COUNTER
SNDBT1:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     E               ;CK MSB OF SECOND BYTE OF DATA
        JP      NC,SH16LP1      ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH16LP1:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBT1       ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT ALL 16 BITS
;
        POP     DE              ;
        POP     AF              ;RESTORE
        RET                     ;
```

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```
;
;       SEND A START BIT
;
STRTBT:
        PUSH    AF              ;SAVE ACC
        LD      A,C             ;GET PORT CONTENTS
        AND     0FCH            ;MASK CLK & DATA LOW
        OUT     (EE),A          ;SEND IT
        OR      1               ;DATA = 1
        OUT     (EE),A          ;SET UP DATA
        OR      2               ;CLK = 1
        OUT     (EE),A          ;SEND
        AND     0FDH            ;CLK = 0
        OUT     (EE),A          ;SEND
        LD      C,A             ;SAVE NEW CONTENTS IN C
        POP     AF              ;RESTORE ACC
        RET                     ;
;
;       SET CS LOW (INACTIVE)
;
;       ALTERS C REG
;
CSLOW:
        PUSH    AF              ;SAVE
        LD      A,C             ;GET PORT DATA
        AND     0F8H            ;SET CS LOW (AND DATA AND CLK)
        LD      C,A             ;SAVE
        OUT     (EE),A          ;WRITE TO PORT
        POP     AF              ;RESTORE
        RET                     ;DONE


        END
```

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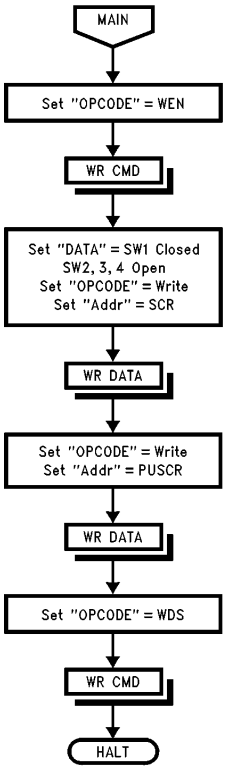
Main Loop



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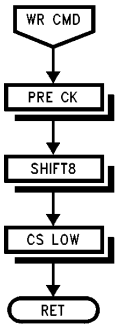
Write Command to NM95C12



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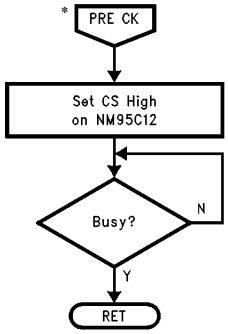

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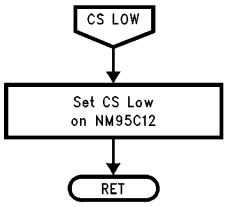
*Pre-check of NM95C12 sets CS active. Returns when NM95C12 not busy.



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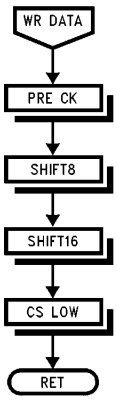
Write Data (16 Bits) to NM95C12



CS Active
Wait Till Not Busy

Send OPCODE + ADDRESS

Send Data

CS Inactive

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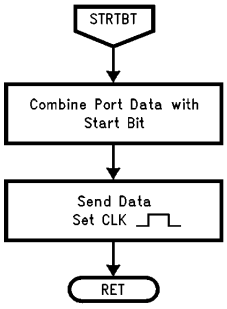
Send Start Bit to NM95C12



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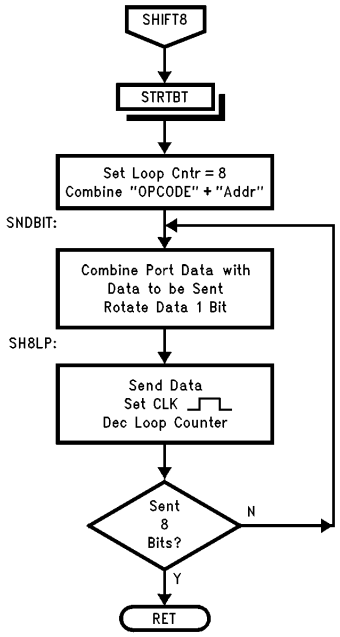
Shifts 8 Bits into the NM95C12 via the Data IN Pin



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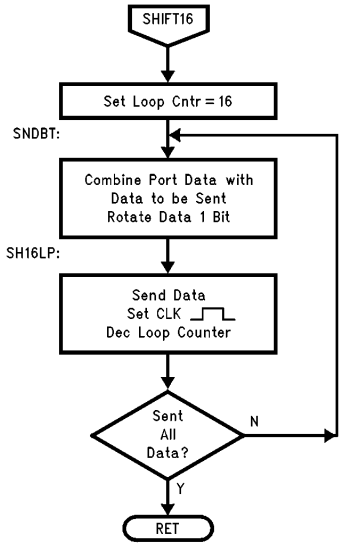
Shift 16 Bits of Data to NM95C12



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