NM95C12 Memory Mapping Solution for PC® Applications

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Christian Plourde
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INTRODUCTION

The design of an adapter card for a PC requires some knowledge of the different mechanisms used by the PC to access or exchange data with the adapter card.

The complexity of the mechanism used depends upon the level of functionality one wishes to implement on his design. At the low-end, the PC will access the adapter card as a simple I/O location, where for the more sophisticated cards, a BIOS will be incorporated onto the adapter card which may also use memory, I/O, interrupts and DMA channels from the PC.

This note discusses how to use the NM95C12 as a low cost solution for the implementation of high-end features on a general purpose adapter card for a PC.

1.0 OVERVIEW OF THE PC AND THE ADAPTER CARDS

In order to fully understand the possibilities offered by using an NM95C12 at the interface level between the PC and its adapter card, let's review the characteristics of that interface.

1.1 The PC has a certain amount of memory available for adapter cards. Both the location and space occupied by this memory vary depending on the type of PC (XT, AT). The XT reserves memory locations for 8-bit data transfers onto the adapter cards. The AT reserves the same locations for 8-bit data transfers but also reserves additional space for 16-bit data transfers.

1.2 The same mechanism applies to the I/O locations on the PC that are reserved for accesses onto an adapter card. A certain amount of I/O addresses will allow the PC to perform 8-bit data transfers with the adapter card on an XT system and some more locations will additionally be made available for 16-bit data transfers with the adapter card on an AT system.

1.3 Any adapter card you install into a PC is allowed to request interrupt service from the main PC card. An XT system offers the adapter card 6 interrupt lines where an AT system offers an additional 5 lines. (Not all of these lines are directly available for the adapter cards since some of them will be used by other cards on the PC.)

1.4 Finally, some DMA channels on the PC main board can be used by the adapter card through proper handling of DMA REQUEST and DMA ACKNOWLEDGE lines available on the PC connector. As for the other mechanisms, 8-bit DMA data transfers are allowed on an XT system where both 8- and 16-bit DMA data transfers are allowed on an AT-based system.

2.0 POSITIONING THE ADAPTER CARD

Any designer which intends to use one or more of the data transfer paths described above is aware that his card will have to carry the ability to be mapped into the available areas on the system, since other cards already installed into the PC probably make use of a part of the space reserved for the adapter cards.

2.1 If the adapter card contains memory accessible from the PC main board, up to two different levels of mapping may take place depending on the size of the memory. For a small memory size (let's say 8K or less), the entire area will be linearly accessible from the PC but its location will have to be mappable at different places into the range reserved for the adapter cards, thus ensuring that it will not interfere with any other cards using parts of this range. For larger memory, a second level of mapping is required, partitioning the memory into software selectable windows of 2K, 4K, 8K, etc. which location will still be mappable into available areas as described above (see *Figure 1*).

2.2 The same procedure applies to I/O locations on the adapter card. Any peripheral address has to have the possibility to be accessed at different selectable locations into the I/O address range reserved for adapter cards, thus ensuring that there won't be any address conflict with peripherals from other cards already installed into the system.

2.3 If the adapter card has the ability to request interrupt service from the PC main board, it also has to have the possibility to select the interrupt line it will use among those not being used by other adapter cards.

2.4 Finally, as for the interrupt lines, an adapter card using DMA channels must be able to select channels not used by other adapter cards.

3.0 TWO ISSUES: POSITIONING AND INITIALIZING

The most widely used way of implementing all of the above options is to install jumpers on the adapter card which setting will allow the end user to position its card into the available areas (see *Figure 2*). Even though this method has some disadvantages, like the fact that the user has to open the PC and remove the adapter card each time he has to modify the setting and the fact that a description of the settings allowed has to be carried along with the adapter card, it remains one of the cheaper and most easy to implement methods of positioning an adapter card into a PC.

Let's now consider some other interesting features that could be implemented on an adapter card. Once the application software is loaded from a diskette usually provided with the card, it may be possible to initialize and then to configure the card. For example, if the card is a data communication product, its on-board peripherals first have to be properly initialized and then the overall configuration of the link has to be defined (the parity and stop bits, the baud rate and such parameters as flow control, echoing, DCE or DTE arrangement, split clocking, etc. for either asynchronous or synchronous data transmission). Once all these parameters have been defined, the card should be operational as long as the power feeds the system.

An interesting step further in functionality would then be the implementation of some non-volatile data storage area on board into which the actual initialization and configuration of the adapter would be stored and referred to at any subsequent call of the application software following a power-up.

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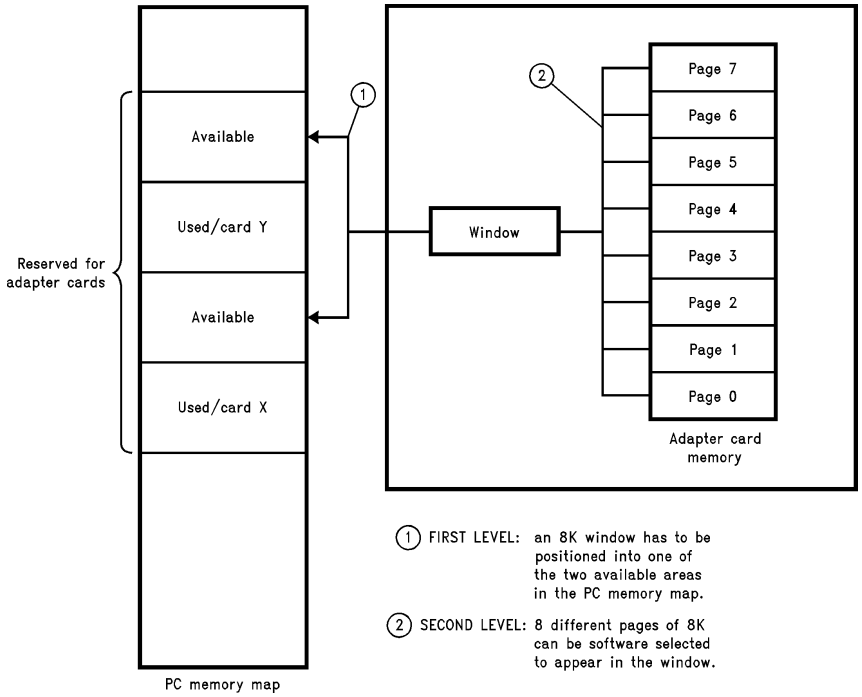

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FIGURE 1. Partitioning of 64K of Memory through an 8k Window Positioned into One of Two Available Areas in the PC Memory Map

If a BIOS is installed on the adapter card, the user could even be prompted to verify and modify (if required) the configuration of the card right away at power-up, since the BIOS signatures are scanned and given control after the usual diagnostics executions, graphic card, floppy and hard-disk recognition.

4.0 USE OF AN NM95C12 ADDS POWERFUL FEATURES TO YOUR ADAPTER CARD

The proposed application is to provide the PC with the possibility to access an NM95C12 located on the adapter card. The BIOS on the adapter card would instruct the PC to verify the status of a configuration flag stored in the NM95C12. If the status indicates that the card hasn't been initialized and configured yet, the user will be requested to accomplish these tasks prior to any further operation of the adapter card. Once the initialization has been properly loaded and saved, the BIOS, at any subsequent power-up, will simply instruct the user of the current configuration and ask if any modification is required.

The initialization portion of the card would make use of both the non-volatile memory and the dip switch's replacement features on the NM95C12. The positioning of the memory, the selection of the I/O addresses range and the interrupt lines or DMA channels (if required) would be set using the dip switch's replacement according to the user selection at first initialization. The other bytes or words used to initialize the peripherals on the adapter card would be stored in the NM95C12. All the configuration parameters related to the software operation of the card would also be saved into the NM95C12.

It is understood that such a solution does not eliminate all the jumpers or dip switches' on the adapter card. The location of the BIOS implemented on the card and the I/O address used to access the NM95C12 both have to be determined and set prior to the installation of the card into the PC. There is no easy way, if any, to work around such restrictions.

The circuit on *Figure 3* shows a simple way to implement an interface to the PC that will allow the user to position an 8K window of memory into one of eight possible locations in the adapter card's reserved area. He will have the possibility to select one of eight possible ranges of addresses for the I/O address of the peripherals on board and he will also be able to select one of four interrupt lines available on the PC connector. The memory on the adapter card consists of 32K of RAM divided into four pages of 8K. The selection of the page is performed through a write operation of 2 bits in a register whose I/O location has been determined by the setting of the NM95C12.

At power-up, before the system has been initialized, the PC must have the possibility to access at least the BIOS on the adapter card (ROM BIOS on *Figure 3*). LK1 on *Figure 3* allows eight different locations for that BIOS in the PC memory range reserved for that purpose. Since that BIOS will verify the configuration byte or word into the NM95C12, the I/O addresses of the circuit that accesses the NM95C12 also have to be selected prior to the installation of the adapter card into the PC. This is done via LK2 on *Figure 3*.

The circuit that allows the accesses to the NMC9512 is very simple. A sequence of writes to a latch (Itch A on *Figure 3*)

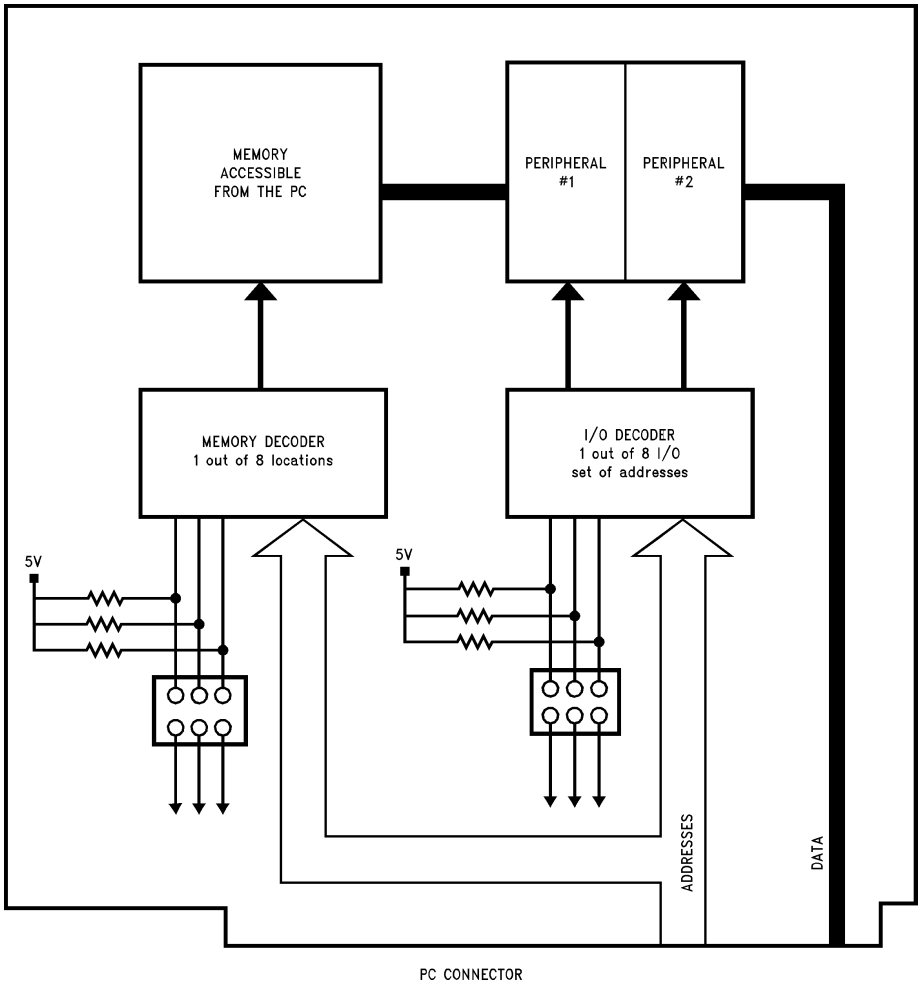

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FIGURE 2. Using Jumpers (or Dip Switches) to Position Both Memory and I/O Addresses on an Adapter Card

enables CS on the NM95C12, presents the data to be written to pin DI and latches this data into the NM95C12 by toggling the pin SK. The same principle applies to the read operation except that the bit output at pin DO of the NM95C12 is sent to the PC via a buffer (buff A on *Figure 3*).

The clock of latch A, the enable of buff A and the select and output enable of the ROM BIOS are all controlled by control A on *Figure 3* which may be a GAL.

The user is then allowed to position and configure its card. On the example of *Figure 3*, three lines of the NM95C12 are connected to the memory decoder. The status of these lines will position a window of 8K of RAM into one of eight possible locations in the PC memory area reserved for adapter cards. Three other lines of the NM95C12, connected to control B on *Figure 3*, will allow the same possibility for the I/O address of the peripherals on the adapter card. One of these peripherals is latch B into which the PC is now allowed to write two bits whose value will select one of the four pages of RAM to appear on the 8K window positioned by the first three lines of the NM95C12.

Finally, the two remaining lines of the NM95C12 are connected to the interrupt encoder on *Figure 3*, thus allowing the user to determine which interrupt line, out of four possible lines, he will select for his application.

Additional precautions should be added by the designer to ensure that a non-initialized card will not interfere with existing cards already plugged into the PC. A latch which status at power-up disables the interrupt encoder, the I/O and memory decoders, for example, could be reset by the PC once the proper configuration has been loaded or confirmed by the BIOS.

CONCLUSION

The implementation of similar features on a PC adapter card without the use of a NM95C12 would still require an EEPROM-like type of device in addition to some non-volatile latch mechanism. For such an application, the NM95C12 represents a simpler, cost-effective solution.

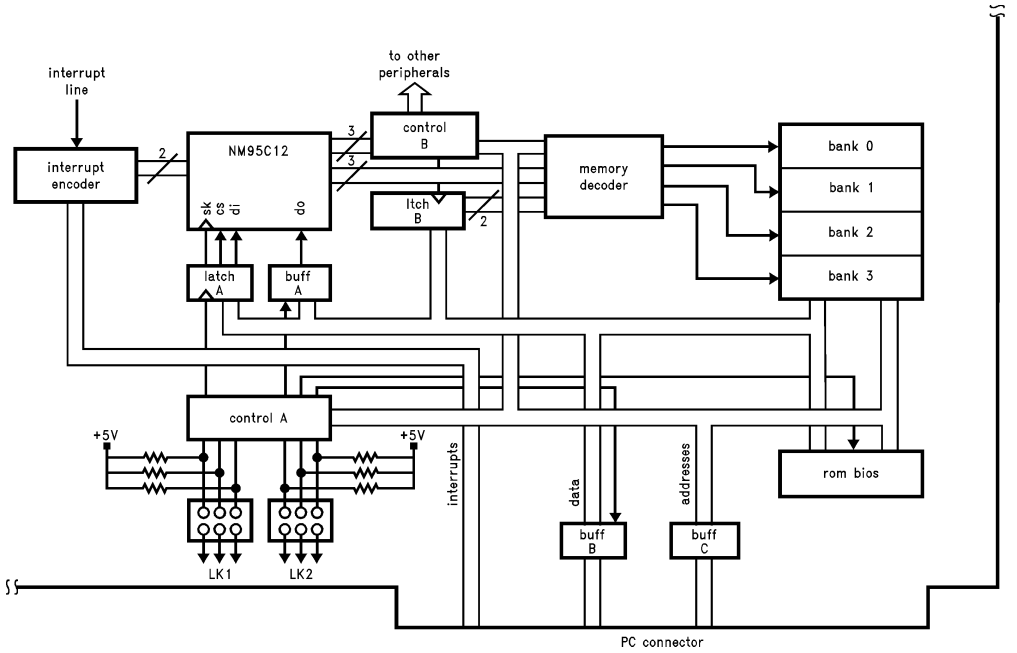

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FIGURE 3. A Powerful Use of the NM95C12 for a PC Interface

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998